Time Budgeting of the FlatLink™ Interface

Application Report

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Time Budgeting of the FlatLink Interface

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Time Budgeting of the FlatLink Interface

ABSTRACT
This document describes the FlatLink™ point-to-point data-transmission interface that provides better than a two-to-one reduction in the number of signal lines used for synchronous parallel data-bus structures.

Introduction
FlatLink is a point-to-point data transmission interface that provides better than a two-to-one reduction in the number of signal lines used for synchronous parallel data-bus structures with no loss in data throughput. To accomplish this reduction, the FlatLink interface receives single-ended data at clock frequencies up to 67 MHz and increases the data-signaling rate seven times up to ± 469 Mbps. At this transfer rate, the understanding and controlling of the interface timing is critical to successful designs. This application report defines the timing parameters and gives an example of a timing budget for a FlatLink interface.

This application report provides some guidelines for the time budgeting of the FlatLink interface. The guidelines are, by necessity, rather general and conservative due to the statistical nature of jitter and the uncertainties of the application constraints. An example budget is provided that can be adapted by users for their designs.

System Definition
The block diagram in Figure 1 shows a typical application of a FlatLink interface in which a host controller presents parallel single-ended input data to a FlatLink transmitter at a nominal clock frequency of 65 MHz. The data is compressed and transmitted differentially to a connector on the host circuit card and through one-half meter of unshielded twisted-pair cabling to a target connector. The target connector is mounted to a circuit board and connected to the inputs of a FlatLink receiver for data decompression and presentation to the target controller at a 65-MHz frequency.

FlatLink is a trademark of Texas Instruments Incorporated.
Figure 1. Typical FlatLink Interface

Host Controller-to-Transmitter

Beginning at the host controller, the data output setup time, $t_{su}$, and hold time, $t_{h1}$, relative to either the rising or falling edge of the clock should be ensured (see CLK1 and SIG1 in Figure 2). These parameters provide the amount of time the data signals are valid prior to and after the clock edge. The CLK1 and SIG1 signals from the host controller propagate over the conductive paths of the printed circuit board (PCB) to the inputs of the FlatLink transmitter. The time delay of any two paths (designated as $t_{d1}$ and $t_{d2}$ in Figure 2) is slightly different due to length and electrical property differences. This delay skewing of the signals reduces the setup and hold times available at the inputs (TXDn) to the FlatLink transmitter by the magnitude their maximum difference, $|t_{d1} - t_{d2}|$. $|t_{d1} - t_{d2}|$ must be held to less than $t_{su1}$ minus the transmitter-input setup time of 3 ns and $t_{h1}$ minus the transmitter-input hold time of 1.5 ns.

Transmitter to Receiver

The transmitter performs the parallel-to-serial conversions and outputs the serial-data streams. The conversion at a frequency of the internal clock (TX7XCLK) that is seven times that of CLK1. The time accuracy of the serial-data transition edges, with respect to the output clock (TXCLKOUT), is a function of the input-clock jitter and internal delay skews. With low input-clock peak-to-peak jitter (< 50 ps), the accuracy is $\pm 4200$ ps relative to the output-clock edges. This timing inaccuracy is designated as output skew, $t_{sk(o)}$, and is primarily caused by the differences in the internal delays of the transmitter.

$t_{sk(o)} = t_{n} - \frac{n}{7f_{CLKIN}}$

where $n = (0, 1, \ldots, 6)$

$t_{sk(o)}$

$t_{RSKM} = \frac{1}{14f_{CLKIN}} \pm 0.6$ ns
Because the data and clock outputs of the transmitter are synchronized to the same internal clock, the jitter-induced timing error at the transmitter outputs, $t_{sk(oj)}$, is the same as that which would occur during changes to TX7XCLK between TXCLKOUT transitions. There is no effective measurement of this effect and budgeting only can be made by an analytical approach. By modeling the PLL response as a simple single-pole low-pass filter with a -3-dB $f_0$, the response of the first TX7XCLK period to a unit-step change in the input-clock frequency can be approximated as shown in Equation 1.

$$t_{sk(oj)} = t_{j\text{in}} \left(1 - e^{-\frac{2\pi f_0 t_{c}}{7}}\right)$$

(1)

Where: $t_{j\text{in}} = \text{the magnitude of a unit-step change in the input clock period, } t_c$.

From the transmitter outputs, the difference in $t_{d3}$ and $t_{d4}$ decreases the data edge-placement accuracy at the host connector.

The interconnecting media or cable is, almost always, the prime contributor to timing uncertainty. In addition, delay skew and intersymbol interference (ISI) can be significant factors. The time uncertainty caused by ISI is a result of signal propagation velocity variation with frequency and is a function of the electrical properties of the media, its length, and the data pattern. When the serial-data streams reach the target connector, the time uncertainty of the data-edge placements is increased by $|t_{d3-4}|$, $|t_{d5-6}|$ and ISI over that of the transmitter outputs (see Figure 2).

After the signals reach the target connector, a small timing inaccuracy is added with the delay skew from $t_{d7}$ and $t_{d8}$ before the signals reach the inputs to a FlatLink receiver (see Figure 2).

The time uncertainty of a data-signal transition to the clock signal at the receiver inputs can be approximated as shown in equation 2.

$$\sum t_{sk} = t_{sk(o)} + t_{(oj)} + (t_{d3} - t_{d4}) + (t_{d5} - t_{d6}) + \text{ISI} + (t_{d7} - t_{d8})$$

(2)
Cable Delay, ISI, and Delay Matching (see Figure 3)

Figure 2. FlatLink Interface Timing Diagram

Cable Delay, ISI, and Delay Matching (see Figure 2)

Figure 3. FlatLink Interface Timing Diagram
Correct receipt depends upon valid data when latched by the internal receiver clock, RX7XCLK. This process is internal to the receiver and an indirect means of determining the internal setup and hold-time requirements is necessary. The setup and hold-time requirements can be determined by measuring the receiver skew margin, $t_{RSKM}$ (see Figure 3). To perform the measurement, the input-clock period must be stabilized. RXCLKIN is then advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is then $t_{RSKM}$ for that particular clock frequency and a direct measurement of the budgeted timing margin.

$$t_{RSKM} = \frac{t_c}{14} - 600 \text{ ps}$$  

(3)

By measurements and characterization with a stable $t_c$, the internal setup time, $t_{su}$, and hold time, $t_h$, is ensured to be less than $\pm 600$ ps. This allows $t_{RSKM}$ in the absence of jitter, to be determined as shown in equation 3. However, $t_c$ can be anything but stable and an allowance must be made for time variation of $t_c$ or jitter. A system-jitter model for the PLL response and identical PLLs for the transmitter and receiver is shown in Figure 4. The unit-step response of the first RX7XCLK period is shown in equation 4.

$$t_{jRX} = t_{jim} \left(1 - e^{-2\pi f_{j0}}\right) \left(1 - e^{-\frac{2\pi f_{j0}}{f_c}}\right)$$  

(4)
Since $t_{jRX}$ is an approximation for the variation of $t_c$ seen inside the receiver, it subtracts directly from $t_{RSKM}$. The major timing errors have been accounted for and the timing requirement is determined as shown in equation 5.

$$t_{jRX} + \sum t_{sk} < t_{RSKM} \quad (5)$$

**Receiver to Target Controller**

The FlatLink receiver performs the serial-to-parallel conversion and presents the parallel data (RXDn) 5 ns before and holds it 5 ns after the falling edge of the output clock (RXCLKOUT). Any of the RXDn bits are delayed over their path to the receiving controller and are skewed by the delay time difference $|t_{d9} - t_{d10}|$. This delay skew must be added to the 5-ns setup and hold times of the receiver to derive the setup time ($t_{su2}$) and hold time ($t_{h2}$) requirements of the receiving controller.

**Examples**

The timing budget of the interface is actually three distinct budgets; the host controller to the transmitter, the transmitter to receiver, and the receiver to the target controller. These budget examples are shown in Tables 1 through 3. All three tables exemplify a single transmitter and receiver operating at a nominal clock frequency of 65 MHz. Printed-circuit boards are assumed to be FR4 and controlled impedance.
### Table 1. Example Timing Budget Between Host Controller and FlatLink Transmitter

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM</th>
<th>TO</th>
<th>BUDGET</th>
<th>TIMING MARGIN</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{su1}$</td>
<td>Host controller</td>
<td>$t_{h1}$</td>
<td>5000 ps/5000 ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$</td>
<td>t_d1 - t_d2</td>
<td>$</td>
<td>Host controller</td>
<td>Transmitter</td>
<td>150 ps</td>
</tr>
<tr>
<td>$t_{su2}$</td>
<td>Transmitter</td>
<td>$t_{h2}$</td>
<td>3000 ps/1500 ps</td>
<td>850 ps/3350 ps</td>
<td></td>
</tr>
</tbody>
</table>

### Table 2. Example Timing Budget Between Transmitter and Receiver

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM</th>
<th>TO</th>
<th>BUDGET</th>
<th>TIMING MARGIN</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{RSKM}$</td>
<td>Receiver</td>
<td></td>
<td>490 ps</td>
<td></td>
<td>Equation 3 with $t_c = 15.4$ ns</td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>Transmitter</td>
<td></td>
<td>200 ps</td>
<td>290 ps</td>
<td>Worst case</td>
</tr>
<tr>
<td>$t_{sk(oj)}$</td>
<td>Transmitter</td>
<td></td>
<td>40 ps</td>
<td>250 ps</td>
<td>Equation 1 with $t_c = 15.4$ ns, $f_0 = 2$ MHz, and $t_{jin} = 1.5$ ns</td>
</tr>
<tr>
<td>$</td>
<td>t_d3 - t_d4</td>
<td>$</td>
<td>Transmitter</td>
<td>Host connector</td>
<td>30 ps</td>
</tr>
<tr>
<td>$</td>
<td>t_d5 - t_d6</td>
<td>$</td>
<td>Host connector</td>
<td>Target connector</td>
<td>60 ps</td>
</tr>
<tr>
<td>$t_{SI}$</td>
<td>Host connector</td>
<td>Target connector</td>
<td>40 ps</td>
<td>120 ps</td>
<td>0.5 m (3.28 ft) of good quality twisted-pair cable</td>
</tr>
<tr>
<td>$</td>
<td>t_d7 - t_d8</td>
<td>$</td>
<td>Peripheral connector</td>
<td>Receiver</td>
<td>60 ps</td>
</tr>
<tr>
<td>$t_{jRX}$</td>
<td>Transmitter</td>
<td>Receiver</td>
<td>50 ps</td>
<td>10 ps</td>
<td>Equation 4 with $t_c = 15.4$ ns, $f_0 = 2$ MHz, and $t_{jin} = 1.5$ ns</td>
</tr>
</tbody>
</table>

### Table 3. Example Timing Budget Between Receiver and Target Controller

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM</th>
<th>TO</th>
<th>BUDGET</th>
<th>TIMING MARGIN</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{su2}$</td>
<td>Receiver</td>
<td></td>
<td>5000 ps/5000 ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$</td>
<td>t_d9 - t_d10</td>
<td>$</td>
<td>Receiver</td>
<td>Target controller</td>
<td>150 ps</td>
</tr>
<tr>
<td>$t_{su2}$</td>
<td>Receiving controller</td>
<td>$t_{h2}$</td>
<td>4000 ps/2000 ps</td>
<td>850 ps/2850 ps</td>
<td></td>
</tr>
</tbody>
</table>
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