Using an LVDS Receiver with TIA/EIA-422 Data

Application Report

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When ground noise between the transmitter and receiver is less than ±1 V, Figure 1 denotes a circuit that uses a resistor divider circuit in front of the LVDS receiver that attenuates the 422 differential signal to LVDS levels.

The resistors present a total differential load of 100 Ω to match the characteristic impedance of the transmission line and to reduce the signal by a ratio of 10:1. The high input impedance of the LVDS receiver prevents input bias offsets and maintains a greater than 200 mV differential input voltage threshold at the inputs to the divider (see Note). This circuit is used in front of each LVDS channel that will receive 422 signals.

NOTE: The components used were standard values. The resistor values do not need to be 1% tolerance. The user may find other suppliers with comparable parts having tolerances of 5% or even 10%. These parts are adequate for use in this circuit.

R1, R2 = NRC12F45R3TR, NIC Components, 45.3 Ω, 1/8 W, 1% 1206 Package
R3, R4 = NRC12F5R11TR, NIC Components, 5.11 Ω, 1/8 W, 1% 1206 Package

Figure 1. TIA/EIA-422 Data Input to an LVDS Receiver Under Low Ground-Noise Conditions

If ground noise between the 422 driver and the LVDS receiver is a concern, the common-mode voltage must be attenuated also, and the circuit must be modified to connect the node between R3 and R4 to the LVDS receiver ground. This modification to the circuit increases the common-mode voltage range from ±1 Vdc to greater than ±4.5 Vdc. For even more common-mode voltage range, the SN65LVDS32B can be used.