Interoperability of M-LVDS and BusLVDS

Kevin Gingerich *High-Performance Linear/Interface Products*

ABSTRACT

M-LVDS is standardized in TIA/EIA-899 to enable interoperability of compliant interface circuits, such as the SN65MLVD200 from Texas Instruments. This report compares data sheet specifications, and makes a conclusion on the interoperability of the nonstandard BusLVDS (BLVDS) DS92LV010A from National Semiconductor and the SN65MLVD200.

1 Interface Definitions

We use the voltage and current definitions shown in Figure 1 for this analysis. We further define the steady-state driver common-mode output voltage as $V_{OS(SS)}$ and equal to $(V_A + V_B)/2$. V_{IT} is defined as the V_{ID} at which the receiver changes output state.

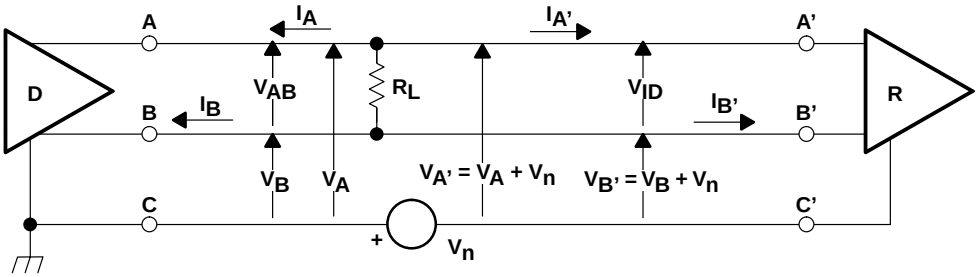

Figure 1. Interface Definitions

2 Discussion

The driver minimum differential output voltage magnitude, V_{AB}, in conjunction with the receiver maximum differential input voltage threshold magnitude, V_{IT}, determines the minimum differential noise margin available. Table 1 compares the worst-case differential noise margin available with different bus interface scenarios. V_{AB} comparison with different loads is accomplished by assuming the driver to be an ideal current source and scaling the specified values accordingly. The lowest differential noise margin exists on a BLVDS-only bus for any bus impedance or load.

Table 1. Differential Noise Margin Comparison

PARAMETER	SCENARIO			
	M-LVDS ONLY	M-LVDS to BLVDS	BLVDS ONLY	BLVDS to M-LVDS
V_{AB} min R_L = 27 Ω	260 mV	260 mV	140 mV	140 mV
V_{AB} min R_L = 50 Ω	481	481	259	259
V_{IT} max	50	100	100	50
Min margin R_L = 27 Ω	210	161	40	90
Min margin R_L = 50 Ω	431	383	159	209

The maximum $V_{AB,}$ along with the common-mode voltage, determines the voltage extremes seen at any node connected to the bus lines according to $V_{bus} = \frac{V_{AB}}{2} + V_{OS(SS)} + V_n$ where V_n is externally coupled noise voltage. Since all but V_n are fixed by specification, Table 2 calculates the external common-mode noise tolerance for different scenarios. The table calculates both a positive and negative noise margin, since it is not symmetrical. In the worst-case, a common-mode noise voltage of –475 mV would result in 0 V on the bus line with an M-LVDS driver to BLVDS on a 50-Ω bus. Note that the common-mode range is limited to the lowest of any device connected to the bus whether it is active or not.

Table 2. Common-Mode Noise Tolerance Comparison

PARAMETER	SCENARIO			
PARAMETER	M-LVDS ONLY	M-LVDS to BLVDS	BLVDS ONLY	BLVDS to M-LVDS
V_{AB} max R_L = 27 Ω	351 mV	351 mV	360 mV	360 mV
V_{AB} max R_L = 50 Ω	650	650	667	667
$V_{OS(SS)}$ min	800	800	1000	1000
$V_{OS(SS)}$ max	1200	1200	1650	1650
$-V_{bus}$	–1400	0	0	0
$+V_{bus}$	3800	2900	2900	2900
$+V_n$ R_L = 27 Ω	2425	1525	1070	1070
$-V_n$ R_L = 27 Ω	–2025	–625	–820	–820
$+V_n$ R_L = 50 Ω	2275	1375	917	917
$-V_n$ R_L = 50 Ω	–1875	–475	–667	–667

Input currents $I_{A'}$ or $I_{B'}$, the common-mode voltage range, and the common-mode drive capability of the driver constrain the maximum number of nodes that may be connected to a bus segment. The DS92LV010A and SN65MLVD200 specify the input currents to be very nearly the same over comparable bus voltage ranges, and no degradation in the maximum number of loads is expected from mixing the two devices on the same bus segment. The SN65MLVDS200 and the M–LVDS standard specify that the driver must be able to drive a common-mode load of 3.32 kΩ over a –1-V to 3.4-V range. This accommodates 32 worst-case loads and at least 1 V of noise voltage. There is no equivalent specification for the DS92LV010A and the maximum number of loads with a BLVDS driver cannot be determined.

The differential bias current from a receiver or high-impedance driver times the parallel combination of the bus termination resistors times the number of nodes connected gives an error voltage that subtracts from the noise margin. This is less than 4 μA for the SN65MLVD200. Thirty-two nodes with a differential bias current of 4 μA generates 6.4 mV across two 100-Ω resistors connected in parallel. This parameter is not specified for the DS92LV010A and its differential noise contribution is unknown.

Using the TIA/EIA-899 criteria for signal quality and the driver t_r and t_f, the maximum signaling rate for the DS92LV010A is 500 Mbps and 333 Mbps for the SN65MLVD200. This is due to the faster transition times of the DS92LV010A. Generally, fast transition times are undesirable in multipoint bus as stubs off the main backbone must be shorter to keep the reflections from them exceeding the differential noise budget.

3 Conclusion

The DS92LV010A and SN65MLVD200 are electrically compatible and interoperate, provided the differential and common-mode noise coupling to the interconnect falls within the capability of the desired scenario. The differential and common-mode noise margins of a purely M-LVDS bus are superior to any scenario that includes BLVDS. The top signaling rate of a bus comprised of the SN65MLVD200s and DS92LV010As using the TIA/EIA-899 signal quality criteria is 333 Mbps—however, the ultimate rate is application dependent.

4 References

1. *SN65MLVD200, SN65MLVD201, SN65MLVD202, SN65MLVD203, SN65MLVD204, SN65MLVD205 Multipoint-LVDS Line Drivers And Receivers, SLLS463, September 2001 – Revised May 2002*
2. *DS92LV010A Bus LVDS 3.3/5.0 V Single Transceiver, DS100052, May 1998*

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265