Difference Between the Intel™ 21150ac/bc and the PCI2050/2050B

Carmen Gonzalez, David Liu

Catalog Interface Solutions/Connectivity Solutions

ABSTRACT

This application report describes the functional difference between the Intel 21150ac/bc and the PCI2050/2050B. The PCI2050 is a 32-bit, 33-MHz PCI-to-PCI bridge that was designed to be pin-to-pin compatible with the Intel 21150ac. The PCI2050B is a 32-bit, 66-MHz PCI-to-PCI bridge that was designed to be pin-to-pin compatible with the Intel 21150bc.

Contents

1 PCI Local Bus Specification Differences ........................................................ 1
2 PCI Bus Power Management Interface Specification Differences ................ 1
3 Power-Up Difference ...................................................................................... 2
4 Fast Back-to-Back Transaction ...................................................................... 2
5 Register Differences ..................................................................................... 2
6 FIFO Size Differences .................................................................................. 2
7 References ..................................................................................................... 2

List of Tables

1 Mode Selection Via MS0 and MS1 .................................................................. 1

1 PCI Local Bus Specification Differences

Intel 21150 is PCI Local Bus Specification Rev 2.1 compliant. The PCI2050/2050B are PCI Local Bus Specification Rev 2.2 compliant.

2 PCI Bus Power Management Interface Specification Differences

Intel 21150 is PCI Bus Power Management Interface Specification Rev 1.0 compliant. PCI2050/2050B are architecture configurable for the PCI Bus Power Management Interface Specification via the MS0 and MS1 signals. Table 1 shows the mode selection via MS0 and MS1. When MS0 is pulled high, PCI2050/2050B are in Intel mode and are PCI Bus Power Management Interface Specification Rev 1.0 compliant. When MS0 is pulled low, PCI2050/2050B are in TI mode and are PCI Bus Power Management Interface Specification Rev 1.1 compliant.

Table 1. Mode Selection Via MS0 and MS1

<table>
<thead>
<tr>
<th>MS0</th>
<th>MS1</th>
<th>MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>CompactPCI™ hot swap friendly. PCI Bus Power Management Interface Specification Rev 1.1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>CompactPCI™ hot swap disabled. PCI Bus Power Management Interface Specification Rev 1.1</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>Intel compatible. CompactPCI™ hot swap disabled. PCI Bus Power Management Interface Specification Rev 1.0</td>
</tr>
</tbody>
</table>
3  **Power-Up Difference**

While the Intel 21150ac/bc does not have a specific power-up sequence, TI recommends that P_VCCP and S_VCCP be powered-up first before applying power to VCC.

4  **Fast Back-to-Back Transaction**

Intel 21150ac/bc supports fast back-to-back transaction as a master and as a target. The PCI2050 supports fast back-to-back transaction only as a target. The PCI2050B supports fast back-to-back transaction as a master and as a target.

5  **Register Differences**

The PCI2050/2050B have a Device ID of AC28h and a Vendor ID of 104Ch. The Revision ID for the PCI2050 is 00h, and the Revision ID for the PCI2050 is 02h.

For PCI2050/2050B, the Hot-Swap Control and Status Register has been added for CompactPCI hot swap support. While in CompactPCI hot swap mode, the Hot-Swap Control and Status Register can be used to control the hot-swap functionality of the PCI2050/2050B. The PCI2050/2050B can be set up to signal ENUM#.

The default state of the Posted Write Combining is enabled in PCI2050B, and is disabled in Intel PCI21150.

6  **FIFO Size Differences**

For the PCI2050B, the FIFO size is 32 DW for delayed responses (3 each direction) or 64 DW posted write and delayed request FIFO (1 each direction).

7  **References**

1. Advanced Configuration and Power Interface (ACPI) Revision 1.0
2. PCI Local Bus Specification Revision 2.2
3. PCI Mobile Design Guide, Revision 1.0
4. PCI-to-PCI Bridge Architecture Specification Revision 1.1
5. PCI Bus Power Management Interface Specification Revision 1.1
6. PICMG Compact-PCI Hot Swap Specification Revision 1.0
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI’s standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifiers</td>
<td>Audio</td>
</tr>
<tr>
<td>Data Converters</td>
<td>Automotive</td>
</tr>
<tr>
<td>DSP</td>
<td>Broadband</td>
</tr>
<tr>
<td>Interface</td>
<td>Digital Control</td>
</tr>
<tr>
<td>Logic</td>
<td>Military</td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>Optical Networking</td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>Security</td>
</tr>
<tr>
<td></td>
<td>Telephony</td>
</tr>
<tr>
<td></td>
<td>Video &amp; Imaging</td>
</tr>
<tr>
<td></td>
<td>Wireless</td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated