ABSTRACT
This document includes guidelines and recommendations for implementing the SN65DSI83, SN65DSI84, or SN65DSI85 in system hardware. These recommendations are only guidelines and it is the designer’s responsibility to consider all system characteristics and requirements. The engineers should refer to the datasheets for technical details such as device operation, terminal description, and so forth.

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1 Overview

1.1 What are SN65DSI83, SN65DSI84 and SN65DSI85?

The three devices: SN65DSI83, SN65DSI84 and SN65DSI85 will be referred to as SN65DSI8X in this document. SN65DSI8X is an MIPI DSI-to-LVDS bridge device that supports video modes in forward direction. The SN65DSI8X is primarily targeted for portable applications such as tablets and smart phones that utilize the MIPI DSI video format. The SN65DSI8X can be used between a GPU with DSI output and a video panel with LVDS inputs.

All three devices share the same pin out and package.

Table 1 lists a summary of the feature sets on these devices.

<table>
<thead>
<tr>
<th>Part Name</th>
<th>Description</th>
<th>Max Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN65DSI83</td>
<td>Single Channel DSI to Single-Link LVDS</td>
<td>Suitable 1366x768/1280x800 60 fps at 24 bpp/18 bpp</td>
</tr>
<tr>
<td>SN65DSI84</td>
<td>Single Channel DSI to two Single-Link LVDS</td>
<td>1920x1200 60 fps at 24 bpp/18 bpp</td>
</tr>
<tr>
<td>SN65DSI85</td>
<td>Dual Channel DSI to two Single-Link LVDS</td>
<td>2560x1600 60 fps, 1920x1080p 120 fps at 24 bpp /18 bpp</td>
</tr>
</tbody>
</table>

(1) Each DSI Channel has 4 DSI data lanes + 1 CLK lane. Each LVDS link has 4 data lanes + 1 CLK lane.
2 Hardware Implementation Guidelines

2.1 Layout Recommendation

2.1.1 Parts and Component Placement

2.1.1.1 VCORE Pin
This pin outputs 1.1 V from the internal voltage regulator. The pin MUST have a 1-µF external capacitor to GND.

2.1.1.2 REFCLK
A series resistor is recommended near the RECLK source for EMI reduction purpose. If possible, bury the REFCLK trace in the inner layer, or minimize the trace length from the REFCLK terminal to the CLK source by placing the source near the SN65DSI8X REFCLK terminal, or do both.

2.1.1.3 Decoupling Capacitors
Decoupling capacitors should be placed near the power plane and power rails for the SN65DSI8X. The trace length between decoupling capacitors must be minimized to avoid large current loops and trace inductance. The use of four ceramic capacitors (two 0.1 µF and two 0.01 µF) near the SN65DSI8X is recommended.

2.1.2 Critical Routes

• DA*P/N and DB*P/N pairs should be routed together with controlled-differential 100-Ω impedance. Keep away from other high speed signals. Keep lengths within 5 mil of each other. Keep traces on layers adjacent to ground plane. The number of VIAS should be kept to a minimum. Each pair should be separated at least by 3 times the signal trace width. Route all differential pairs on the same group of layers (outer layers or inner layers) if not on the same layer.

• A_Y*P/N and B_Y*P/N pairs should be routed together with controlled differential 100-Ω impedance. Keep away from other high speed signals. Keep lengths within 5 mil of each other. Keep traces on layers adjacent to ground plane. The number of VIAS should be kept to a minimum. Each pair should be separated at least by 3 times the signal trace width. Route all differential pairs on the same group of layers (outer layers or inner layers) if not on the same layer.

• Ref CLK trace should be routed as short as possible.

2.1.3 Spread Spectrum CLK
The system is allowed to provide the center spread CLK input to the REFCLK or DSI CLK for EMI reduction purpose. The center spread CLK input to the REFCLK or DSI CLK is passed through to the LVDS CLK output A_CLKP/N or B_CLKP/N. The spread depth can be 0.5% to 2% with 30 Hz to 50 Hz of modulation frequency range.
The layer stack up of the board in Figure 1 is as shown in the following:

*6-layer PCB*
Layer 1: Top component side
Layer 2: GND
Layer 3: Signal Route
Layer 4: Power
Layer 5: GND
Layer 6: Bottom component side

2.2 **RESET Implementation**

The SN65DSI8X is reset by controlling the EN terminal (pin B1). The reset implementation defined in the datasheet should be followed for correct operation of the device after the reset.

Figure 2 and Figure 3 depict the reset timing. User should refer to the datasheet for further details on reset operation.

Figure 2 shows the EN implementation during cold start when the device is first powered on. \( T_{\text{enable}} \) must be always greater than \( T_{\text{vcc}} \). In case of using the passive reset circuitry, this timing must be insured by using the correct values of \( R \) and \( C \) which could vary depending on the ramp up time of the system. The internal \( R \) value on the EN is 200 k\( \Omega \).
Figure 2. Cold Start Vcc Ramp Up to EN

Figure 3 shows the EN implementation while the device is powered on. The following timing must be met when the SN65DSI8X transitions from a normal operation state to a RESET or SHUTDOWN state while Vcc remains high.

Figure 3. RESET or SHUTDOWN Timing When Vcc = HIGH

2.3 ADDR

The ADDR determines the least significant bit of the I²C ADDR for the SN65DSI8X. This bit should be pulled high or low through a resistor depending on the I²C address the system chooses to use for the SN65DSI85. When this pin is pulled low, the device address is 0x2C, high 0x2D.

NOTE: When it is pulled high, it must be tied to the device Vcc such that this pin does not remain high when the device power is removed.

2.4 LVDS REVERSE Routing Option

The SN65DSI85 allows reversing or swapping the order of the LVDS pins via the register bit control at address 0x1A per the definitions below.

2.4.1 LVDS Even Odd Swap Option

By setting the 0x1A bit6 EVEN_ODD_SWAP bit in the CSR, the routing of even and odd pixels can be swapped. When this bit is set to 0 (default), odd pixels are routed to LVDS Channel A (A_Y*P/N) and even pixels routed to LVDS Channel B (B_Y*P/N). When this bit is set to 1, odd pixels are routed to LVDS Channel B (B_Y*P/N) and even pixels routed to LVDS Channel A (A_Y*P/N).

2.4.2 LVDS Reverse Pin Order Option

The order of the LVDS pins for LVDS Channel A or Channel B can be reversed by CSR configurations at the address 0x1A bits 5 CHA.Reverse_LVDS and bit4 CHB.Reverse_LVDS.
### Table 2. Channel A LVDS Reverse Pin Order

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>CHA_REVERSE_LVDS=0 (Default)</th>
<th>CHA_REVERSE_LVDS=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>C8</td>
<td>A_Y0P</td>
<td>A_Y3P</td>
</tr>
<tr>
<td>C9</td>
<td>A_Y0N</td>
<td>A_Y3N</td>
</tr>
<tr>
<td>D8</td>
<td>A_Y1P</td>
<td>A_CLKP</td>
</tr>
<tr>
<td>D9</td>
<td>A_Y1N</td>
<td>A_CLKN</td>
</tr>
<tr>
<td>E8</td>
<td>A_Y2P</td>
<td>A_Y2P</td>
</tr>
<tr>
<td>E9</td>
<td>A_Y2N</td>
<td>A_Y2N</td>
</tr>
<tr>
<td>F8</td>
<td>A_CLKP</td>
<td>A_Y1P</td>
</tr>
<tr>
<td>F9</td>
<td>A_CLKN</td>
<td>A_Y1N</td>
</tr>
<tr>
<td>G8</td>
<td>A_Y3P</td>
<td>A_Y0P</td>
</tr>
<tr>
<td>G9</td>
<td>A_Y3N</td>
<td>A_Y0N</td>
</tr>
</tbody>
</table>

### Table 3. Channel B LVDS Reverse Pin Order

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>CHB_REVERSE_LVDS=0 (Default)</th>
<th>CHB_REVERSE_LVDS=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>B3</td>
<td>B_Y0P</td>
<td>B_Y3P</td>
</tr>
<tr>
<td>A3</td>
<td>B_Y0N</td>
<td>B_Y3N</td>
</tr>
<tr>
<td>B4</td>
<td>B_Y1P</td>
<td>B_CLKP</td>
</tr>
<tr>
<td>A4</td>
<td>B_Y1N</td>
<td>B_CLKN</td>
</tr>
<tr>
<td>B5</td>
<td>B_Y2P</td>
<td>B_Y2P</td>
</tr>
<tr>
<td>A5</td>
<td>B_Y2N</td>
<td>B_Y2N</td>
</tr>
<tr>
<td>B6</td>
<td>B_CLKP</td>
<td>B_Y1P</td>
</tr>
<tr>
<td>A6</td>
<td>B_CLKN</td>
<td>B_Y1N</td>
</tr>
<tr>
<td>B7</td>
<td>B_Y3P</td>
<td>B_Y0P</td>
</tr>
<tr>
<td>A7</td>
<td>B_Y3N</td>
<td>B_Y0N</td>
</tr>
</tbody>
</table>

#### 2.5 Unused DSI Channels or Lanes

Unused DSI input terminals (DA*N/P, DB*N/P) should be left unconnected or driven to LP11 state.

#### 2.6 RSVD Pins

The RSVD1 and RSVD2 are reserved pins. Leave these unconnected for normal operation.

#### 3 References

SN65DSI8X Datasheets ([SLLSEB9](#), [SLLSEC1](#), [SLLSEC2](#))
The number of capacitors and their values may vary depending on the system implementation:

- **SN65DSI83** implementation: All DB* pins and B_Y*&B_CLK* pins are NCs.
- **SN65DSI84** implementation: All DB* pins and B_Y*&B_CLK* pins are NCs.
- **SN65DSI85** implementation: All DB* pins and B_Y*&B_CLK* pins are NCs.

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**Figure 4. SN65DSI8X Reference Schematics**

- 1uF is min value.
- Place only if external CLK is used for LVDSOUT CLK
- A/B_CLKP/N. 15-Ohm is recommended for EMI reduction but may need to be adjusted depending on the CLK waveform.
- Place as close as possible to CLK source.
- Terminate to GND with a pull-down resistor if unused.
- Optional ref CLK for LVDS Pixel
- CLK 25MHz-154MHz
- LVDS RefCLK
- NOTE for SN65DSI83 and SN65DSI84 implementation:
  - SN65DSI83 implementation: All DB* pins and B_Y*&B_CLK* pins are NCs.
  - SN65DSI84 implementation: All DB* pins and B_Y*&B_CLK* pins are NCs.
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