**Application**

- The TLK10022 is used as an aggregation device aggregating four independent Display Port (DP) sources into one high speed serial link.
- The low speed serial data rate being received by the TLK10022 is 2.7Gbps.
- The low speed serial lanes are aggregated into one 10.8 Gbps high speed serial link that is transmitted downstream either optically or electrically.
- The high speed serial link is de-aggregated by a second TLK10022 with the four original DP data sources intact.
- The original DP data is then presented on four independent monitors completing the aggregation process.

**Key Requirements**

- **Voltage Supply:**
  - Core Supply: 1 V
  - I/O Supply: 1.5 V / 1.8 V
- **Clocking:** The TLK10022 supports a large range of frequency allowing support for many different applications. Some of the typical frequencies that the TLK10022 supports are:
  - 122.88, 125, 156.25, 153.6, 312.5 MHz

  **NOTE:** Other frequencies are supported.

**Video Demo Description**

- Resolution: 1280 x 720
- Four DP Sources: 2.7Gbps / Lane
- Data Format: 8b/10b Encoded DP Data

**System Impact**

Display Port video transmission using multiple serial links

- DP Video Sources
- Four DP Cables
- Each Link @ 2.7Gbps

Display Port video data aggregated over one serial link

- DP Video Sources
- Aggregated serial link @ 10.8 Gbps
- Lower cost – smaller diameter cabling
- Long cable transmission distances
- Future Scalability

**Provisioning**

- TLK10022 is configured for 4:1 operation; Byte Interleave Mode; Link Training Disabled; and REF_CLK 1
  - Write 0x2 to register 0x01
- Lane Marker Function Enabled For Lane Alignment
  - Write 0xABC to register 0x17

**Documentation References**

- TLK10022 EVM User’s Guide (SLLU187)
- TLK10022 EVM GUI Software (SLLU188)
- TLK10022 IBIS-AMI Model (SLLM231)

**Video Demo Description**

- Resolution: 1280 x 720
- Four DP Sources: 2.7Gbps / Lane
- Data Format: 8b/10b Encoded DP Data

**Block Diagram**

[Diagram showing the block diagram of the Video Aggregation using TLK10022 for Display Port interfaces.]
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