Application Report
SLLA350–October 2014

Video Aggregation HD–SDI Interface Application Sheet

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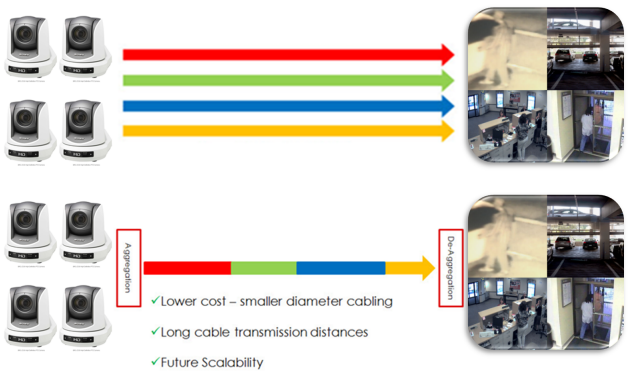
Application

- The TLK10022 is used as an aggregation device to combine four synchronous HD-SDI sources together into one high-speed serial link.
- The low-speed serial data rate being received by the TLK10022 is 1.485 Gbps.
- The low-speed serial lanes are then aggregated into one 5.94 Gbps high-speed serial link that is transmitted downstream either optically over an optical fiber or electrically via a differential connection.
- On the receiver side, the high-speed serial link is de-aggregated with another TLK10022 which outputs the four original HD-SDI data sources intact.
- The original HD-SDI data is then presented on four independent monitors completing the transmission of the four independent video sources.
- The TLK10022 also contains a 4:1 MUX that allows for data multiplexing of any input to any output. One example of using the MUX is in a broadcast mode where one camera's output is shared between multiple monitors.

Documentation References

- TLK10022 Product Folders
- TLK10022 Tools Folders
- TLK10022 EVM User's Guide (SLLU187)
- TLK10022 EVM GUI Software (SLLU188)
- TLK10022 IBIS-AMI Model (SLLM231)

System Impact



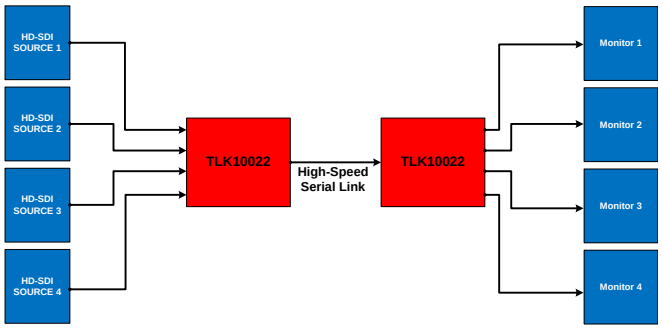
Key Requirements

- Voltage Supply:
  - Core Supply: 1.0 V
  - I/O Supply: 1.5 V / 1.8 V
- Clocking: The TLK10022 supports a large operating frequency range allowing support for many different applications. Some of the typical frequencies supported by the TLK10022 include:
  - 148.5, 297 MHz
    NOTE: Other frequencies are supported
- Synchronized Data Inputs
  NOTE: Synchronization can be achieved via a black burst generator, SDI frame buffer, or various other methods. End applications will vary in design.
- Data MUXing available through the built in high-speed cross point switch.
- Optical or electrical media support via the high-speed outputs.

Provisioning – Setting Up the Device

- The TLK10022 is configured for 4-lane operation; Bit Interleave Mode; Link Training Disabled; and REF_CLK 1
  - Write 0x2 to register 0x01
- Lane Marker Function Enabled For Lane Alignment
  - Write 0xABC to register 0x17 to enable the lane marker function
  - Write 0x2BC to register 0x17 to disable the lane marker function once lane alignment is achieved

Block Diagram



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