Application Report
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TUSB1310 Implementation Guide

Wes Ray

ABSTRACT

Texas Instruments' TUSB1310 is a single port, 5.0 Gbps USB 3.0 Physical Layer Transceiver available in a Lead-Free 175-Ball 12 x 12 nFBGA Package (175ZAY).

This application note describes general PCB layout guidelines for the TUSB1310. The Link Controller interfaces to the TUSB1310 are via a PIPE (16-bit wide operating and 250 MHz) and a ULPI (8-bit wide operating at 60 MHz) interface. The USB connector interfaces to the TUSB1310 via a USB 3.0 SuperSpeed USB Differential Pair (TX and RX) and USB 2.0 differential pair (DP/DM).

This document is intended for developers familiar with high-speed PCB design and layout. Knowledge of the USB 3.0 specification and USB protocol is required as well. The following layout recommendations are not the only way to layout a design and are only provided as a guide. The preferences of the individual developer, requirements of the design, number of components in the circuit, as well as many other factors will influence each individual layout.

REFERENCES

- Latest TUSB1310 Errata (SLLZ061)
- TUSB1310 Data Sheet (SLLSE32)
- TUSB1310 IBIS Model
- USB 3.0 Specification
  http://www.usb.org/developers/docs/

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1 Typical System Implementation

Figure 1 represents a typical implementation of the TUSB1310 USB 3.0 physical layer transceiver. It operates off of a single crystal or an external reference clock. The reference frequencies are selectable from 20, 25, 30, and 40 MHz. The TUSB1310 provides a clock to the USB Link Layer controllers. The single reference clock allows the TUSB1310 to provide a cost effective USB 3.0 solution with few external components and a minimum implementation cost.

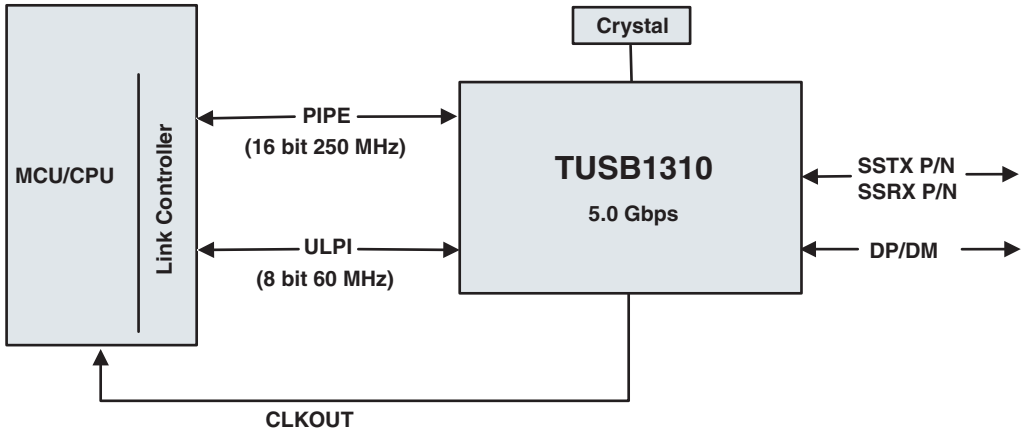

Figure 1. Typical System Implementation

2 General Implementation Guidelines

- Connect 1% 10-kΩ calibration resistor between R1EXT and R1EXTRTN, within 500 mils of the device. See Figure 2.
- Use appropriate high speed logic analyzer connectors on the PIPE and ULPI interfaces for initial prototypes.
- CEXT and CEXTSS (balls M14 and A14) are repurposed on the TUSB1310A. For the TUSB1310A, CEXTSS (ball A14) is not connected on the die; it becomes a No Connect pin. CEXT (ball M14) will need to be connected to VDDA (1.1 V), replacing the 4.7 nF with a bypass capacitor. Customers are encouraged to use a zero ohm resistor to VDDA for full compatibility with both versions of the device. See Section 11 and Section 12.
- Make sure all strap pins are at the desired voltage level.
- Perform post route analysis of the PCB/circuit. Contact TI for the TUSB1310 IBIS model.
- Check the latest errata.

3 Power Considerations

3.1 1.1-V and 1.8-V Digital Supply

The TUSB1310 requires 1.1-V and 1.8-V digital power sources.

The 1.1-V terminals are named VDD1P1. These terminals supply power to the digital core. The 1.1-V core allows for a significant reduction in both power consumption and logic switching noise.

The 1.8-V terminals are named VDD1P8 and supply power to the input and output cells.

Both VDD1P1 and VDD1P8 supplies must have 0.1-µF bypass capacitors to VSS (ground) in order for proper operation. The recommendation is one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors like 0.01-µF are also recommended on the digital supply terminals.

When placing and connecting all bypass capacitors, high-speed board design rules must be followed.

3.2 1.1-V, 1.8-V and 3.3-V Analog Supplies

Since circuit noise on the analog power terminals must be minimized, a Pi filter is recommended for each supply.

Analog power terminals should have a 0.1-µF bypass capacitor connected to VSSA (ground) in order for proper operation. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors like 0.01-µF are also recommended on the analog supply terminals.

3.3 Ground Terminals

VSS and VSSA can be connected together to form one ground plane. This technique allows for creating a big image plane for the signal layer directly adjacent to the ground plane.

3.4 Capacitor Selection Recommendations

When selecting bypass capacitors for the TUSB1310 device, X7R-type capacitors are recommended. The frequency versus impedance curves, quality, stability, and cost of these capacitors make them a logical choice for most computer systems.

The selection of bulk capacitors with low-ESR specifications is recommended to minimize low frequency power supply noise. Today, the best low-ESR bulk capacitors are radial leaded aluminum electrolytic capacitors. These capacitors typically have ESR specifications that are less than 0.01 Ω at 100 kHz. Also, several manufacturers sell “D” size surface mount specialty polymer solid aluminum electrolytic capacitors with ESR specifications slightly higher than 0.01 Ω at 100 kHz. Both of these bulk capacitor options significantly reduce lowfrequency power supply noise and ripple.

3.5 Power-Up/Down Sequencing

All TUSB1310 analog and digital power terminals must be controlled during the power-up and power-down sequence. Absolute maximum power terminal ratings must not be exceeded to prevent damaging the device. There is no requirement on which power rail be applied first nor does it matter which rail is removed first.

For additional power requirements, please reference the TUSB1310 Data Sheet (SLLSE32).

3.6 External Voltage Regulator Recommendation

Since the TUSB1310 requires three voltage supplies (1.1-V, 1.8-V, and 3.3-V) a multi-channel voltage regulator is recommended. The TPS6500x or TPS65024x are good choices.

The TPS6500x utilizes a DC/DC converter and two LDO regulators in a single package. The DC/DC converter can supply 600mA nominal current while the two LDO's can supply 300-mA nominal current. The DCDC converter is ideal for supplying the 1.1-V current while the two LDO's can be used to supply 1.8-V and 3.3-V current.

Likewise the TPS65024x utilizes three DC/DC converters and three LDO's. Both devices also have a built in supervisor circuit that can be connected to RESETN on the TUS1310.

While either of the two solutions mentioned here could be considered overkill for the TUSB1310 alone, they may make sense based on the USB device being implemented.

3.7 USB VBUS

VBUS is a 5-V source that is connected to the USB VBUS terminal on the TUSB1310 via a voltage divider. Connect a 90.9-k 1% resistor from the cable VBUS connector to the USB VBUS terminal on the TUSB1310 and a 10-k 1% resistor from USB VBUS to ground, see Figure 2.

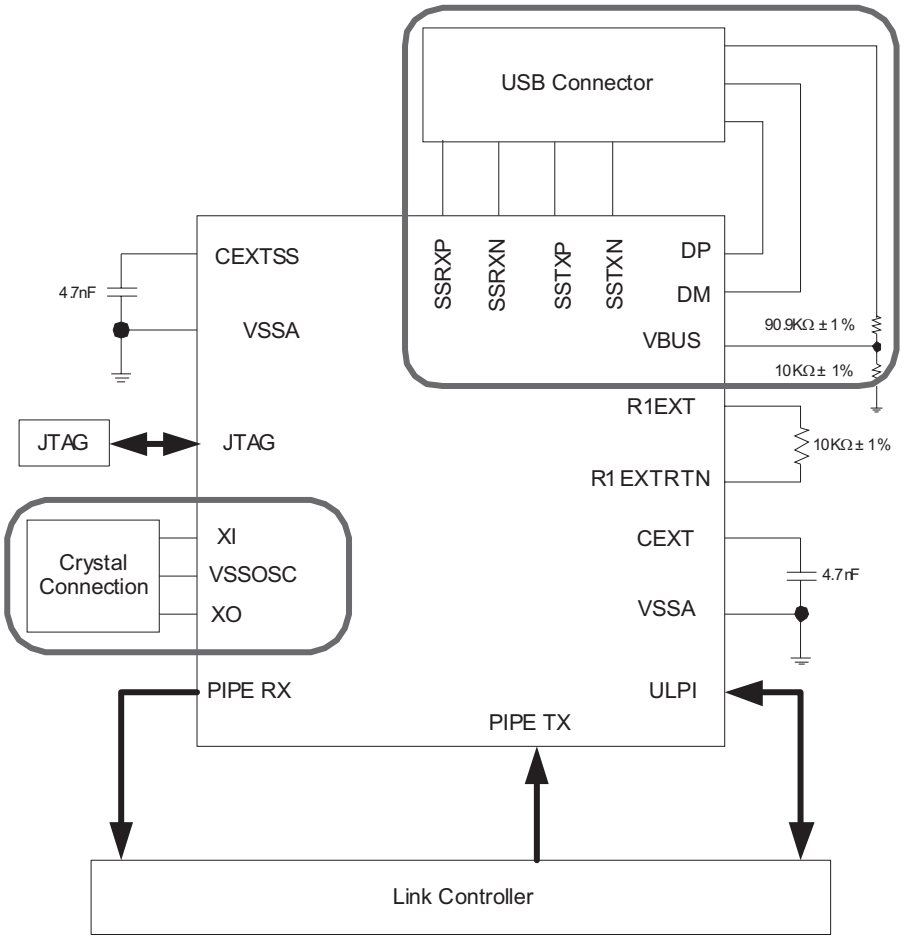

Figure 2. VBUS Connection

3.7.1 Limiting Inrush Current on VBUS

If the design is Bus Powered, use of the TI TPS2560/61 is recommended. Inrush current can occur on VBUS when a function is plugged into the network.

For example the bulk capacitance used to supply power to a SATA device can be quite large, causing inrush current when the USB cable is connected. The TPS2560/61 power-distribution switches are intended for applications where heavy capacitive loads are likely to be encountered.

4 Input Clock

The TUSB1310 supports an external oscillator source or a crystal unit. If a clock is provided to XI instead of a crystal, XO is left open and VSSOSC is connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow the guidelines below.

Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground if using a crystal. See Figure 3.

Load capacitance (Cload) of the crystal varying with the crystal vendors is the total capacitance value of the entire oscillation circuit system as seen from the crystal. It includes two external capacitors CL1 and CL2 in Figure 9. The trace length between the decoupling capacitors and the corresponding power pins on the TUSB1310 needs to be minimized. It is also recommended that the trace length from the capacitor pad to the power or ground plane be minimized.

See the TUSB1310 Data Sheet (SLLSE32) for input clock selection parameters.

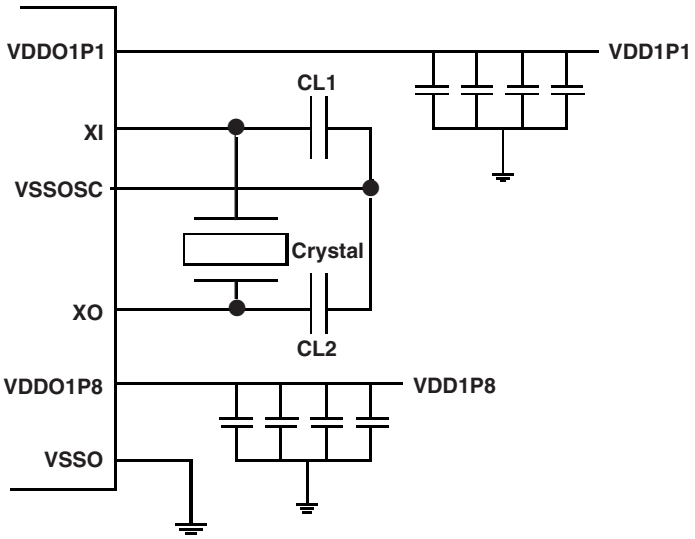

Figure 3. Crystal Connection

5 USB Connection

There are three sets of differential pairs for connecting the USB port. One set for high-speed and two sets for SuperSpeed.

5.1 High-Speed Differential Routing

The high-speed differential pair (USB_DM and USB_DP) is connected to a USB type B connecter. The diff pair traces should be routed with 90-Ω ±15% differential impedance. The high-speed signal pair should be trace length matched. Max trace length mismatch between High speed USB signal pairs should be no greater than 150 mils. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. No termination or coupling caps are required. If a common mode choke is required then place the choke as close as possible to the USB connector signal pins. Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke).

5.2 SuperSpeed Differential Routing

SuperSpeed consists of two differential routing pairs, a transmit pair (USB_SSTXM and USB_SSTXP) and a receive pair (USB_SSRXM and USB_SSRXP). Each diff pair traces should be routed with 90-Ω ±15% differential impedance. The high-speed signal pair should be trace length matched. Max trace length mismatch between SuperSpeed USB signal pairs should be no greater than 2.5 mils. The transmit diff pair does not have to be the same length as the receive diff pair. Keep total trace length to a minimum. Route differential traces first. Route the differential pairs on the top or bottom layers with the minimum amount of vias possible. The transmitter diff pair requires 0.1-µF coupling caps for proper operation. The package/case size of these caps should be no bigger than 0402. C-packs are not allowed. The caps should be placed symmetrically as close as possible to the USB connector signal pins. If a common mode choke is required then place the choke as close as possible to the USB connector signal pins (closer than the transmitter caps). Likewise ESD clamps should also be placed as close as possible to the USB connector signal pins (closer than the choke and transmitter caps).

It is permissible to swap the plus and minus on either or both of the SuperSpeed differential pairs. This may be necessary to prevent the differential traces from crossing over one another. However it is not permissible to swap the transmitter diff pair with the receive diff pair.

6 JTAG Interface

The TUSB1310 supports JTAG (IEEE 1149.1 and 1149.6) for board level test. Contact TI for TUSB1310 BSDL file.

7 PIPE Connection

The PIPE signals are 1.8-V LVCMOS. The source synchronous signals for each direction of the interface, see Table 1 for critical TX and RX signals, should be matched in length to within 250 mils. Other signals can be of different lengths but should be as short as possible.

Table 1. Matched Length PIPE Signals

SIGNAL NAME	TYPE
TX_CLK	TX
TX_DATA[15:0]	TX
TX_DATAK[1:0]	TX
PCLK	RX
RX_DATA[15:0]	RX
RX_DATAK[1:0]	RX
RX_VALID	RX

External source series termination resistors are not required if the interface is kept to less than two inches in length with an impedance of 50 Ω ±10%.

Routing this interface longer than two inches or through a connector is not recommended. If this must be done, special care must be taken to select the proper high-speed connector as well as modeling of the transmission line. Post route modeling of the circuit is recommended. Contact TI for the appropriate IBIS file.

8 ULPI Connection

The ULPI signals are 1.8-V LVCMOS. They should be as short as possible and matched in length, with a single ended impedance of 50 Ω ±10%.

9 ESD Protection

The TUSB1310 provides ESD protection on all signal and power pins up to 2000 V using the human body model and 500 V using the charged device model. If more protection is required then the TI TPD2EUB30 can be used, the device meets or exceeds IEC61000-4-2 (Level 4) requirements. This device can be used on any of the differential pairs of the TUSB1310. Place the device as close as possible to the signal pins of the connector. Refer to the datasheet for more information regarding this device.

10 FPGA Timing

Any FPGA can be used as long as it has IO cells capable of operating at the speeds required for the PIPE (250 MHz) and ULPI (60 MHz). Previous knowledge of high speed interface design is a benefit. Reference the PIPE and ULPI timing parameters defined in the TUSB1310 data sheet (SLLSE32).

For Xilinx Virtex-5 applications, the following are recommendations for improving PIPE3 I/O timing based on the Virtex-5 User's Guide (ug190.pdf).

- Deskew the PCLK clock input. See "Clock Deskew" in the "DCM Design Guidelines" section.
- Ensure PIPE interface signals are registered and FFs are packed in the ILOGIC/OLOGIC resources.
- Use ODDR to forward MCLK. See "Clock Forwarding" in the "Output DDR Overview" section and Figure 2-10. Also invert the output clock to center the data relative to the rising-edge of MCLK. This will ensure that the FPGA PIPE3 outputs to the TUSB1310 are aligned.

```
ODDR u_pipe3_mclk_oddr (
.Q(pipe3_mclk),
.C(pipe3_pclk_int),
.CE(1'b1),
.D1(1'b0),
.D2(1'b1),
.R(1'b0),
.S(1'b0));
```

Review the Xilinx timing reports. If the PIPE3 input timing does not align with the TUSB1310 output timing, it may be necessary to either adjust the PHASE_SHIFT of the PCLK DCM or use an IDELAY element on the inputs.

Anticipate several iterations of FPGA builds in order to tweak the PIPE and ULPI signals relative to the clock in order to meet the TUSB1310 AC characteristics.

11 TUSB1310 CEXT/CEXTSS Connections

CEXT and CEXTSS both need a 4.7-nF capacitor to ground as shown below.

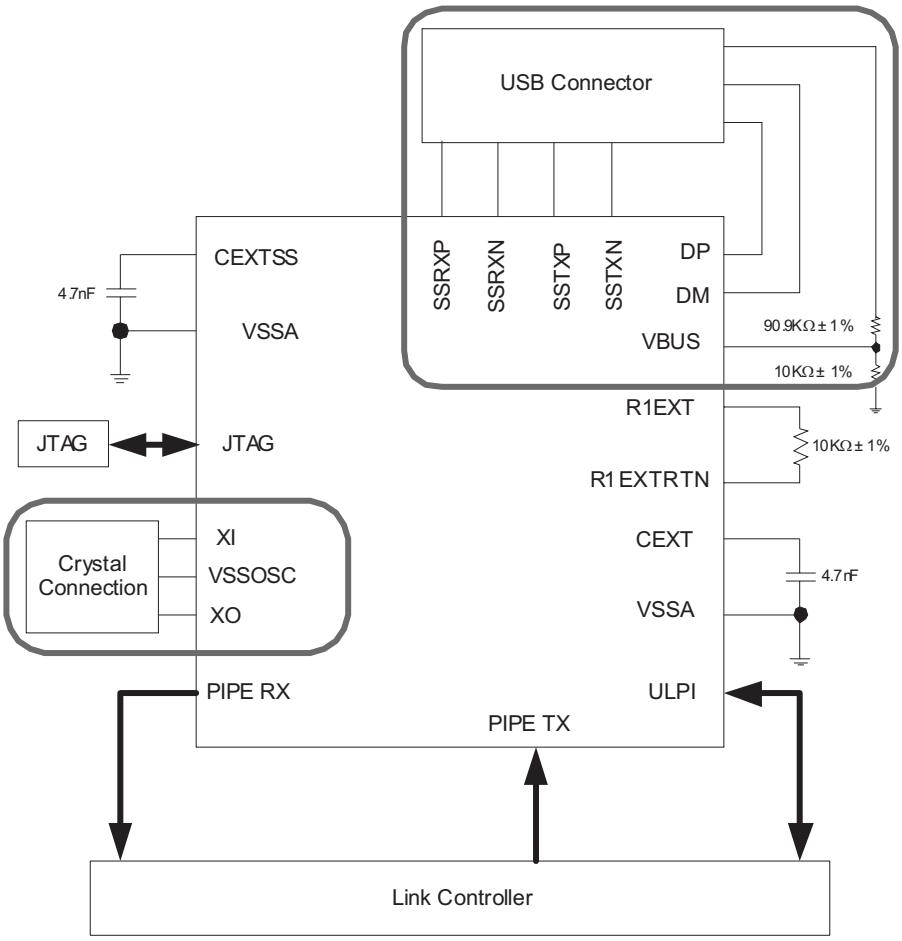

Figure 4. TUSB1310 Connections

12 TUSB1310A CEXT/CEXTSS Connections

CEXT and CEXTSS (balls M14 and A14) are repurposed on the TUSB1310A.

CEXT (ball M14) will need to be connected to VDDA (1.1 V), replacing the 4.7 nF with a 1-µF bypass capacitor. Customers are encouraged to use a zero ohm resistor to VDDA for full compatibility with both versions of the device.

CEXTSS (ball A14) is not connected on the die; it becomes a No Connect pin.

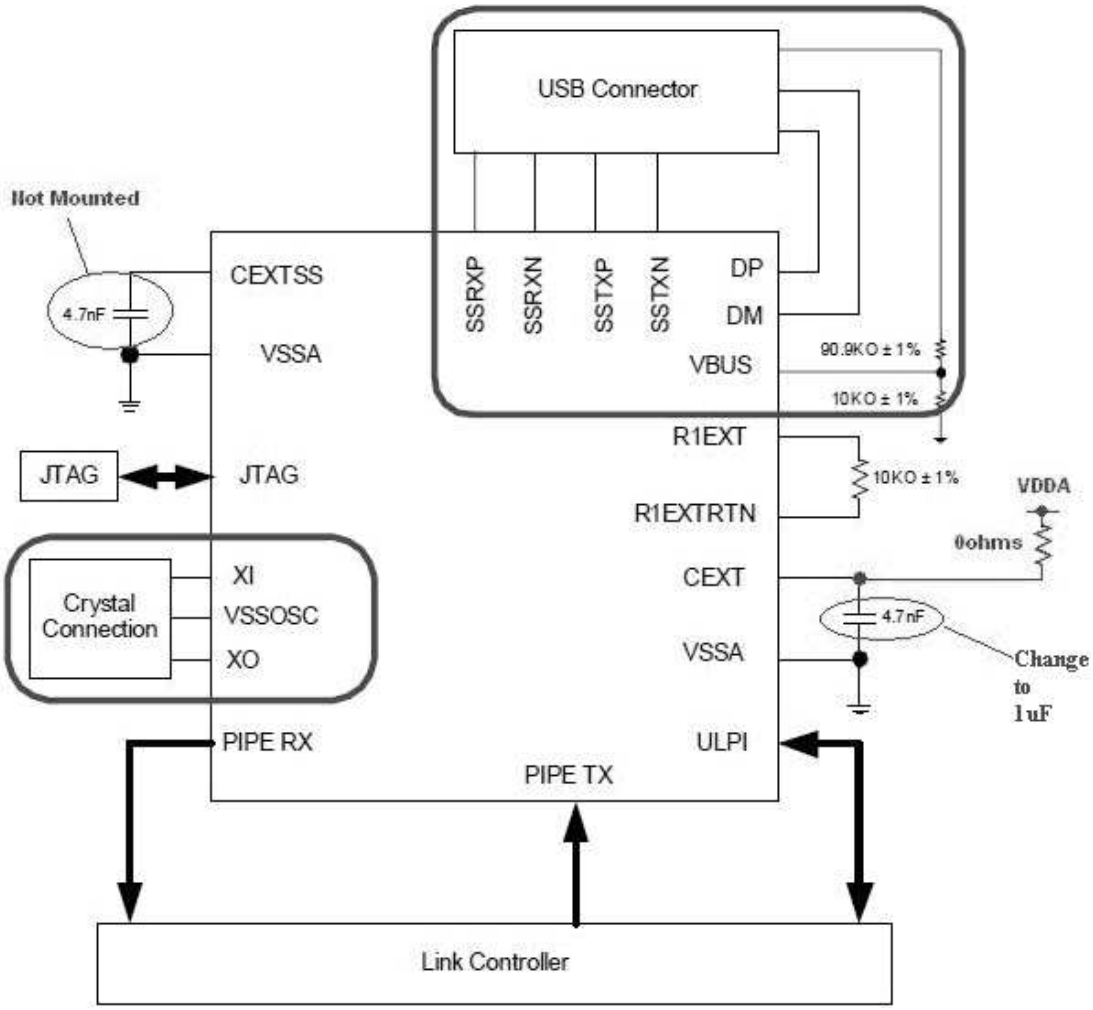

Figure 5. TUSB1310A Connections

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