Universal Battery Monitor
Using the bq2018 Power Minder™ IC

Features
- Counts charge and discharge for Li-Ion, NiCd, NiMH, and other chemistries
- Works with host controller to form comprehensive battery pack monitor
- Direct connection to battery stack
- Connects to 4 to 12 series NiCd/NiMH cells or 2 to 4 Li-Ion series cells; other configurations available
- Low operating current
- Measures a wide dynamic range of current
- Small size
  - Entire circuit can fit on less than 0.5 square inches of PCB space
- Low implementation cost
  - Fewer than 15 discrete components required

Typical Applications
- Cellular telephones
- Personal digital assistants
- Other portable handheld equipment

Figure 1. bq2018 Circuit Connection
General Description

The circuit shown in Figure 3 is a typical bq2018 Power Minder implementation. The battery is connected between BAT+ and BAT-. Q1 and C5, in conjunction with the REG output, regulate the supply voltage to the bq2018 to between 3.5V and 3.9V for the varying battery input at BAT+. The SR V-to-F input pins sense the charge and discharge current using the low-value resistor R1.

A microcontroller communicates with the Power Minder IC using an I/O port connected to the bq2018 HDQ pin. The microcontroller reads the charge/discharge and timer counters of the bq2018 and calculates remaining battery capacity for communication to the user or to the system’s power management controls. The bq2018 WAKE output pin alerts the microcontroller that charge/discharge activity greater than a programmable level is taking place.

The circuit monitors a battery pack of any chemistry. The typical operating parameters of the circuit are:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>Input voltage BAT+ to BAT-</td>
<td>3.5V to 18.0V</td>
</tr>
<tr>
<td>ISR</td>
<td>Measurable current range</td>
<td>±4A Max. (1)</td>
</tr>
<tr>
<td>ISOPR</td>
<td>Operating current</td>
<td>80µA</td>
</tr>
<tr>
<td>IS</td>
<td>Sleep current</td>
<td>10µA</td>
</tr>
<tr>
<td>ISBACK</td>
<td>Register backup current</td>
<td>&lt; 0.1µA (2)</td>
</tr>
</tbody>
</table>

(1) Assumes 50mΩ 1W sense resistor and bq2018 offset compensation.
(2) Provides years of backup time when using cell(s) from the battery stack.

Sense Resistor Selection

R1 must be sized properly to measure the entire range of charge and discharge currents in the application within the limits of the bq2018. The input parameters include:

1. The potential of the SR input is limited to -200mV to +200mV. The charge/discharge currents through the sense resistor must not produce a voltage greater than ±200mV.
2. The bq2018 counts charge and discharge at a rate of 12.5µV per hour. Signals < 12.5µV require greater than one hour to resolve. The designer should consider the resolution vs. time when selecting a sense resistor.

The sense resistor must also handle the power dissipation of all charge and discharge activity. The circuit example uses a 50mΩ 1W sense resistor.

Measurement Offset

The bq2018 has a calibration test mode that measures the offset of the bq2018 based circuit. A final test setup for the battery pack can enable this mode by setting the appropriate bits in the bq2018. When the bq2018 is in calibration mode, no charge/discharge current should be applied. In calibration mode, the bq2018 measures the circuit offset and latches a value in the offset adjustment register. The host microcontroller uses the value in the register to periodically adjust the charge and discharge count values from the bq2018.

Note: Board layout affects offset. C2, C3, and C5 should be as close to the bq2018 as practical. Figure 2 shows one example of how to lay out the circuit in Figure 3.

Parts List

<table>
<thead>
<tr>
<th>Item</th>
<th>Quantity</th>
<th>Reference</th>
<th>Part</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>U1</td>
<td>bq2018</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>R4, R6</td>
<td>1K</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>R5</td>
<td>100</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>R3, R2</td>
<td>100K</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>C1</td>
<td>0.1µF/1.0µF</td>
</tr>
<tr>
<td>6</td>
<td>3</td>
<td>C4, C2, C3</td>
<td>0.1µF</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>C5</td>
<td>0.01µF/0.001µF</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>Q1</td>
<td>SST108</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>D3</td>
<td>BAV99</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>R1</td>
<td>0.05Ω tolerance = 2%, Watt = 1W</td>
</tr>
<tr>
<td>11</td>
<td>2</td>
<td>D2, D1</td>
<td>B2X84C5V6 Zener</td>
</tr>
</tbody>
</table>

Figure 2. bq2018 Circuit Board Layout
Microcode Example for HDQ Interface

```assembly
; TITLE  "HDQ.ASM - 201XH INTERFACE"
;LAST UPDATE:  04/15/96
;TIMING VALUES ARE FOR 8.0Mhz CRYSTAL
;
;MASSIGNMENT
;
W  EQU  00H
PC  EQU  01H
STATUS EQU  02H ;PROGRAM COUNTER
X   EQU  04H  ;FILE SELECT
;
PORTB EQU  06H  ;PORTB 0 is HDQ line
;
TIMEOUT EQU  06H  ;TIMEOUT FLAG, 0=NO TIMEOUT
HSERDAT EQU  08H  ;HIGH SERIAL DATA REGISTER
HSERBIT EQU  0CH  ;HIGH SERIAL BIT COUNTER
WTACK  EQU  0DH  ;TEMP STORE FOR W REGISTER
;
HCMD  EQU  0FH  ;HOST COMMAND
;
RESET  GOTO  1FH ;MIRROR TRIS
;
ORG  00H
;
SUBROUTINES
;
;H168-Speed Service FOR Battery
;
HS_SERVA MOVLB  08H  ;LOAD BIT COUNTER
MOVFW  HSERBIT  ;WITH 8 FOR 8 BITS
READIT CLRWF WSTACK  ;GET TIMEOUT READY
CLRF  TIMEOUT
HABQ0 MOVWF PORTB,0  ;REQUEST FOR HS
GOTO  HABQ1
DECFSZ WSTACK,1  ;COUNT FOR TIMEOUT
GOTO  HABQ0
;
;TIME-OUT ON RECEIVE
;
MOVLB  0FFH
MOVWF  TIMEOUT
GOTO  BREAKIT
;
HABQ1 RF  HSERDAT,1  ;SHIFT DATA
CLRF  WSTACK  ;TIME LOW TIME
HABQ2 BTSSL PORTB,0  ;CHECK FOR STOP BIT
GOTO  HABQ3
incf  WSTACK,1
BTSSL  WSTACK,6  ;BREAK DURING READ LOW 144us
GOTO  HABQ2
;
;BREAK DETECTED
;
BREAKIT CLRWF HCMD  ;CANCEL PENDING COMMAND
MOVLB  08H  ;LOAD BIT COUNTER
MOVWF  HSERBIT  ;WITH 8 FOR 8 BITS
HABQ5 MOVWF PORTB,0  ;CHECK FOR STOP BIT
GOTO  HABQ6
RETlw  00H  ;DONE
;
HABQ3 BCF  HSERDAT,7
MOVLB  30H
ANDWF WSTACK,W
BTSSL STATUS,2
BCF  HSERDAT,7
DECFSZ HSERBIT,1
GOTO  READIT  ;MORE TO DO!
;
MOVF  HSERDAT,W
MOVWF  HCMD
DONE_WA MOVLB  08H
MOVWF  HSERBIT  ;WITH 8 FOR 8 BITS
RETlw  00H
;
;Shda IT will Send ONE Byte TO HDQ Module
;
Shda _IT MOVLB  08H  ;LOAD BIT COUNTER
MOVWF  HSERBIT  ;WITH 8 FOR 8 BITS
;
;DELAY A BIT
;
CLRF  HCMD
```
Microcode Example for HDQ Interface (continued)

```
SNDA_1  ZNCy  HCMO, 1
BTFSS HCMO, 6
GOTo  SNDA_1
;
SNDA_2  BCF  BTRIS, 0
MOVf  BTRIS,W
TRIS  PORTB
CLRF  HCMO
;
SNDA_3  ZNCy  HCMO, 1
BTFSS HCMO, 4
GOTo  SNDA_3
;
SNDA_5  BTFSS HSERDAT, 0  ;TEST DATA BIT
GOTo  SNDA_4
;
SF  BTRIS, 0
MOVf  BTRIS,W
TRIS  PORTB
;
SNDA_4  CLRF  HCMO
;
SNDA_7  ZNCy  HCMO, 1
BTFSS HCMO, 5
GOTo  SNDA_7
;
SF  BTRIS, 0
MOVf  BTRIS,W
TRIS  PORTB
;
CLRF  HCMO
SF  HCMO, 4
;
SNDA_9  ZNCy  HCMO, 1
BTFSS HCMO, 6
GOTo  SNDA_9
;
BSF  HSERDAT, 1  ;SHIFT DATA, FOR NEXT BIT
DECFsz  HSERBIT, 1  ;DEC COUNTER
GOTo  SNDA_2  ;MORE BITS TO SEND
;
CLRF  HCMO
MOVlw  08h  ;LOAD BIT COUNTER
MOVwf  HSERBIT  ;WITH 8 FOR 8 BIT
RETlw  00h  ;NO, DONE
;
INITIALIZATION
;
BEGIN  CLRWUT
MOVlw  06h
OPTION
CLRW  PORTB
MOVWF  PORTB
MOVlw  03h
MOVWF  BTRIS
TRIS  PORTB
MOVlw  08h
MOVWF  HSERBIT  ;WITH 8 FOR 8 BIT
;
OTHER USER CODE
;
READ EXAMPLE
;
READ SCR
;
MOVlw  03h
MOVWF  HSERDAT
CALL  SNDA_5
CALL  HSERVA
;
HSERDAT= null
;
WRITE EXAMPLE
;
WRITE RAM = 64AA
;
MOVlw  83h
MOVWF  HSERDAT
CALL  SNDA_5
MOVlw  64AA
MOVwf  HSERDAT
CALL  SNDA_5
;
OTHER USER CODE
;
GOTo  RESet
;
END
```
Figure 3. bq2018 Schematic

Notes:
- C1—bypass for $V_{CC}$
- C2, C3, R2, R3—bypass for SR
- D2, R6; D1, R5—ESD protection
- D3, R4—Isolation for RB1 cell connection
- C5—bypass for REG
- R1—sense resistor
Interfacing to a Microcontroller

A microcontroller can interface the bq2018 using a general purpose I/O port. The WAKE output of the bq2018 interrupts the microcontroller when it detects charge or discharge activity greater than a programmable level. HDQ and WAKE are open-drain and require a pull-up resistor as shown.

Microcontroller Software

A microcontroller must configure the bq2018 and read and format its counter data to implement a battery capacity monitor. There are three main aspects of the software: Factory Configuration Program, Operating Program, and Serial Communication Program.

Factory Configuration Program (Test System Microcontroller)

The factory program configures a bq2018 based intelligent battery pack for operation. Actual battery monitor information, such as remaining capacity, compensation rates, and status flags may be stored in the bq2018 user RAM. The factory program initializes the user RAM and the bq2018. The battery maintains the bq2018 data with a low backup current of < 0.1\( \mu \)A.

Operating Program (Host System Microcontroller)

The Operating program loop reads the bq2018 and updates the RAM locations for charge/discharge use conditions. The microcontroller periodically applies self-discharge and offset correction and calibrates remaining capacity and the full-charge reference based on state-of-charge and battery voltage.

Notes:
1. Requires A-to-D converter.
2. Typical loop time is once per minute.

Serial Communication Program (Test and Host Microcontroller)

The Designed to GO insert shows an example of the microcode required to communicate with the bq2018 using a port pin of a microcontroller. The code is for a PIC16C5X running at 8.0MHz.

Note: 1. Write default values to RAM if necessary.

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