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A Power Management Interface Circuit for Telecom Hot Swap with Local DC/DC Conversion

Andrew Ripanti *Power Distribution and Processing Solutions*

ABSTRACT

Much of the Telecom and Datacom equipment infrastructure operates from a power architecture based on a –48 Vdc distribution bus. This supply level has emerged as a standard and efficient means of distributing power throughout equipment racks, while facilitating alternate source operation from secondary power, such as batteries, when the AC line supply is unavailable. To further improve uptime ratios while meeting the needs of maintenance and reconfiguration, *hot swap* capability is often incorporated in removable subassembly specification and design.

Today, the brains of these communication systems; i.e., microprocessors, DSPs, ASICs, and programmable logic, are evolving to ever-lower operating voltages. Typical integrated circuits run at supply levels of 3.3 V, 2.5 V, and even lower. As this occurs, new devices and modules are being developed to address the functions of *hot-swapping* the –48 Vdc bus, and subsequent conversion to local regulation levels. These devices provide a high level of integration for the point-of-use power supplies, saving the system designer both design time and critical board space.

This application report presents one possible solution to the telecom plug-in power problem, based on a nominal –48 Vdc system bus and a module needing two low-voltage supply outputs. The material includes a detailed design methodology for tailoring the circuit to the specific requirements of the reader's system. The solution is based on two device families offered by Texas Instruments, the UCC3913 and UCC3921 hot swap power manager ICs, and the PT3320 series of integrated switching regulators (ISRs).

The document organization is such that some example system requirements are defined, then a step-by-step procedure is presented for determining external component values to set user-programmable features. There is discussion of some optional features. Finally, the circuit operation and performance is further illustrated through scope plots of the circuit's response to various live insertion events, and input and output fault conditions.

CONTENTS

1 Introduction

1.1 The Power Transmission Problem

Many telecom and datacom systems are configured from subsystem racks and chassis, or boxes, each containing a system host or controller card, one or more power supplies, and various sub-assembly cards performing functions of data processing, data transmission and switching. The interconnect between the different modules is often accomplished with a backplane or motherboard. Power is commonly provided to the various module slots via a –48 Vdc distribution bus. This is an efficient means of supplying power throughout the box for two main reasons:

1. Current bussing requirements are significantly reduced compared to the current levels that would be encountered if power were distributed at the regulation levels of 5.0 V, 3.3 V, or even lower, and
2. System supply voltage droops and spikes of several volts are more easily tolerated by the driven electronics, as significant voltage margin now exists between the power bus and the regulation levels.

This configuration, however, creates the need for efficient and cost-effective voltage conversion to the local regulation levels at the points-of-use.

The power conversion issue is further complicated when the driven boards are specified to have *hot swap* or *hot plug* capability. Simply put, *hot swap* is the ability to safely insert a module into or remove it from a host system, without first interrupting power to the host. This feature is generally designed in wherever there is a need to replace modules on-the-fly. Such a requirement may be for purposes of repair, reconfiguration, redundancy, or system upgrade. It is also useful in systems with high availability requirements (i.e., high up-time ratios). Finally, hot swap requirements may be included in the target industry specification that is being designed to, such as PCI, Compact PCI, USB, and 1394. Not surprisingly, it has seen significant use in telecom systems.

As a highly desirable feature in many applications, hot swap capability also creates several issues that must be addressed in the system design. A number of related phenomena occur with a live insertion or removal event, including contact bounce, arcing between connector pins, and large voltage and current transients. The stresses on the mechanical interface, power supply, and input filter components can produce latent defects leading to intermittent or premature failures. Therefore, a power interface is needed which can safely mitigate these effects. This interface provides protection for both the host and plug-in electronics, data stored or transferred in the system, and any transactions within or between systems.

This application note presents one possible solution for hot swapping a –48-Vdc bus, and performing the required DC/DC conversion. The organization is such that the operating parameters are defined, a top–level electrical schematic presented, followed by a detailed procedure for determining component values, description of some optional features, and performance verification.

The proposed solution is built around two main device types offered by Texas Instruments (TI). The UCC3921 Hot Swap Power Manager (HSPM) integrated circuit handles the main functions needed for hot swap capability; the conversion is performed using the PT3320 series of integrated switching regulators (ISRs).

The UCC3921 IC is a floating, negative-voltage hot-swap controller which, in conjunction with an external N-channel FET, provides inrush current limiting, fault timeout, and fault reporting. An on-chip shunt regulator generates the internal supply voltages and the gate drive for the external pass element. Other features include continuous supply current monitoring with electronic circuit breaker, remote enable, and user–programmable duty cycle to limit dissipation in the FET in automatic retry mode. For a complete description of the UCC3921 features and operation, please refer to the device data sheet.

The PT3320 is a series of 30-W, isolated DC/DC converter modules designed specifically for 48-V distribution systems. They are complete modules assembled onto a space-saving, PCB-based, vertical- or horizontal-mount SIP package. A wide range of output voltage/current combinations is available from 2 V to 15 V (see Table 1). A wide input voltage operating range (36.0 V to 75.0 V) and high efficiencies make them applicable in numerous distributed power applications. The converters contain an external inhibit function, and remote sense inputs to compensate for any voltage drop from converter output to load. The only external component required for operation is a 330-μF electrolytic capacitor. For further information on the full range of 48-V converter products, including the 3-W to 7-W PT4200/4300 and 15-W PT3100 series modules, please visit **www.ti.com**.

Table 1. PT3320 Series of Converters

DEVICE NUMBER	OUTPUT	
	VOLTAGE (V)	CURRENT (A)
PT3321	3.3	8
PT3322	5.0	6
PT3323	12.0	2.5
PT3324	15.0	2
PT3325	2.0	8
PT3326	2.5	8
PT3327	1.8	8
PT3328	5.2	6

1.2 Design Requirements

To illustrate the detailed design steps for using the UCC3921 in a –48 V (or Telecom) system, the following system-level requirements were defined:

- Input supply voltage: nominal –48 Vdc, –36 Vdc (min) to –72 Vdc (max)
- Output voltage/current: 1.8 Vdc at 6.0 A (max), and 2.5 Vdc at 6.0 A (max)
- Isolated outputs
- Redundant supply operation (2 sources)
- Hot-swap capability
- Interface to host ENABLE signal
- Fault indication to host
- 0°C to 70°C ambient operating temperature
- Host V_{DD} supply: 3.3 Vdc

2 The Power Management Interface

2.1 Electrical Schematic Diagram

The electrical schematic for one type of implementation of the power interface specified in the design requirements is shown in Figure 1. Some of the secondary functions are shown here in block form for later discussion. The output voltages are generated from the –48-Vdc input via the PT3326 (2.5 V) and PT3325 (1.8 V) modules[1]. The PT3320 modules are fully isolated, thus eliminating the need for additional transformers. The UCC3921 HSPM resides between the input supply and the VIN pins of the converters. It drives N-channel FET Q1, which switches the low side of the supply (–48 V). The SNS input of the IC monitors the voltage drop across sense resistor R5, so the current load on the 48 V supply is monitored.

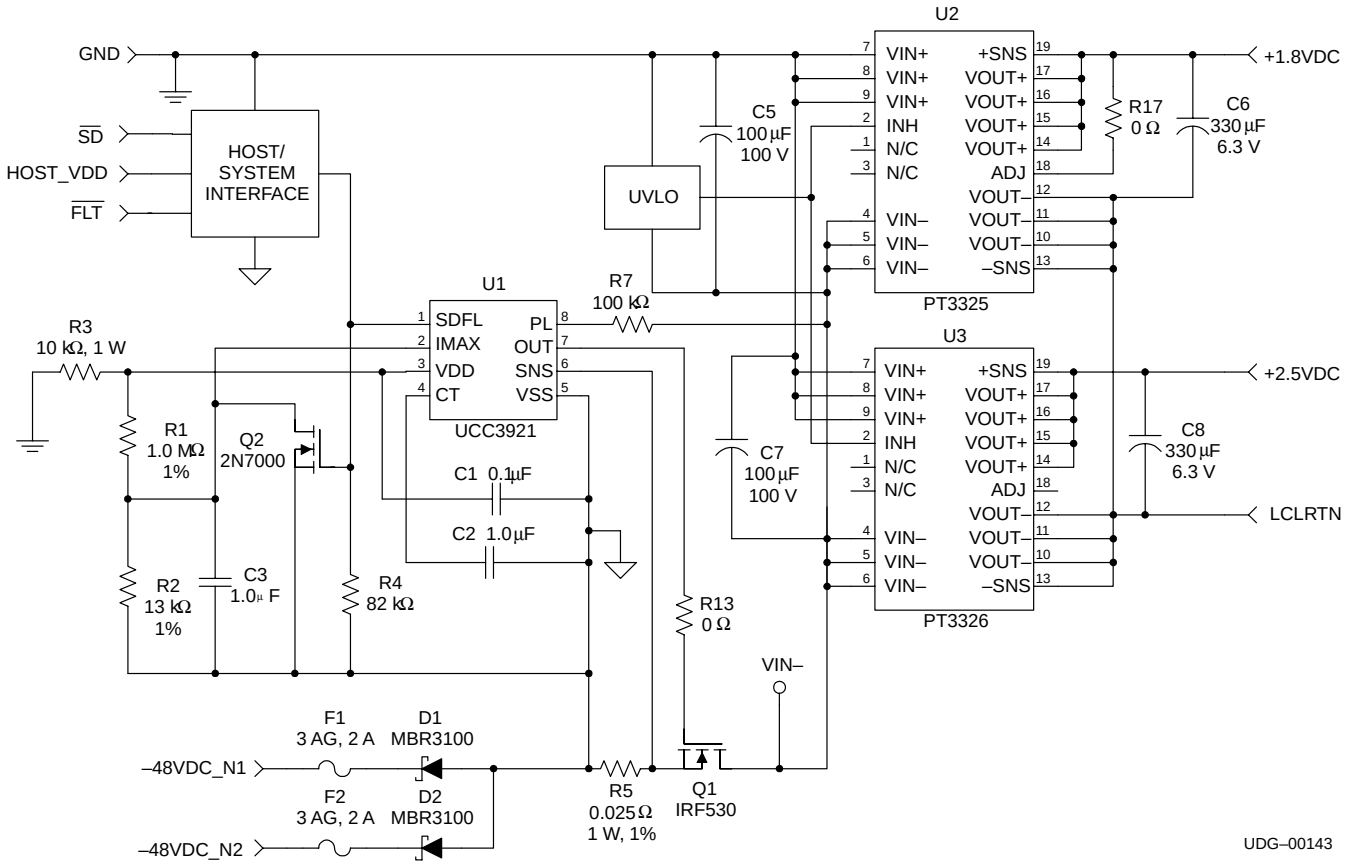

Figure 1. Top-Level Schematic Diagram for –48 Vdc Hot Swap with DC/DC Conversion

Table 2. Hot Swap Power Circuit Signal Descriptions

SIGNAL NAME	DESCRIPTION
–48VDC_N1	–48-Vdc input supply no. 1 to the plug-in PCB.
–48VDC_N2	–48-Vdc input supply no. 2 to the plug-in PCB.
GND	Supply common for the two –48 Vdc supplies. This is also intended as the system ground node.
HOST_VDD	Host or controller V_{DD} node, +3.3 V dc.
$\overline{SD}$	Active low SHUTDOWN input for remote or host control of the module ON/OFF status.
$\overline{FLT}$	Active low FAULT output to the system.
+1.8VDC	+1.8 V dc power supply output.
+2.5VDC	+2.5 V dc power supply output.
LCLRTN	Common local return for the two output supply rails.

2.2 Detailed Circuit Description

The UCC3921 device determines load current levels by monitoring the voltage drop across a low-ohmic value sense resistor, R5, as shown in Figure 1. The device has two distinct current thresholds for defining different modes of operation. The first threshold is the fault current, referred to herein as I_{FLT}. This can be thought of as the circuit breaker trip current. When enabled, and under normal load conditions below the fault current threshold, the UCC3921 OUT pin drives external FET Q1 gate with a nominal 9.5-V source, relative to the VSS node. Q1 is switched on, and completes the low impedance return path from the load (VIN– pins of the ISR's). When the device detects a nominal drop of 50 mV or greater between the SNS and VSS pins, an internal source begins charging an external capacitor connected to the CT pin, essentially generating a time delay before tripping, or opening the supply return path by turning off transistor Q1. However, during this timeout period, the pass FET is still driven as a low–ohmic value switch. If the fault condition is removed prior to timeout, the capacitor is discharged, and supply operation continues uninterrupted.

The second threshold is the maximum current that will be sourced to the load by the HSPM circuit, or IMAX. Under heavy overcurrent or short-circuit conditions, the input current to the converter circuit will be clamped at this maximum level. During a live PCB insertion, inrush current caused by charging bulk capacitance (C5 and C7 in Figure 1) will also be limited to this level. The threshold is programmable by using a resistor divider to set the voltage at the U1 IMAX pin. The VDD node provides a ready reference for this divider. In the Figure 1 schematic, this threshold is set by the R1/R2 resistor network.

Since the UCC3921 is a current-driven device, it essentially floats from the positive supply input. Resistor R3 sets the biasing supply level for the VDD input. Capacitor C1 provides supply bypassing for U1, and C2, tied to the CT pin, is the timing capacitor. Resistor R7 is an optional component used by the UCC3921 to further limit power dissipation in the pass element, under certain fault conditions, below the limits that are automatically provided by the IC.

The detailed procedure for determining component values for the hot swap interface will be shown in Section 2.3, *Circuit Design Procedure*. For a complete description of the HSPM IC operation and electrical specifications, see the UCC3921 device data sheet.

Capacitors C6 and C8 provide the energy storage capability required for proper operation of the PT3320 switcher modules, U2 and U3 respectively. They also provide some output filtering for the DC/DC converters. The 330-µF value used is the manufacturer's recommended value. The input capacitors C5 and C7 are used to ensure good power quality to the ISRs.

Diodes D1 and D2 provide a diode–OR function between the two redundant supply nodes (–48VDC_N1 and –48VDC_N2). If only one supply is present, or if one supply has failed, supply return is still provided by the alternate path. Note that Schottky diodes are used; at least one of these devices is always conducting, so Schottkys are used to minimize the reduction in overall efficiency of the interface.

Fuses F1 and F2 provide a one-shot over-current protection in the event of catastrophic failure of the more intelligent protection devices downstream. The PT3320 ISRs feature output short-circuit protection. The UCC3921 features both a programmable current limit, and circuit breaker operation. These provide redundancy to the output protection, and protect against an overcurrent or short-circuit on the primary (VIN) side. Should these devices fail in the right combination, fuses F1 and/or F2 provide a permanent, mechanical interrupt.

The block labeled *HOST/SYSTEM INTERFACE* in Figure 1 is an optional sub-circuit to allow remote ON/OFF control of the plug-in module, and generate a current fault indication back to the host. This block provides the level-translation needed to refer the multifunctional SDFL pin of the UCC3921 to the system common, or GND node. If these features are not needed, implementation of this circuit is not necessary.

The block labeled *UVLO* provides an optional undervoltage lockout (UVLO) function to the startup of the two DC/DC converters. However, the PT3320 regulators incorporate an internal UVLO circuit, the threshold of which is specified to be 33 ±2.0 Vdc. Since the design specification requires this circuit to operate down to a –36-V supply level, and the maximum ISR UVLO level is just below this voltage, this solution was developed assuming the internal UVLO is to be used. To address a wider range of application requirements, an alternative implementation of an external UVLO circuit is shown in Section 3.3, *Optional UVLO Circuit.*

2.3 Circuit Design Procedure

The following is a sequence of design steps that can be used to determine component values for the configuration circuitry around the hot-swap controller IC. The process takes into consideration the load characteristics, both during startup and under dc operating conditions, and the device parameter specifications. To assist the reader in determining the source and value of the UCC3921-specific variables plugged into the following equations, Appendix I summarizes the key device parameters.

2.3.1 Step 1 – Determine Input Load Current

In order to set the fault levels for the HSPM IC, the nominal load current on the input supply must be estimated. Given the operating loads on the two regulated outputs from the design specification, the converter efficiency can be used to estimate the average load on the primary (bus) side. Also, since the PT3320 modules are switching regulators, the peak load is anticipated to occur when the bus potential is at its lowest.

From the PT3321 curves shown in the data sheet[2], the efficiency at 6 A for input voltage of 36 V is nearly 80%, decreasing to about 75% at 75 V. Power delivered to the loads, P_{OUT}, and subsequently input current to the board, I_{IN}, are estimated from the following equations.

$$P_{OUT} = P_{O1} + P_{O2} = \left(V_{O1} \times I_{LOAD1}\right) + \left(V_{O2} \times I_{LOAD2}\right) \quad (1)$$

where:

- V_{O1} = local regulation level No. 1, +2.5VDC
- I_{LOAD1} = maximum output load on V_{O1}
- V_{O2} = local regulation level No. 2, +1.8VDC
- I_{LOAD2} = maximum output load on V_{O2}

The input supply current under normal steady-state operation, I_{IN}, can then be estimated from:

$$I_{IN} = \frac{P_{IN}}{V_{IN}} = \frac{\frac{P_{O1}}{\eta_1} + \frac{P_{O2}}{\eta_2}}{V_{IN}} \quad (2)$$

$$I_{IN} = \frac{V_{O1} \times I_{LOAD1}}{\eta_1 \times V_{IN}} + \frac{V_{O2} \times I_{LOAD2}}{\eta_2 \times V_{IN}} \quad (3)$$

where:

- P_{IN} = input power delivered to the board
- η_1, η_2 = respective converter efficiencies for outputs 1 and 2
- V_{IN} = the input supply voltage level

For reasons detailed in *Section 2.3.5*, the designer must determine the maximum input current at each of the input voltage extremes. Therefore, two maximum current levels need to be calculated. Defining $I_{IN(max)}$ as the supply current when the bus is at its lowest potential, and $I_{IN(max')}$ as the supply current when the bus is at its highest potential, then substituting the values from the requirements specification, the input current levels shown in equations 4 and 5 are obtained. Note that equations 4 and 5 are a simplification of equation 3 when the converters are anticipated to be operating at virtually equivalent efficiency points.

$$I_{IN(max)} = \frac{\left(V_{O1} \times I_{LOAD1}\right) + \left(V_{O2} \times I_{LOAD2}\right)}{\eta_{36} \times V_{IN(min)}} \quad (4)$$

$$I_{IN(max)} = \frac{[(2.5\ V \times 6.0\ A) + (1.8\ V \times 6.0\ A)]}{(0.8 \times 36\ V)}$$

or

$$I_{IN(max)} = 0.896\ A$$

and

$$I_{IN(max')} = \frac{\left(V_{O1} \times I_{LOAD1}\right) + \left(V_{O2} \times I_{LOAD2}\right)}{\eta_{75} \times V_{IN(max)}} \quad (5)$$

$$I_{IN(max')} = \frac{[(2.5\ V \times 6.0\ A) + (1.8\ V \times 6.0\ A)]}{(0.75 \times 72\ V)}$$

or

$$I_{IN(max')} = 0.478\ A$$

These estimates were made considering the dc or average-output currents. For the PT3320 series, the input ripple current is typically less than 0.25 A peak. This is added to the average values to get an approximation of the peak input current under normal operating conditions, to ensure that the HSPM does not trigger due to expected input ripple. The results (rounded to the nearest 10 mA) are:

$I_{IN(max)} \cong 1.15$ A

$I_{IN(max')} \cong 0.730$ A

2.3.2 Step 2 – Set Fault Current Level And Determine Sense Resistor Value

The fault current level for the hot swap interface circuit must be selected. This is established by the value of the sense resistor, R5 in the Figure 1 schematic. Since the nominal overcurrent threshold of the UCC3921 is 50 mV, the resistor value can be determined from equation 6.

$$R5 = \frac{V_{FLT}}{I_{FLT}} = \frac{50\ mV}{2.0\ A} = 25\ m\Omega \quad (6)$$

Selecting a nominal fault threshold of 2.0 A provides nearly 100% margin over the anticipated peak operating levels. Some design margin is desirable to provide headroom for any transient peaks on the output supplies, tolerances on the converter efficiency from unit-to-unit, transients on the –48-V supply bus that cause surges in input current, and as an overall guard against nuisance trips. Using the UCC3921 specification values for the overcurrent threshold, and with the sense resistor value fixed, the minimum and maximum current fault levels can be verified using equations 7 and 8.

$$I_{FLT(min)} = \frac{V_{FLT(min)}}{R5} = 1.84\ A \quad (7)$$

$$I_{FLT(max)} = \frac{V_{FLT(max)}}{R5} = 2.14\ A \quad (8)$$

where :

- $V_{FLT(min)}$ = minimum fault (overcurrent) threshold
- $V_{FLT(max)}$ = maximum fault threshold

The calculated minimum value, 1.84 A, demonstrates that significant margin is available even with a device at the low end of its specification limit.

2.3.3 Step 3 – Set IMAX Threshold And Determine IMAX Divider Values

The maximum sourcing current level of the hot swap circuit, herein referred to as IMAX, is user programmable, using the IMAX input pin of U1. In an effort to predict performance under worst-case parameter conditions, it is recommended to establish the *lower* threshold for this maximum sourcing capability, or $IMAX_{MIN}$. Generally, this will correspond to the IMAX level for a device with a regulator output (VDD) at the specification minimum voltage, taking into account two other sources of variance, the input offset voltage and bias current of the internal linear current amplifier (LCA). For proper device operation, this value should be greater than the calculated maximum fault current, $I_{FLT(max)}$. If a relatively fast rate of input current slewing is allowed, or a large amount of bulk capacitance exists at the input to the plug-in, the IMAX feature can be used to accomplish faster charging of the load capacitance, thus minimizing the startup transient duration. However, if the distribution supply has a slow transient response, minimal output capacitance, or is required to operate near peak capability at the expected system steady-state load, the IMAX level should be selected with these limitations in mind. In addition, under a short-circuit situation, the load current of the affected module(s) will make a step change to this level. For this example, a minimum sourcing level of 4.0 A is used.

Figure 2 is a simplified model of the UCC3921 operation when the sense voltage, V_{SNS}, is above the IMAX threshold. During inrush or short-circuit conditions, the HSPM device acts to control the gate of Q1 such that it appears as a constant-current source. The internal LCA will respond to maintain the V_{SNS} node equal to the IMAX reference, (i.e., the drop across the sense resistor equal to the drop across R2.) Therefore, an equation for the sense voltage is generated by writing the loop equation at the linear current amplifier (LCA) inputs (equation 9).

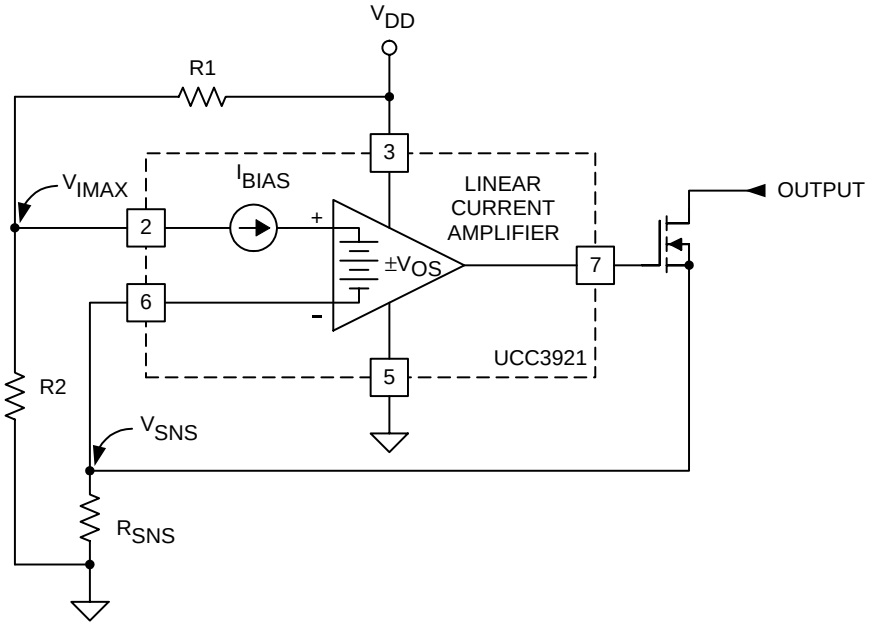

Figure 2. Model of UCC3921 Linear-Mode Operation

$$V_{SNS} = V_{IMAX} - V_{BIAS} \pm V_{OS} \quad (9)$$

where:

- V_{SNS} = the drop across the sense element
- V_{IMAX} = the voltage at the 3921 IMAX input pin
- V_{BIAS} = the error component developed by the IMAX bias current
- V_{OS} = the input offset of the internal LCA

Also from Figure 2, the V_{IMAX} DC voltage is given by the R1/R2 divider equation.

$$V_{IMAX} = \frac{R2}{R1 + R2} \times V_{REF} \quad (10)$$

where:

- V_{REF} = the internal shunt regulator output, V_{DD}

Considering that the bias current flow is into the IMAX pin, the smallest error contribution occurs for a device with negligible bias current, which is approximated here to zero. Then, a special case of equation 9 for the minimum sense voltage in linear mode, is given by equation 11.

$$V_{SNS(min)} = V_{IMAX(min)} - V_{OS} \quad (11)$$

Given that $V_{SNS(min)} = IMAX_{MIN} \times R5$, combining equations 10 and 11, and solving for R2 in terms of R1, yields:

$$R2 = \frac{\left(IMAX_{MIN} \times R5\right) + V_{OS}}{\left[V_{REF(min)} - \left(IMAX_{MIN} \times R5\right) - V_{OS}\right]} \times R1 \quad (12)$$

The value for R1 can be set to limit the overall current draw of the divider net; if R1 is set to 1 MΩ, equation 12 then becomes:

$$R2 = \frac{(4.0 \times 0.025) + 15\ mV}{[9.0 - (4.0 \times 0.025) - 15\ mV]} \times 1.0\ M\Omega \quad (13)$$

or

$$R2 = 12.94\ k\Omega$$

The standard 1% value of 13 kΩ was selected for R2.

With values now selected for resistors R1 and R2, the actual minimum and maximum sourcing current levels is predictable. These values are useful for determining the startup time (ramp-up from 0 V to the dc input level) under different conditions. Equations 14 and 15 are obtained by manipulating equation 12. For the $IMAX_{MAX}$ value, the error contribution from the bias current is included.

$$IMAX_{MIN} = \frac{\left[\frac{R2}{R1+R2} \times V_{REF(min)}\right] - V_{OS}}{R5} = 4.02\ A \tag{14}$$

$$IMAX_{MAX} = \frac{\left[\frac{R2}{R1+R2} \times V_{REF(max)}\right] + V_{OS} + V_{BIAS}}{R5} = 6.07\ A \tag{15}$$

2.3.4 Step 4 – Soft-Start Programming

The UCC3921 is easily configured for optional soft-start operation. Without soft-start, when a plug-in is inserted into a live socket, the resultant inrush makes a step change to the IMAX limit, where it becomes clamped for the duration of the transient period. Soft-start operation provides an inrush slew rate control, such that the load charging current is gradually ramped, potentially to the maximum value established by the IMAX pin programming resistors.

Soft-start is selectable by installing a capacitor in parallel with the IMAX programming resistor (shown in Figure 1 as capacitor C3.) The feature operates by putting an RC time constant on the voltage ramp at the IMAX pin when the power manager is started. This forces the device to operate in linear mode immediately from Q1 turnon, essentially producing a dynamic IMAX function.

For a UVLO-protected load, such as presented by the two ISRs in this solution, the startup voltage ramp to the converter inputs will have two stages. During the first stage of rampup, from turnon until achieving the UVLO threshold, the load appears virtually capacitive to the charging source. This capacitance, C_{LOAD}, is the equivalent capacitance of the input filter capacitors, the converter input capacitance, and any parasitics. Wherever this quantity is used in this document to derive other values, it is approximated as the 200-μF value of C5 and C7.

For a constant-current source of value IMAX (i.e., no soft-start), the voltage at the converter inputs during this stage, for a charging time of t, is given by equation 16.

$$v_{INU1}(t) = \frac{IMAX \times t}{C_{LOAD}} \tag{16}$$

Once the load charges to the UVLO threshold, V_{UV}, the ISRs are allowed to start up. During this second stage of the voltage ramp, the load capacitance is charged by the sourcing current in excess of the ISR startup load, $i_L(t)$. This portion of the ramp-up curve is given by:

$$v_{INA1}(t) = \frac{\left[\left(IMAX - i_L(t)\right) \times \left(t - t_{VUV}\right)\right]}{C_{LOAD}} + V_{UV} \tag{17}$$

where:

- $i_L(t)$ = load startup current
- V_{UV} = the UVLO threshold voltage
- t_{VUV} = the time to charge the input from 0 V to V_{UV}, from equation 16

When soft-start programming is used, both the input voltage and current waveforms are of interest. Due to the control action of the U1 LCA described above in step 3, we know that the sense voltage tracks the R2 voltage during rampup, which is now the voltage across capacitor C3. Since the output current of the HSPM circuit can be determined from the drop across R5, the following equation for input current to the load is derived:

$$i_{IN}(t) = IMAX \times \left[1 - e^{\left(\frac{-t}{\Im_{SS}}\right)}\right] \tag{18}$$

where:

- $i_{IN}(t)$ = the charging load on the –48-Vdc supply
- $\Im_{SS}$ = the soft-start time constant, given by $\Im_{SS} = R2 \times C3$, in seconds.

Since the capacitor charging current is given by equation 18 under this condition, the input voltage profile has an exponential term also. The first stage of the input rampup, prior to startup of the ISRs, is defined by equation 19.

$$v_{INU}(t) = \frac{\Im_{SS} \times IMAX}{C_{LOAD}} \times \left[e^{\left(\frac{-t}{\Im_{SS}}\right)} + \frac{t}{\Im_{SS}} - 1\right] \tag{19}$$

where:

- $\Im_{SS}$ = the soft-start time constant

Different criteria may be used for establishing the target slew rate of the hot swap circuit on powerup. However, one overriding requirement is that the input current must be allowed to attain a minimum value prior to the voltage across the input capacitance achieving the UVLO threshold. This minimum level is the current that is demanded by the load. In this case, it is the startup current of the two converters. If the minimum current is not obtained, the active load will begin discharging the input capacitance (C5 and C7 in this case). Some amount of voltage droop may be tolerated by the load, but that is dictated by the complexity and hysteresis of the UVLO circuitry. As a general guideline, be sure to provide sufficient current to avoid any voltage droop. This target current, or *set* current, is referred to as I_{SET} in the following paragraphs.

To simplify what easily becomes a complicated math exercise, assume that the load startup current is constant, or $i_L(t) = I_L$. To further simplify, assume that this constant value is in fact the value previously calculated for the peak operating current, or $I_{IN(max)}$. For this example, the minimum current required at load startup, I_{SET}, is set to 5% over this value, or

$$I_{SET} = 1.05 \times I_{IN(max)} = 1.208 \text{ A} \tag{20}$$

Given the voltage ramp profile of equation 19, what is the value of C3 which will ramp the input current to at least I_{SET} by the time the voltage reaches the UVLO threshold? By solving equation 18 for the time t when $i_{IN}(t) = I_{SET}$, plugging this expression into Eq. 19, and solving for the C3 term, equation 21 is derived.

$$C3 = \frac{-V_{UV}}{\left[\left(\frac{R2}{C_{LOAD}}\right) \times \left(I_{SET} + IMAX \times \ell n\left(1 - \frac{I_{SET}}{IMAX}\right)\right)\right]} \quad (21)$$

Examination of equation 18 reveals that the slowest current ramp occurs under minimum sourcing conditions. Substituting $IMAX_{MIN}$ for IMAX in equation 21, and using the minimum specified UVLO threshold (31 V), yields C3 = 2.09 μF. Because of the criteria used to establish equation 21, the 2.09-μF value represents essentially the maximum size capacitor that should be used in this solution.

To demonstrate an alternative, assume that a maximum slew rate requirement of 0.5 A per msec is included in the design specification. The value of the soft-start capacitor, C3, for a given slew rate can be found by taking the derivative of the input current during the startup voltage ramp, given by equation 18. The result is equation 22 .

$$\frac{di}{dt} = \frac{IMAX}{\mathcal{T}_{SS}} \times e^{\left(\frac{-t}{\mathcal{T}_{SS}}\right)} \quad (22)$$

Setting di/dt for t = 0 to the maximum slew rate spec, and substituting $IMAX_{MAX}$ for IMAX yields:

$$C3 = \frac{IMAX_{MAX}}{\left(R2 \times (di/dt)_{MAX}\right)} = 0.934\ \mu F \quad (23)$$

As shown in the schematic, a value of 1.0 μF was used.

2.3.5 Step 5 – Estimating Ramp TIme

The minimum delay to a fault timeout must be long enough to allow charging of the input capacitance at startup. Therefore, an estimate of the total voltage ramp time at module startup is needed. An empirical approach can be taken by bench-testing the interface circuit with the load connected, and measuring the time for the converter input voltage to ramp to the DC input potential. To do this, the fault timer can be defeated by temporarily installing a resistor with a value ≤1 kΩ in place of capacitor C2. Alternatively, the analysis detailed in this section can be used to better predict the worst-case timing.

For the analysis, two possible scenarios exist.

1. Either soft-start is not used, or soft-start reset switch Q2 is not used. For this case, the output voltage equations 16 and 17 apply.
2. Output soft-start is used. The required delay is given by the t_{CTSS} calculation shown in the discussion after Figure 5.

   For case 1, the HSPM IC operates in fault mode immediately from turn-on, and the minimum delay needed is the total start time. This is given by equations 24 and 25.

$$t_{CT} = t_{ST1X} = \frac{C_{LOAD} \times \left(\nu_{INA1}(t) - V_{UV}\right)}{IMAX_{MIN} - I_L} + t_{VUVX} \quad (24)$$

where:

$$t_{VUVX} = \frac{C_{LOAD} \times \left(V_{UV} - 0\right)}{IMAX_{MIN}} \quad (25)$$

Solve t_{CT} for $V_{INA1}(t) = V_{IN(max)}$ and $V_{UV} = V_{UV(min)}$.

For case 2, soft-start, equation 19 determines the time required to reach the UVLO threshold, designated here as t_{VUV}. Through repeated sampling of the voltage equation, the following values were determined:

- t_{VUVX} = 6.89 ms, the time for $V_{IN}(t)$ to reach V_{UV} when IMAX = $IMAX_{MIN}$
- t_{VUVM} = 5.51 ms, the time for $V_{IN}(t)$ to reach V_{UV} when IMAX = $IMAX_{MAX}$

To approximate the worst case startup time, the minimum UVLO threshold of the converters, 31 V, was used as the target voltage level. Due to the tedious nature of sampling the voltage waveforms at different times, it may be useful to create a spreadsheet or use some other software tool to generate a table of values while sweeping the time variable.

At time t = t_{VUV}, the load starts up. This defines the transition point between the two equations for the input profile. The second stage of the ramp-up, from $V_{IN}(t) = V_{UV}$ to the dc input level, is given by:

$$\nu_{INA}(t) = \left[\frac{\mathcal{T}_{SS}}{C_{LOAD}}\right] \times \quad (26)$$

$$\left[\left[IMAX \times e^{\left(\frac{-t}{\mathcal{T}_{SS}}\right)} + \frac{\left(IMAX - i_L(t)\right) \times t}{\mathcal{T}_{SS}}\right] - \left[IMAX \times e^{\left(\frac{-t_{VUV}}{\mathcal{T}_{SS}}\right)} + \frac{\left(IMAX - i_L(t)\right) \times t_{VUV}}{\mathcal{T}_{SS}}\right]\right] +$$

$$\nu_{INU}\left(t_{VUV}\right)$$

Figures 3 through 5 show a graphic representation of the input current and voltage waveforms during the transient ramp-up. Plots were produced for sourcing current limit, IMAX, at the nominal, minimum and maximum levels.

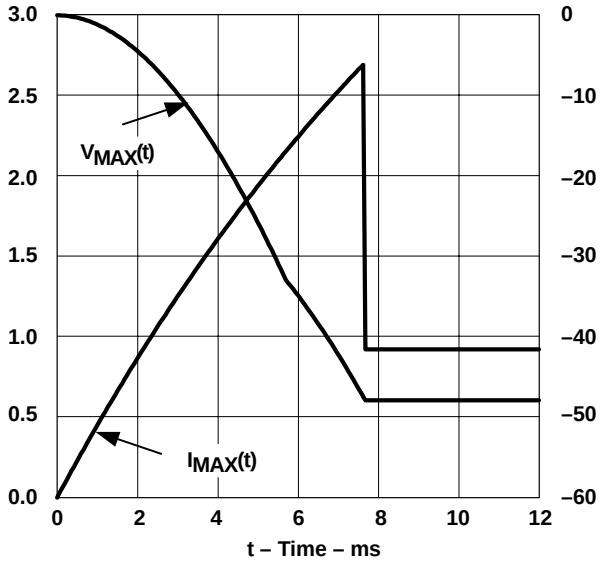

Figure 3. ISR Input Voltage and Current – $IMAX_{MAX}$ Condition

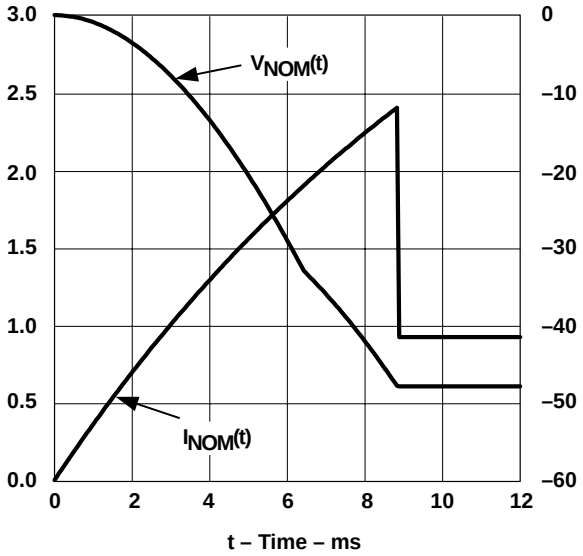

Figure 4. ISR Input Voltage and Current – $IMAX_{NOM}$ Condition

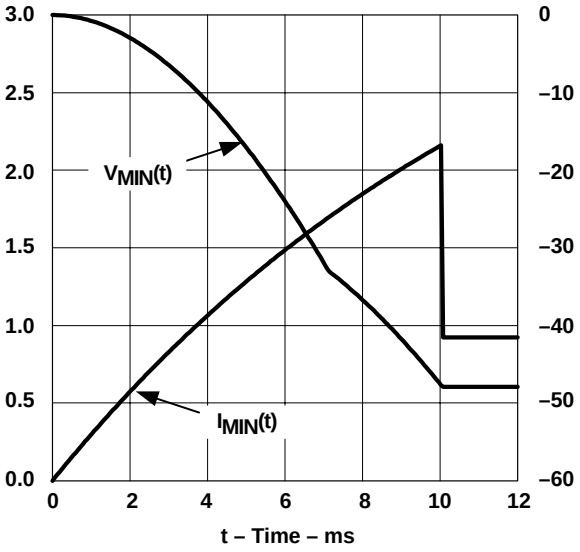

Figure 5. ISR Input Voltage and Current – $IMAX_{MIN}$ Condition

The selection of a minimum value for the fault timing capacitor, C2, is described in more detail in *Section 2.3.7*. Since input current greater than the fault level may occur during the turn-on transient, the time delay generated by C2 must be sufficient to allow charging of the input capacitance after plug-in insertion or remote turn on. Therefore, the total duration of the turn-on transient must be known. However, the internal fault timer is not started until the current fault threshold is crossed, so the time for charging current to ramp to the minimum (i.e., worst-case) fault threshold must also be determined. Ultimately, it is the maximum time *difference*, for a given IMAX value, from fault threshold to the total startup time, which dictates the value of C2.

Inspection of equation 18 for $i_{IN}(t)$ indicates that the current ramp is independent of the supply voltage, but is directly proportional to the IMAX level of the particular module. So the extremes of the fault timing are determined by rewriting equation 18 to determine the time to reach the $I_{FLT(min)}$ under both the $IMAX_{MIN}$ and $IMAX_{MAX}$ conditions.

$$t_{FLT} = - R2 \times C3 \times \ell n\left(1 - \frac{I_{FLT(min)}}{IMAX}\right) \quad (27)$$

and

- $t_{FLT(min)}$ = 4.695 ms, the fault time when IMAX = $IMAX_{MAX}$
- $t_{FLT(max)}$ = 7.956 ms, the fault time when IMAX = $IMAX_{MIN}$

These values were calculated with the 1.84 A minimum fault current determined in Section 2.3.2.

The total duration of the ramp time must also be estimated. From the startup plots of Figures 3 through 5, it is almost intuitive that this value not only depends on the IMAX tolerance, but is also a function of the UVLO threshold and the input supply level. These voltage curves show that an earlier load turn-on, and a higher voltage to charge to extend the total voltage ramp time. Therefore, in order to use equation 26 to determine the total startup times (t_{STM} and t_{STX}), some definitions are needed. First, the worst-case start time calculations should be performed for the maximum input potential, in this case, –72 Vdc. Secondly, the load is assumed to be a constant at the peak input current. But since the bus potential is at its maximum, the current calculated for a –72 Vdc input will be used, or $i_L(t) = I_{IN(max')}$. Lastly, we will define a target DC voltage to be 100mV below the input DC level, or 71.9 V.

By sampling equation 26, first setting $t_{VUV} = t_{VUVM}$ while IMAX = $IMAX_{MAX}$, then for $t_{VUV} = t_{VUVX}$ when IMAX = $IMAX_{MIN}$, the following startup times were determined:

For t = 12.78 ms, $V_{INA}(t)$ = 71.846 V (t_{STX}; $IMAX_{MIN}$ condition)

For t = 9.72 ms, $V_{INA}(t)$ = 71.892 V (t_{STM}; $IMAX_{MAX}$ condition)

The maximum time delay needed to guarantee hot-swap startup when using soft-start, t_{CTSS}, is calculated as:

$$t_{CTSS} = MAX[\,(t_{STX} - t_{FLT}(MAX)),\,(t_{STM} - t_{FLT}(MIN))\,]$$

$$= 9.72\ ms - 4.695\ ms = 5.025\ ms$$

It is interesting to note that, at least for this solution, the maximum timeout needed occurs under the $IMAX_{MAX}$ condition.

Consider one final point regarding soft-start operation. Once capacitor C3 has charged up to its dc level, it will remain charged as long as the board is powered. This means that soft-start operation occurs only at insertion, and is disabled under any other conditions of turn-on, including restart under the fault retry mode of operation, and also from a remote enable using the $\overline{SD}$ input. Transistor Q2 is added to the circuit to provide a discharge path for C3 whenever the output is turned off. The gate of Q2 is driven by the SDFL node, so that Q2 is turned on whenever U1 asserts the fault output, or SDFL is pulled high externally. The soft-start reset action of Q2 ensures that the HSPM soft-starts each time the output is turned on.

2.3.6 Step 6 – Set Average Power Limiting For Pass Fet; Determine Power Limiting Resistor Value, R7

The UCC3921 can be configured for either of the two modes of operation during fault conditions, latched mode or retry mode.

In retry mode, the device periodically turns on the FET switch Q1 and checks for continued fault conditions. Timing control of this mode is automatically provided by the device. During retry operation, U1 alternately charges C2 with a nominal 36-μA internal constant-current source while Q1 is on, then discharges C2 at a nominal 1 μA while the output is off. This provides a nominal 2.7% duty cycle. To select retry mode, resistor R4 in the Figure 1 schematic would **not** be used (left open).

In latched mode, once a fault condition times out, the device latches off the pass element. In order to restart the output, either the SDFL pin must be pulled to the shutdown level for > 1 ms, or device power must be cycled. To select latched operation, install resistor R4 as shown. In this mode, the need for power dissipation limiting is essentially negated; therefore, R7 would not be installed.

When using the retry feature of the UCC3921, care must be taken not to exceed the dissipation capability of the FET switch. Under normal (non-fault) operating conditions, the FET is fully enhanced by the gate drive, and dissipation in the device is relatively low, assuming an appropriate device has been selected for the application parameters. However, under short-circuit conditions, the full-input potential appears across Q1 while it is on. The power limit function gives the user a means of externally limiting the duty cycle of the external FET switching, further reducing it below the nominal 2.7% level. This is done by sensing the output voltage level, and providing additional charging current for the timing capacitor, through a high-value resistor, based on the output level relative to the V_{SS} node of the device, (i.e., the voltage drop across the FET switch.) The total current now available for charging the timing capacitor, I_Q, is now given by equation 28.

$$I_Q = I_q + I_{PL} \tag{28}$$

where:

- I_q = the device internal charging source, 36-μA nominal
- I_{PL} = the current through the power limiting resistor

In Figure 1, R7, connected to the drain of Q1, is the power limiting resistor.

The IRF630 FET selected for this solution comes in the TO–220AB package, rated for a 62°C/W thermal resistance, junction to ambient. Maximum operating junction temperature is specified as 150°C. For the 70°C ambient operating temperature specified in Section 1.2, the average dissipation in Q1 will be limited to 1.0 W as a conservative level. The maximum allowable duty cycle, D, can then be derived from equation 29:

$$D = \frac{P_{D(avg)}}{IMAX_{MAX} \times V_{IN(max)}} \approx 0.23\% \tag{29}$$

Since this is significantly less than the HSPM guaranteed maximum of 3.7%, the power limiting function will be used. Because 1/D >> 1, a good approximation of the timing capacitor charge-current contribution required through R7 (I_{PL} in equation 28) is obtained from equation 30:

$$I_{PL} = \frac{I_{dq(max)}}{D} - I_{q(min)} \quad (30)$$

where:

- I_{dq}(MAX) = maximum capacitor discharge current into the U1 CT pin
- I_q(MIN) = the minimum charging current sourced from CT

Substituting the values from the UCC3921 data sheet for $I_{dq(max)}$ and $I_{q(min)}$,the required power limiting current is determined to be about 634 μA. The value of R7 is then found from equation 31:

$$R7 = \frac{V_{IN} - V_{PLIM}}{I_{PL}} \quad (31)$$

The obvious worst-case dissipation in the FET occurs when input voltage and drain output current are at their maximum. Therefore, the value of 72 V is substituted for V_{IN}, and the calculated value for R7 is:

$$R7 = \frac{72\ V - 5.0\ V}{634\ \mu A} = 105.7\ k\Omega \quad (32)$$

A standard 5% value suffices for this function. R7 is set to 100 kΩ.

2.3.7 Step 7 – Determine value for fault timing capacitor C2

The power-limiting current required, and subsequently the value of R7, are determined under worst-case dissipation conditions (e.g., a short-circuit across the input capacitors). However, during a normal startup voltage ramp, input voltage to the ISRs is not shorted, but ramps up according to the appropriate equations. Therefore, the timing current I_{PL} is not a constant under these conditions, but decreases over the period of the input ramp from a maximum value of $\frac{\left(V_{IN} - V_{PLIM}\right)}{R7}$.

Approximating the input transient as a linear ramp, the average current through R7 is estimated from equation 33.

$$I_{PL(avg)} = \frac{\left(V_{DC} - V_{PLIM}\right)}{2 \times R7} = \frac{\left(V_{IN(max)} - V_{PLIM}\right)}{2 \times R7} \quad (33)$$

Therefore, the minimum value of capacitor C2 needed to ensure startup of the output is:

$$C2 = \left[I_{q(max)} + I_{PL(avg)}\right] \times \frac{t_{CT}}{dV_{CT}} \quad (34)$$

where:

- $I_{q(max)}$ = maximum charging current sourced from CT
- t_{CT} = required fault time delay
- dV_{CT} = the delta-V that must be developed across C2 for the UCC3921 to detect a fault

From the device data sheet, the minimum fault threshold at the CT input pin is given as 2.20 V, and the maximum level for fault reset is 0.57 V. However, for latched mode of operation, only the initial fault timeout is of concern, in which case the voltage at CT is ramping up from 0 V. This allows selection of a slightly smaller value for C2 than if retry mode is used, as shown in equations 35 and 36.

For retry mode:

$$C2 = \left[I_{q(max)} + I_{PL(avg)}\right] \times \frac{t_{CT}}{\left(V_{LS} - V_{LR}\right)} \tag{35}$$

where:

- V_{LS} = the internal fault latch SET threshold
- V_{LR} = the internal fault latch RESET threshold

For latched mode:

$$C2 = \left[I_{q(max)} + I_{PL(avg)}\right] \times \frac{t_{CT}}{V_{LS}} \tag{36}$$

Since the proposed solution makes use of input current slewing, the t_{CTSS} value calculated in *Section 2.3.5 Step 5 – Estimating Ramp TIme* is used. Substituting $t_{CT} = t_{CTSS} \cong 5$ ms, the calculated value of C2 is about 0.88 μF, and a standard value of 1.0 μF was used in the solution.

2.3.8 Step 8. Set resistor R3 value

Resistor R3 is the supply biasing resistor for the UCC3921. The maximum supply current required by the HSPM IC to maintain the internal-shunt-regulator voltage within the data sheet specifications is 2.0 mA. A value of 2.5 mA was used in the development of this solution to provide some margin and bias the IMAX divider network when the supply voltage is at its minimum potential. To provide this minimum bias current, the value of R3 is defined by:

$$R3 = \frac{\left(V_{IN} - V_{REF}\right)}{0.0025} \tag{37}$$

So, the maximum allowable value of R3 is provided by:

$$R3 = \frac{\left(V_{IN(min)} - V_{REF(max)}\right)}{0.0025} = \frac{36\ V - 10.15\ V}{0.0025\ A} \cong 10\ k\Omega \tag{38}$$

At maximum bus potential conditions (–72 V), about 6.64 mA of current could flow through R3 (assuming a 5% tolerance resistor); which is well below the specification maximum of 50 mA. Also, this corresponds to a maximum power dissipation of about 420 mW; therefore, a 1-W-rated resistor is used in this application.

3 Additional Features

The design of the basic power management interface is now complete. The main functions of hot swapping the –48-Vdc input and converting it to local V_{DD} levels is accomplished through the circuitry described previously. However, there are some additional features which can be easily implemented. Two of these functions, which see frequent usage in power management, are presented in the following sections. First, this report describes a host interface to provide a remote shutdown/enable input ($\overline{SD}$) and fault indication to the system. Secondly, an inexpensive circuit is shown for shifting the UVLO threshold of the PT332x module.

3.1 Host Interface to SDFL Pin

Pin 1 of the UCC3921 is a three-function pin. The use of a resistive pull-down at this pin to select the fault mode of operation is described in *Section 2.3.6, Step 6 –Set Average Power Limiting For Pass Fet; Determine Power Limiting Resistor Value, R7.* This pin is also an active-high input for turning off the external FET (shutdown), and provides an output fault indication. However, the signal levels at this pin are referred to the V_{SS} node of the circuit (i.e., the VSS pin of U1). An interface circuit is needed to translate these signals to a system ground reference, and generate the $\overline{FLT}$ output and the $\overline{SD}$ input, as shown in the top level schematic. Figure 6 is the Figure 1 diagram redrawn to show the details of one interface implementation.

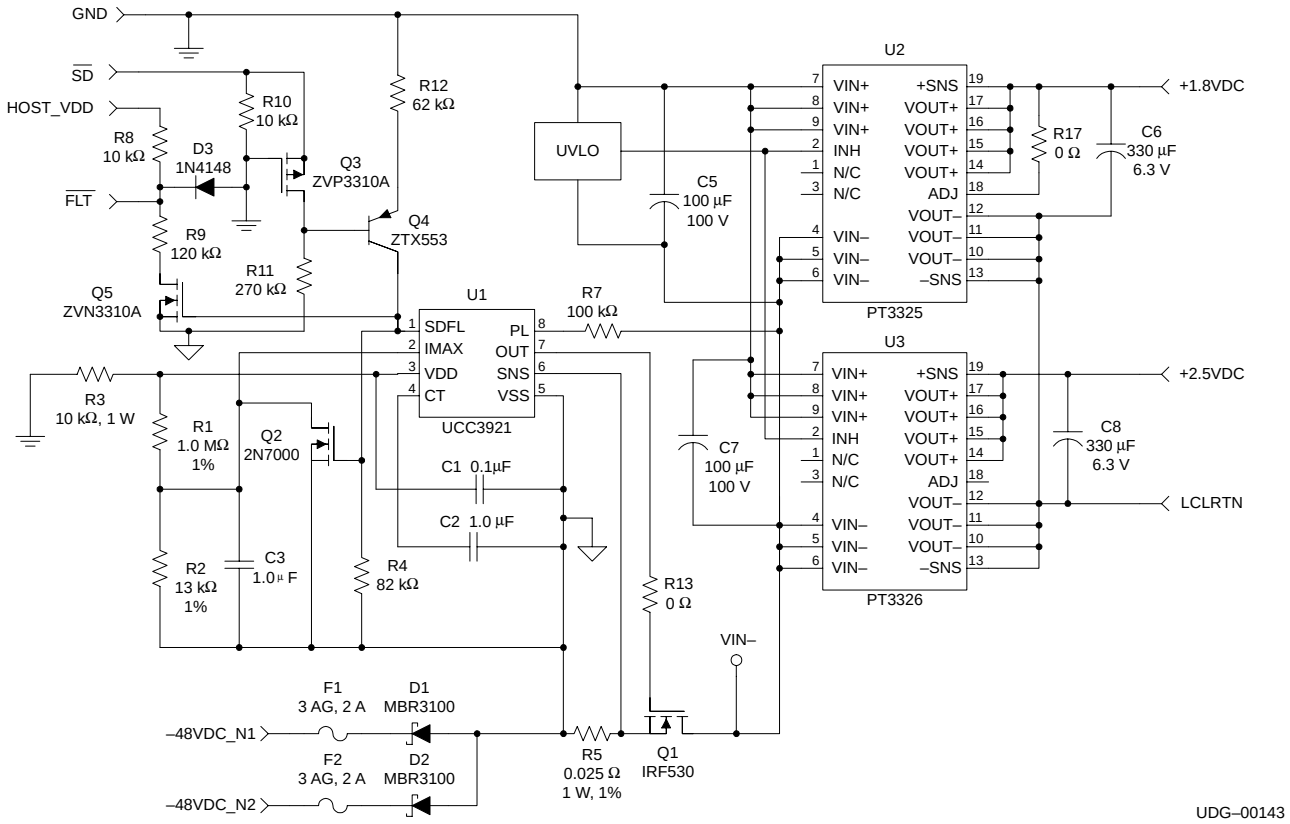

Figure 6. Schematic Diagram with Host Interface Details

The FAULT output translation is comprised of the circuit of R8, R9 and Q5. Under normal operating conditions, U1 sinks a nominal 100 µA at pin 1. This keeps the gate of Q5 discharged. With Q5 turned off, R8 applies a pull-up to the HOST_VDD potential at the $\overline{FLT}$ output, indicating normal operation.

During any condition that causes the HSPM device to turn off the gate drive to the FET Q1, the SDFL output attempts to drive to the UCC3921 V_{DD} rail. Device Q5 turns on, and R8 and R9 form a divider on the HOST_VDD to V_{SS} potential. From the divider equation for the fault signal level, the following equation for R9 is derived.

$$R9 = \frac{V_{FLT\#}}{\left(HV_{DD} - V_{SS} - V_{FLT\#}\right)} \times R8 \tag{39}$$

where:

- $V_{FLT\#}$ = the voltage level of the $\overline{FLT}$ signal line
- HV_{DD} = the voltage level of the system HOST_VDD supply
- V_{SS} = the V_{SS} node potential of the plug-in module

If the maximum assertion level of $\overline{FLT}$, $V_{FLT\#(max)}$, is defined to be 0.5 V maximum, then:

$$V_{FLT\#(max)} = 0.5\ V = 0.5\ V - \left(-\ V_{SS(min)}\right) = 36.2\ V\ , \tag{40}$$

when referenced to the module V_{SS} node, and allowing for about a 300-mV drop across the Schottkys and fuses when the load is not powered. For this condition, the maximum value that should be used in the R9 position is given by equation 41.

$$R9(max) = \frac{V_{FLT\#(max)}}{\left(HV_{DD} - V_{SS(min)} - V_{FLT\#(max)}\right)} \times R8 \tag{41}$$

Substituting the system values into equation 41, and setting R8 to a nominal 10 kΩ, the resulting R9 value is:

$$R9 = \frac{36.2\ V}{[3.3\ V - (-\ 35.7\ V) - 36.2\ V]} \times 10\ k\Omega \cong 129\ k\Omega \tag{42}$$

The next lowest 5% value of 120 kΩ was used for R9. Now, the minimum voltage level for fault assertion can be determined from:

$$V_{FLT\#(min)} = \left[\left(\frac{R9}{(R8 + R9)}\right) \times \left(HV_{DD} - V_{SS(max)}\right)\right] + V_{SS(max)} \tag{43}$$

$$= \left[\left(\frac{120\ k\Omega}{130\ k\Omega}\right) \times (3.3\ V + 72\ V)\right] - 72V \cong -\ 2.5V$$

Due to the possibly large signal level below the host or system ground potential, small-signal diode D3 is used as shown in the schematic to clamp the assertion level at about 0.5 V below the GND node.

The interface block of circuitry must also provide level-shift of the host shutdown or enable input, $\overline{SD}$ in the schematic. A brief description of the circuit operation follows.

To turn on the HSPM output, the $\overline{SD}$ input is pulled high by the host controller. Since the Q3 gate is tied to the system GND node, Q3 turns on and provides a strong pull-up on the base of transistor Q4, above the emitter potential. With Q4 off, the internal pull-down at U1 pin 1 is dominant, and the output pulls to a low state. This enables the hot swap controller to turn on the pass FET Q1.

When shutdown is asserted ($\overline{SD}$ pulls low), FET Q3 turns off. Resistor R11 can now pull the Q4 base towards V_{SS}, and Q4 turns on. Q4 now sources sufficient current from the GND potential to overcome the internal pull-down, pulling pin 1 above the shutdown input threshold. The HSPM IC subsequently turns off Q1.

The use of the two-transistor (Q3/Q4) level shifter as shown in figure 6 provides an additional feature. If at some point the host V_{DD} supply fails while the controlled module is plugged in, the module outputs will be automatically disabled via the HSPM circuit. Loss of the host supply would mean loss of the $\overline{SD}$ drive to the Q3 source, turning off P-FET Q3. Since the Q4 emitter is tied to the GND node, as opposed to a backplane-side input signal, Q4 is still able to source shutdown current into the SDFL pin.

A quick methodology is given here to determine recommended values for resistors R11 and R12. Per the device specification, the SDFL input has a maximum shutdown threshold of (VDD + 1) V. In addition, this pin may sink a maximum of 250 μA. Therefore, R11 and R12 must be selected to ensure that PNP transistor Q4 can source a minimum of 250 μA while pulling the pin high.

Under minimum input supply conditions, the drop across limiting resistor R12 is given by:

$$V_{R12(min)} = -V_{SS(min)} - V_{EC(max)} - V_{SD(max)} \tag{44}$$

Set up this level translator to keep Q4 in saturation under minimum supply conditions. For the ZTX553 transistor, the maximum V_{CE} is specified as –250 mV at a gain of 10. The drop across R12 is:

$$V_{R12(min)} = 35.5\ V - 0.25\ V - 11\ V = 24.25\ V \tag{45}$$

Under the same conditions the current consumed by latching resistor R4 is $I_{R4(max)} = \frac{V_{SD(max)}}{R4_{MIN}} \cong 141\ \mu A$ (assuming a 5% tolerance resistor is used). Therefore, the maximum value of R12 that can ensure shutdown control is determined by equation 46.

$$R12(max) = \frac{V_{R12(min)}}{\left(I_{R4(max)} + I_{SD(max)}\right)} = 62\ k\Omega \tag{46}$$

The drive current that will be needed, and the value for R11 to provide that current can be found from the following.

$$I_{B(Q4)} > \frac{V_{R12(min)}}{[R12(max) \times 10]} = \frac{24.25\ V}{[(1.05 \times R12) \times 10]} \cong 37\ \mu A \tag{47}$$

and,

$$R11 < \frac{\left[-V_{R12(min)} - 0.6V - \left(-V_{SS(min)}\right)\right]}{I_{B(Q4)}} \tag{48}$$

$$= \frac{[-24.25\ V - 0.6\ V - (-35.5\ V)]}{37\ \mu A} \cong 288\ k\Omega$$

The closest available 5% tolerance value is 270 kΩ.

3.2 Alternate Host Interface

The interface circuit described in Section 3.1 (Figure 6) would be useful when the ON/OFF control-electronics' biasing supply (the HOST_VDD input) and the control lines are referenced to the GND node. This is also the return line for the two –48 V power busses. However, in a truly isolated system, logic supply returns would not have a common connection with the power section. Therefore, Figure 7 illustrates an optional interface configuration to maintain isolation from the power bus.

In the Figure 7 circuit, the return of the two DC/DC converters (LCLRTN) is used as the reference for the I/O signals ($\overline{SD}$ and $\overline{FLT}$). Opto-couplers maintain isolation from the primary side. The pull-up on the $\overline{FLT}$ line is shown on the plug-in schematic to provide extra detail. However, this pull-up can just as easily be located in the control module or board, eliminating the need for bussing the HOST_VDD to the controlled slot altogether.

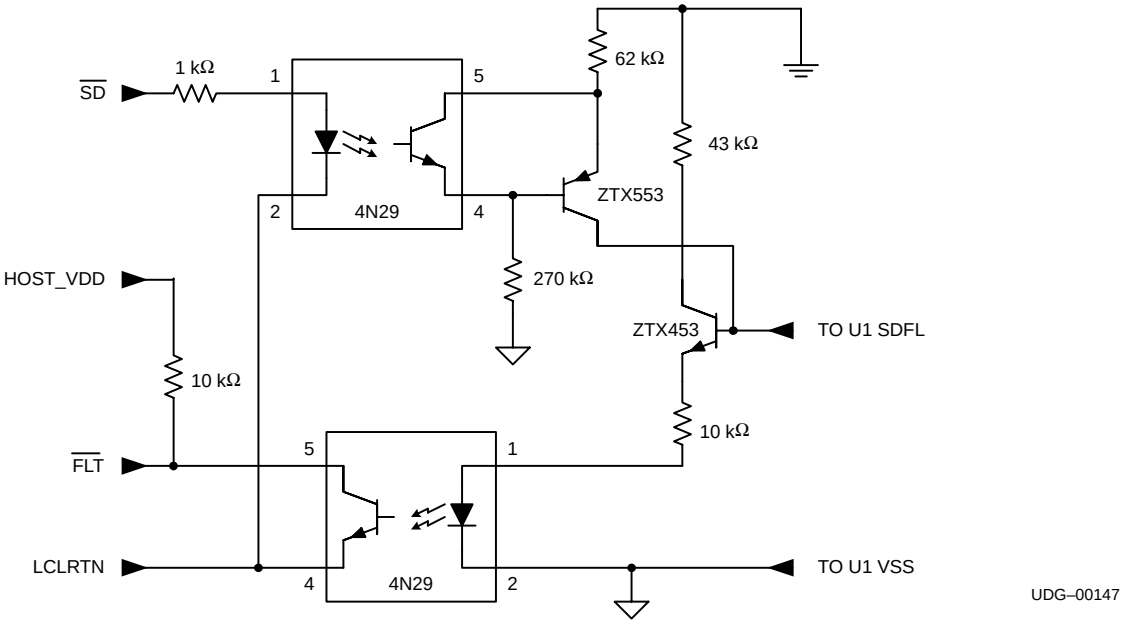

Figure 7. Alternate Host/System Interface for Isolated Controller

3.3 Optional UVLO Circuit

The solution developed through the steps of Section 2.3, *Circuit Design Procedure*, assumes that the internal UVLO circuit of the PT3320 regulators is used. However, during a live insertion, any current consumed by the load, in this case, the two ISRs, is not available for charging up the input capacitance (C5 and C7). For a given maximum current-sourcing level, as controlled by the UCC3921, faster charging of this load capacitance can be achieved when the source does not have to also supply the regulators and secondary-side load. Therefore, when the operating input supply range allows, or if using different converters, or where large input capacitance exists, it may be desirable to keep the load disabled until the input voltage has achieved a higher potential. One way of doing this is to shift the threshold of the UVLO function upward.

The Figure 8 schematic shows the details of an *undervoltage lockout* sub-circuit achieved with a few discrete components. The circuit is driven by the supply voltage across the VIN terminals of U2 and U3. During the input ramp-up transient, diode D4 keeps transistor Q6 off until its breakdown voltage is exceeded. R16 is then able to bias Q7 on, which pulls the converter INH pins to the VIN– potential. This keeps the converter outputs off.

Once the converter input voltage exceeds the D4 Zener threshold, D4 conducts, turning on Q6. Q6 acts to pull the Q7 base low, which turns Q7 off. The inhibit control circuitry of the PT3320 modules features a nominal 10-µA pull-up. With external transistor Q7 presenting a high impedance, the INH input is internally pulled high, above the enable threshold of 2.5 V, and the converters start up. Using the 39-V Zener diode as shown in the schematic should provide a UVLO function of 39 V to 41 V.

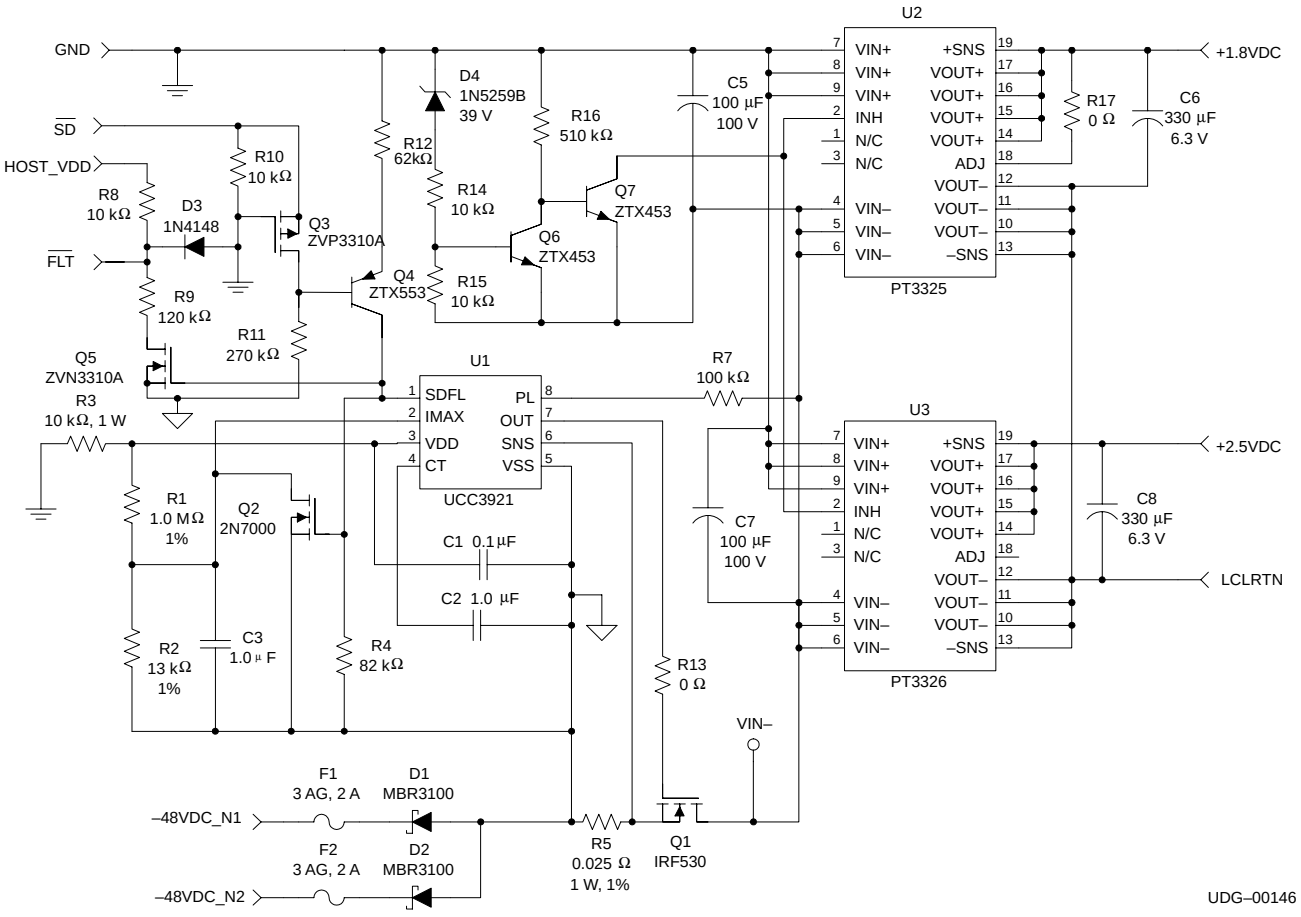

Figure 8. Complete Detailed Application Circuit

4 Performance Evaluation and Sample Waveforms

The oscilloscope plots presented in this section demonstrate the operation of the circuit shown in Figure 8. To obtain these figures, the external UVLO circuit was disabled, so that the DC/DC turn-on is controlled by the on-board UVLO circuit. The HOST_VDD supply was set to a nominal 3.3 V. Unless stated otherwise, the ISR outputs were each loaded at 6.0 A. Generally, the scope channel connections in the plot labels refer to the node names in any of the preceding schematics; I_{IN} refers to input current into the plug-in module.

Figure 9 shows the input voltage ramp-up and output turn-on following a live insertion event, with the supply voltage at –48 Vdc. In Figures 9 and 10, hot swap was performed with the –48VDC_N1 making last. Both figures demonstrate the smooth ramp of the converter input voltage, (i.e., the voltage across filter capacitors C5 and C7) Figure 10 shows the nearly linear ramp of the inrush current during the voltage ramp. Of particular interest is that the startup delay of the converters (from VIN reaching the UVLO threshold) is such that the outputs do not ramp until after the input ramp is complete.

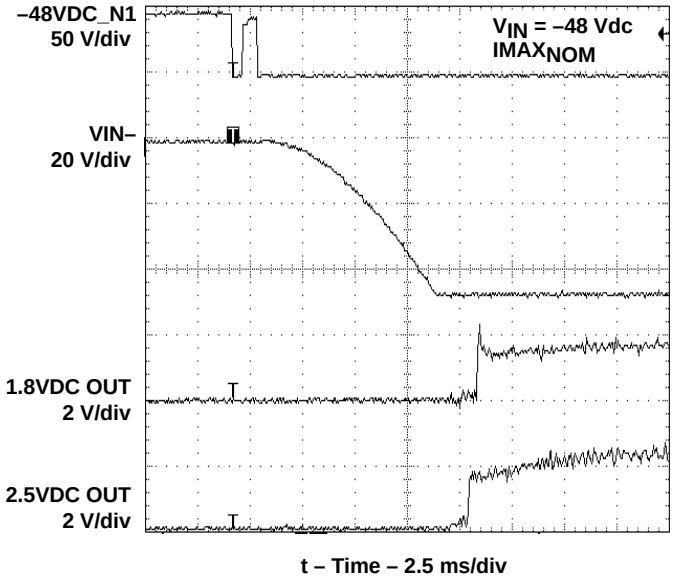

Figure 9. Hot-Swap Startup Sequence

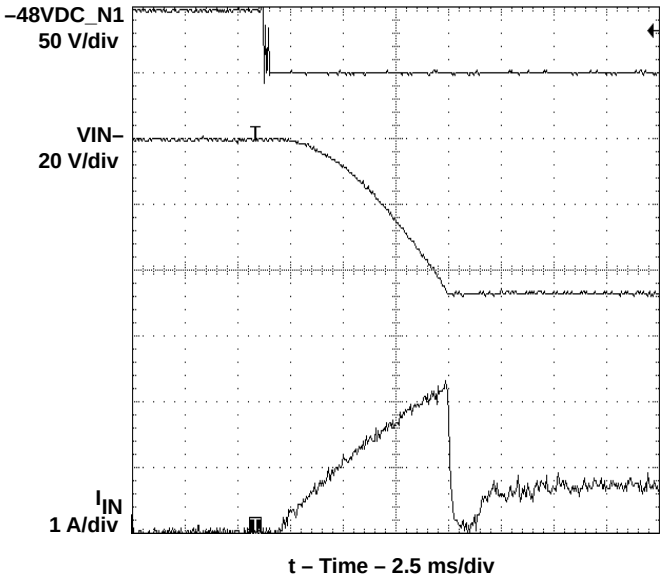

Figure 10. Hot-Swap Startup Input V/I Profile

Figures 11, 12, and 13 show the insertion waveforms for a –72 Vdc bus potential, for an HSPM IC operating at the minimum, maximum and nominal sourcing current levels, respectively.

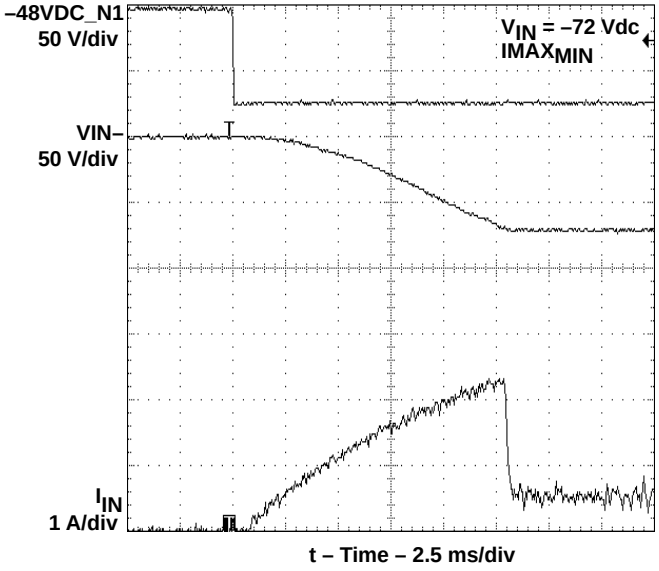

Figure 11. $IMAX_{MIN}$ Startup Waveforms

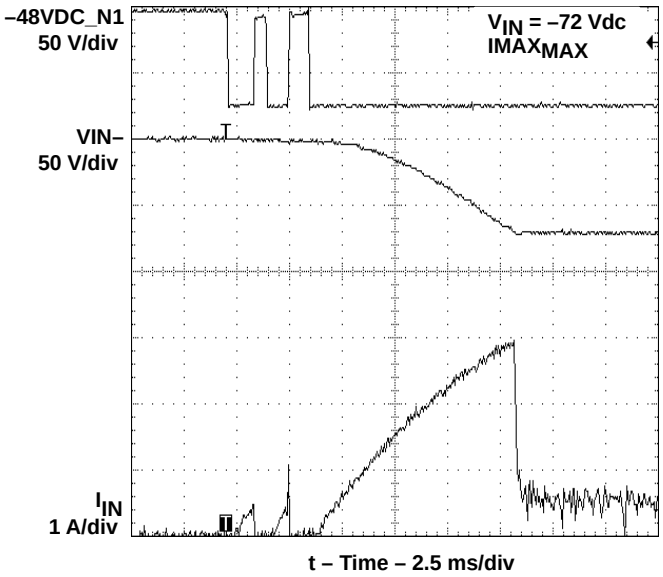

Figure 12. $IMAX_{MAX}$ Startup Waveforms

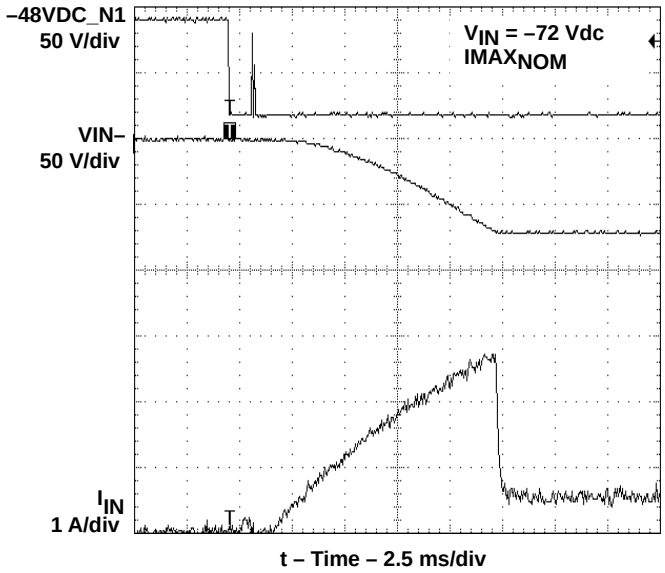

Figure 13. $IMAX_{NOM}$ Startup Waveforms

Figure 12, at –72 Vdc input and $IMAX_{MAX}$ was generated under conditions closely representing the worst-case scenario for starting up with a fully discharged plug-in (t_{CTSS} determination in *Section 2.3.5 Step 5 – Estimating Ramp TIme*). The Figure 12 waveforms confirm that the module starts up smoothly even under this condition. Also, it can be seen that at this input potential, with the extension in rampup time, the turn-on of the two converter modules occurs during the input ramp-up transient.

In order to verify some of the equations used in Section 2.3, *Circuit Design Procedure*, in determining circuit component values, some theoretical input voltage ramp times and peak inrush levels were calculated using equations 19 and 26, under some sample circuit conditions. These start times and peak currents, shown in the *Calculated* columns in Table 3, were determined for an HSPM IC operating at its nominal, minimum and maximum current limit thresholds. A nominal ISR UVLO threshold of 33 Vdc was assumed. These values were then checked against measurements obtained from the transient waveforms of Figures 9 through 13, and similar plots. The results are summarized in Table 3.

Table 3. Startup Time and Peak Current Comparison

SUPPLY VOLTAGE	TOTAL STARTUP TIME (ms)		PEAK CURRENT (A)		CONDITIONS
	Calculated	Measured	Calculated	Measured	
–48 Vdc	8.825	7.85	2.403	2.26	$IMAX_{NOM}$
	10.05	9.05	2.164	1.90	$IMAX_{MIN}$
	7.67	7.15	2.705	2.48	$IMAX_{MAX}$
–72 Vdc	11.13	10.70	2.805	2.66	$IMAX_{NOM}$
	12.685	12.15	2.505	2.26	$IMAX_{MIN}$
	9.66	9.30	3.183	3.0	$IMAX_{MAX}$

Table 3 shows good correlation between the anticipated and actual startup times. In general, the actual ramps were about 1 ms faster at the –48-Vdc input level. The primary factor for this is most likely the delay in ISR output turnon, which means that the use of the maximum input current estimates for $I_L(t)$ in equation 24 is overly conservative. For the –72-Vdc input case, the start time estimates are only about 500 μs too high; not surprising because at this supply level, the converters do start supplying the load currents prior to the end of the input voltage ramp.

The waveform graphics in Figures 14 and 15 demonstrate the startup from $\overline{SD}$ deassertion. For the Figure 15 plot, the soft-start capacitor C3 was removed to show the transient current clamp at the IMAX level. The nominal current limit obtained is the 4.8-A theoretical value. In addition, the –48VDC_N1 traces demonstrate the extent of the disturbance on the supply bus. At 200 mV/div (Figure 15), the bus transients are only about +600/–100 mV about the steady-state level, even without inrush current slewing.

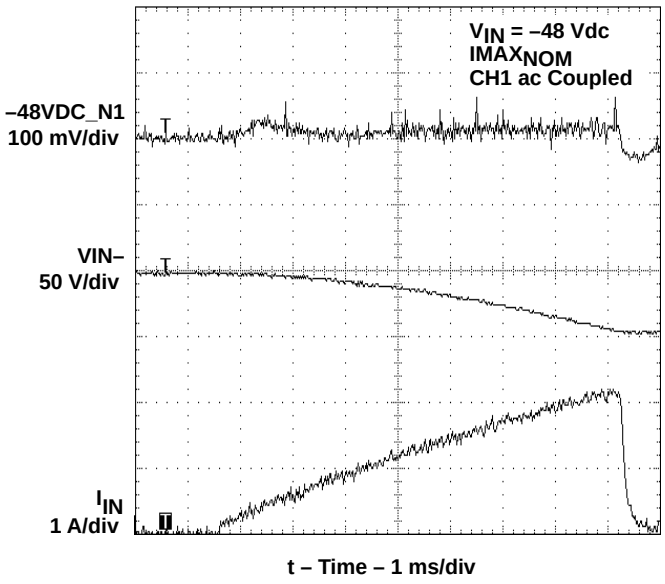

Figure 14. Startup from $\overline{SD}$ Deassertion

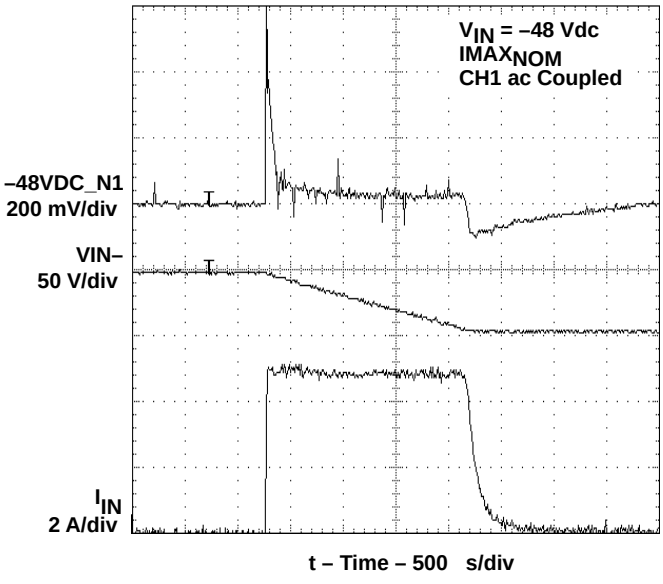

Figure 15. Startup from $\overline{SD}$ – No Soft-Start

Figure 16 shows another hot swap event at the –48-Vdc supply level, with the time base expanded to view the inrush current ramp under soft–start. Using the 10% and 90% points, the average di/dt obtained with the circuit was determined to be:

$$\frac{(2.0\ \text{A} - 0.222\ \text{A})}{6.52\ \text{ms}} \cong 0.27\ \frac{\text{A}}{\text{ms}}\ .$$

Recall that capacitor C3 was selected in Step 4 for a maximum slew rate of 0.5 A per ms; therefore, the average di/dt obtained is approximately half that value.

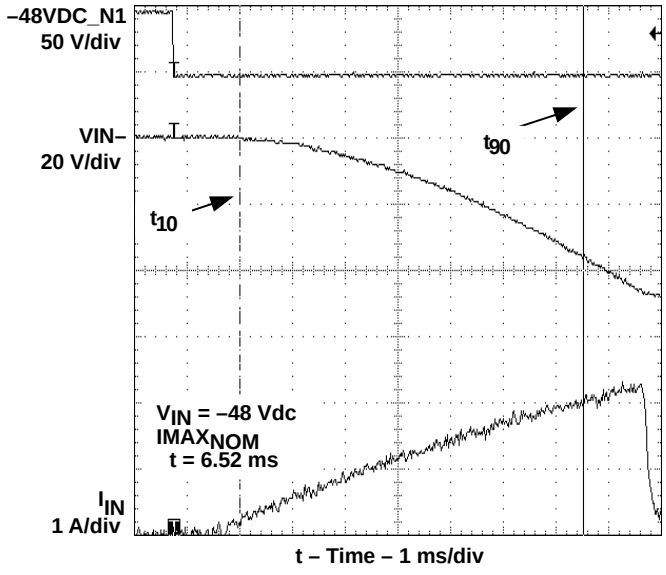

Figure 16. Slew Rate Calculation

The waveforms in Figures 17 and 18 demonstrate the operation of the $\overline{FLT}$ output during startup (Figure 17) and shut-down (Figure 18) sequences, when initiated from the $\overline{SD}$ input.

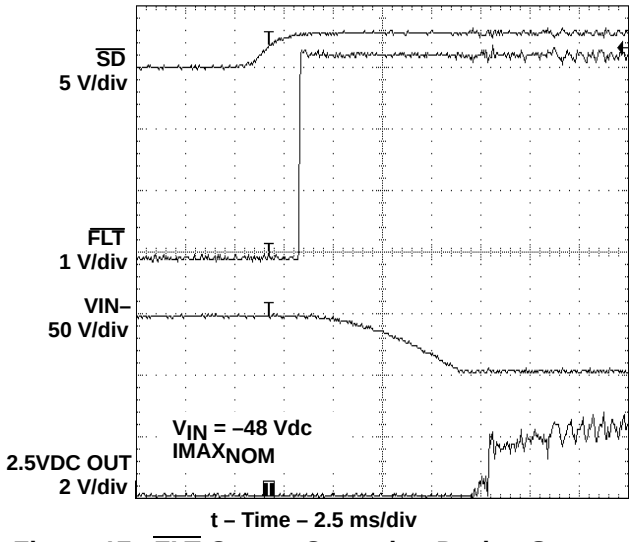

Figure 17. $\overline{\text{FLT}}$ Output Operation During Startup

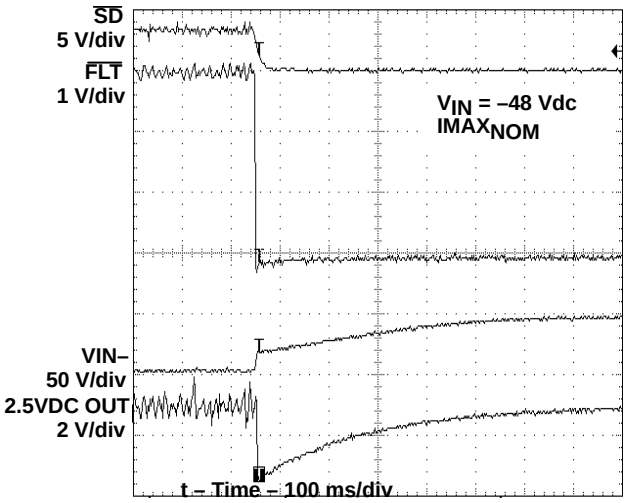

Figure 18. $\overline{\text{FLT}}$ Output Operation During Shutdown

Figure 19 shows the circuit response should the HOST_VDD supply be removed or fail. As desired, the pass FET is switched off, and the $\overline{\text{FLT}}$ output is asserted. The input voltage to the ISRs decays in a manner dictated by the load characteristics. There is an initial step drop in voltage, and then, when the input hits the UVLO threshold, the ISRs turn off, and the 200-µF bulk capacitance is discharged by leakage only.

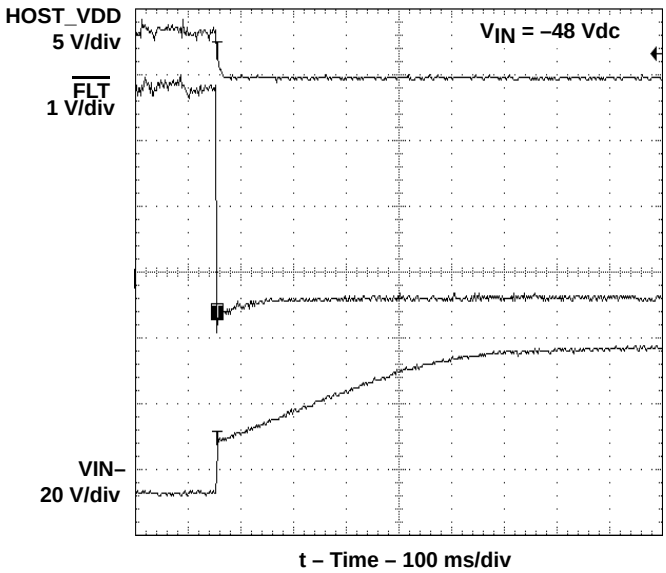

Figure 19. Shutdown for HOST_VDD Failure

The next two scope plots show the circuit's fault response to a short-circuit condition at the DC/DC converter inputs. Figure 20 depicts initial normal steady-state operation with a –48 V dc input supply and about an 800-mA load, from the I_{IN} trace. With the sudden application of a short (see VIN–trace), the HSPM IC clamps the short-circuit current at approximately 4.8 A, times out in about 6 ms, and ultimately latches the pass FET off. Figure 21 shows attempted startup into a short across the VIN terminals of the converters. The input current slews up as programmed, but no voltage develops across the converter inputs (VIN– scale is 1V/div), and the HSPM again times out and latches off. In this case, the total time-out is longer than that shown in Figure 20. Recall that the fault timer does not start until the input current exceeds the nominal 2-A overcurrent threshold.

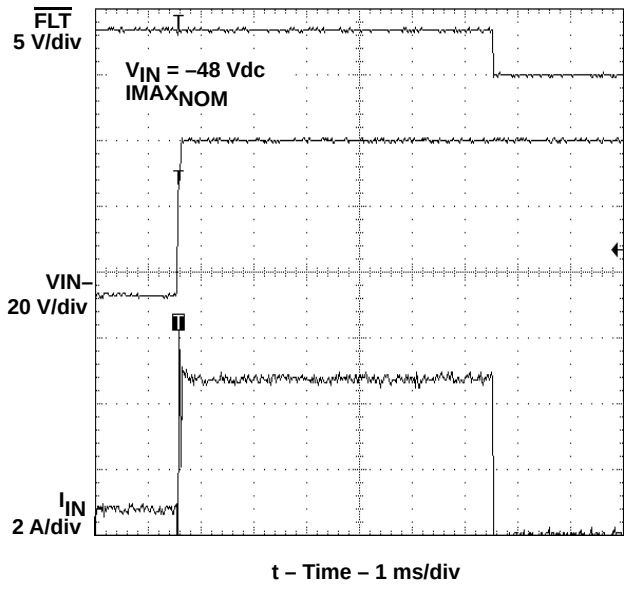

Figure 20. Short-Circuit at Converter Inputs

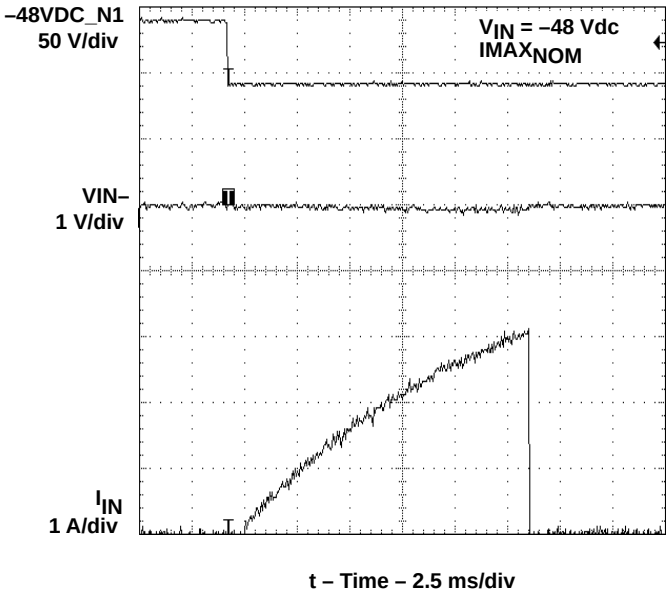

Figure 21. Startup into Shorted ISR Input

The scope plots of Figures 22 and 23 demonstrate the short-circuit response of the PT3320 converters. In Figure 22, the module is initially operating steady-state with –48-V input, and a 6-A load on each of the ISR outputs. When a short-circuit is applied to the +1.8 Vdc output, the converter shuts off, then periodically pulses on to test for a continued fault condition (I_{OUT} trace). Because of the voltage step-down, the input current peaks remain below the HSPM overcurrent threshold, and the HSPM does not trigger. Because of this, the second output (+2.5 Vdc, not shown), can continue to operate normally. Applying a short to the +2.5V output produces the corresponding pulsed current response. Figure 23 is a plot of the same fault conditions, but with the power bus at a –36 V potential.

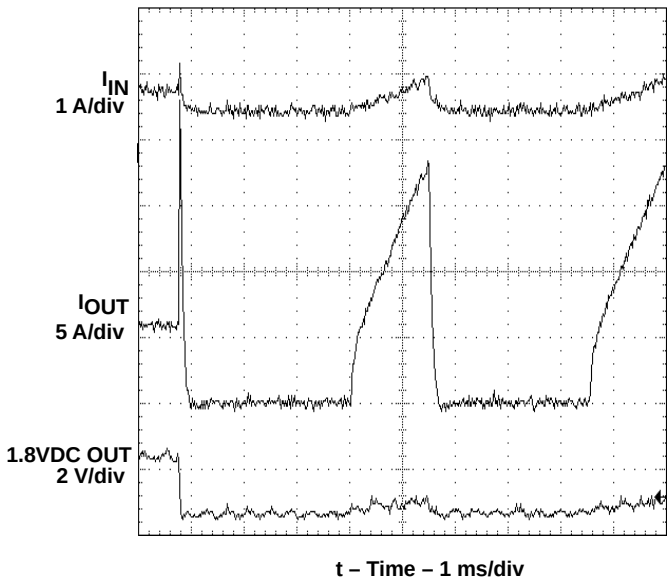

Figure 22. Output Short-Circuit Response (–48-V Supply)

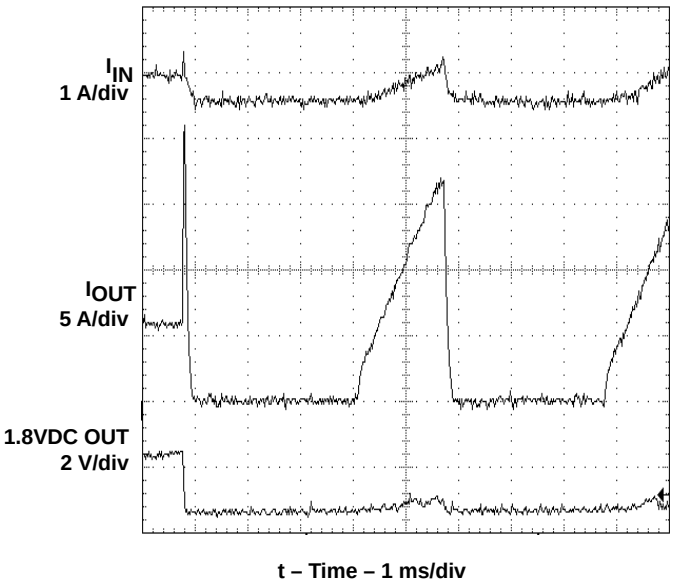

Figure 23. Output Short-Circuit Response (–36-V Supply)

5 Notes

1. The PT3327 module produces a nominal 1.8 Vdc output voltage. However, the PT332x converters also provide for output voltage adjustment from 90% to 110% of nominal value using an external resistor. Due to sample availability at the time of this study, the 2-V PT3325 unit was used, with output adjustment to 1.8-V using R17 in the Figure 1 schematic.
2. Since only three of the available devices in the series are characterized in the data sheet, the PT3321 curves were used as the closest available output voltage/current match to the modules used in this solution.

6 References

1. *UCC3921 Latchable Negative Floating Hot Swap Power Manager*; Data Sheet; Texas Instruments Literature No. SLUS207; March 1998
2. *PT3320 Series 30–Watt Isolated DC/DC Converter;* Data Sheet; Texas Instruments Literature No. SLTS018A; June 2000
3. *Adjusting the Output Voltage of the Power Trends' 30W Isolated DC/DC Converter Series*, Application Note; Texas Instruments Literature No. SLTS018A
4. *Using the Inhibit Function of the Power Trends' 30W Isolated DC/DC Converter Series*, Application Note; Texas Instruments Literature No. SLTS018A
5. *ISR Input/Output Filters*, Application Note; Texas Instruments Literature No. SLTA013A, June 2000

The UCC3921 device parameters used in this document are listed in the Table A–1for quick reference. To aid the user in determining the source of these values, the corresponding data sheet parameter name is shown. For a complete listing of the UCC3921 specifications, the user is referred to the device data sheet.

Table 4. UCC3921 Hot Swap Power Manager Device Parameters

PARAMETER	DATA SHEET REF	CONDITIONS	VALUE	UNIT	DESCRIPTION
V_{FLT}(MIN)	Overcurrent Threshold	Over Op. Temp	46	mV	Minimum fault threshold (Overcurrent Comparator)
V_{FLT}(MAX)		Over Op. Temp	53.5	mV	Maximum fault threshold (Overcurrent Comparator)
V_{REF}(MIN)	Regulator Voltage		9.0	V	Minimum shunt regulator voltage
V_{REF}(NOM)			9.5	V	Nominal shunt regulator voltage
V_{REF}(MAX)			10.15	V	Maximum shunt regulator voltage
V_{OS}	Input Offset Voltage	V_{IMAX} = 100mV	±15	mV	V_{OS} of the Linear Current Amplifier (LCA)
		V_{IMAX} = 400 mV	±30	mV	
I_{BIAS}	LCA Input Bias		500	nA	Input bias current on the LCA
I_q(MIN)	CT Charge Current	I_{PL} = 0	22	µA	Minimum CT charge current (overcurrent condition)
I_q(MAX)		I_{PL} = 0	50	µA	Maximum CT charge current (overcurrent condition)
I_{dq}(MAX)	CT Discharge Current		1.5	µA	Maximum CT discharge current
V_{LS}	CT Fault Threshold		2.2	V	Minimum Fault Comparator SET threshold
V_{LR}	CT Reset Threshold		0.57	V	Maximum Fault Comparator RESET threshold
V_{PLIM}	V_{SENSE} Regulator		5.0	V	Voltage at PL pin (sink condition)
V_{SD}(MAX)	Shutdown Threshold		VDD + 1	V	Maximum shutdown threshold
I_{SD}(MAX)	Input Current, SDFLTCH		250	µA	Maximum I_{IH} at SDFL pin

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Mailing Address:

Texas Instruments
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