ABSTRACT

The TPS43000 is a high-frequency, voltage-mode, synchronous PWM controller that can be flexibly used in buck, boost, buck-boost, and SEPIC topologies. This reference design explains the design procedure of a step-down application from 4.5 V to 8.5 V down to 3.3 V with the TPS43000 PWM controller.

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1 Introduction

This full-featured controller is designed to drive a pair of external MOSFETs (N or P) and can be used with a wide range of output voltages and power levels. It can be widely used in networking equipment, servers, PDAs, cellular phones, and telecommunication applications. The datasheet describes the functionalities of the controller in more detail.

A schematic of this board is shown in Figure 1. Recommended parts list is provided in Table 1. The layout of the PCB board is shown in Figure 6.

The specification for this board is as follows:

- $4.5\, \text{V} \leq V_{\text{IN}} \leq 8.5\, \text{V}$
- $V_{\text{OUT}} = 3.3\, \text{V}$
- $50\, \text{mA} \leq I_{\text{OUT}} \leq 2\, \text{A}$, enters PFM at 200 mA, nominal current is 1 A
- Switching frequency, $f_S = 1\, \text{MHz}$
- Ripple = 1%
- Efficiency at nominal load > 90%

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2 Design Procedure

2.1 Frequency Setting

The TPS43000 can operate either in constant frequency, or in an automatic PFM mode. In the automatic PFM mode, the controller goes to sleep when the inductor current goes discontinuous, and wakes up when the output voltage has fallen by 2%. This pulse skipping can decrease gate-drive losses and significantly improve the efficiency at light load. (Refer to the TPS43000 Data Sheet, TI Literature No. SLUS489 for more information.) The converter is designed to operate at fixed 1 MHz above 0.2 A. The PFM mode is used when the load decreases to below 0.2 A.

A resistor, R4, connected from the RT pin to ground, programs the oscillator frequency. The approximate operating frequency is calculated in equation (1).

\[ f (\text{MHz}) = \frac{38}{R4 \ (\text{k}\Omega)} \]  

\[ R4 = 37.4 \ \text{k}\Omega \] is chosen for 1-MHz operation.
2.2 Inductance Value

The inductance value can be calculated as shown in equation (2).

\[
L_{(\text{min})} = \frac{V_{\text{OUT}}}{f \times I_{\text{RIPPLE}}} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN(max)}}}\right)
\]  

\(I_{\text{RIPPLE}}\) is the ripple current flowing through the inductor, which affects the output voltage ripple and core losses. According to the specification, the converter enters PFM mode at 200 mA, so the desired ripple current is 0.4 A. Based on this and the 1-MHz operating frequency, the inductance value is calculated at 5.0 \(\mu\)H.

2.3 Input and Output Capacitors

The output capacitance and required ESR can be calculated by equations (3) and (4).

\[
C_{\text{OUTPUT (min)}} = \frac{I_{\text{RIPPLE}}}{8 \times f \times V_{\text{RIPPLE}}}
\]  

\[ESR_{\text{OUT}} = \frac{V_{\text{RIPPLE}}}{I_{\text{RIPPLE}}}
\]

With 1% output voltage ripple, the capacitance required is at least 1.5 \(\mu\)F and its ESR should be less than 81.7 m\(\Omega\). A Panasonic 4-V, 120-\(\mu\)F capacitor is chosen with an ESR of 18 m\(\Omega\).

The required input capacitance is calculated in equation (5). The calculated value is approximately 20 \(\mu\)F. A 22-\(\mu\)F ceramic capacitor is used in order to handle the ripple current.

\[
C_{\text{IN (min)}} = I_{\text{OUT (max)}} \times D_{\text{max}} \times \frac{T_{S}}{V_{\text{IN (ripple)}}}
\]

2.4 Compensation Design

The TPS43000 uses voltage-mode control. R1, R2, and R3 along with C1, C2 and C3, form a Type III compensator network. The L-C frequency of the power stage, \(f_C\) is approximately 6.5 kHz and the ESR zero is around 73.7 kHz, as shown in Figure 2. The overall crossover frequency, \(f_{\text{0db}}\), is chosen at 50 kHz for reasonable transient response and stability. The two zeros, \(f_{Z1}\) and \(f_{Z2}\) from the compensator are set at 0.5 \(f_C\) and \(f_C\) separately. The two poles \(f_{P1}\) and \(f_{P2}\) are set at ESR zero and 0.5 \(f\). The frequency of poles and zeros are defined by the following equations:

\[
f_{Z1} = \frac{1}{2\pi \times R2 \times C1}
\]

\[
f_{Z2} \approx \frac{1}{2\pi \times R1 \times C3} \quad \text{assuming } R1 \gg R3
\]

\[
f_{P1} = \frac{1}{2\pi \times R3 \times C3}
\]

\[
f_{P2} = \frac{1}{2\pi \times R2 \times C2} \quad \text{assuming } C1 \gg C2
\]
The compensator values are calculated as follows:

\[ C_1 = 270 \text{ pF}, \quad C_2 = 3.0 \text{ pF}, \quad C_3 = 560 \text{ pF}, \quad R_1 = 100 \text{ k}\Omega, \quad R_2 = 115 \text{ k}\Omega, \quad \text{and } R_3 = 5.76 \text{ k}\Omega. \]

![POWER STAGE GAIN AND PHASE VS FREQUENCY](image)

**Figure 2.**

### 2.5 MOSFETs and Diode

For a 3.3-V output voltage, the lower the \( R_{\text{DS(on)}} \) of the MOSFET, the higher the efficiency. Also, considering the 1-MHz switching frequency, Si3442DV (\( R_{\text{DS(on)}} = 65 \text{ m}\Omega \)) and Si3443DV (\( R_{\text{DS(on)}} = 70 \text{ m}\Omega \)) are chosen for fast switching speed.
2.6 Current Limiting

Two types of current limiting can be selected from the controller. Detailed information is available in the datasheet (TI Literature No. SLUS489). A jumper, JP2, is used to choose different current limiting. By tying the CCS pin to VIN, the controller enters pulse-by-pulse current limiting and the current-limiting threshold is calculated by equation (6):

\[
I_{_{MAX\ (p-p)}} = \frac{150 \text{ mV}}{R_{DS(on)}}
\]  

in which \( R_{DS(on)} \) is the on-resistance of Q2. In this design, the threshold is approximately 2.3 A.

By tying the CCS pin to ground, the controller enters hiccup-mode overcurrent limiting. The current-limiting threshold is calculated in equation (7). The threshold in this case is approximately 3.8 A.

\[
I_{_{MAX\ (hu)}} = \frac{250 \text{ mV}}{R_{DS(on)}}
\]

2.7 Voltage Sense Resistor

R1 and R6 operate as the output voltage divider. The internal reference voltage is 0.8 V. The relationship between the output voltage and divider is described in equation (8).

\[
\frac{V_{_{REF}}}{R_6} = \frac{V_{_{OUT}}}{R_1 + R_6}
\]

With an R1 value of 100 kΩ and 3.3-V voltage regulation, R6 is calculated at 32.4 kΩ.
3 Test Results

3.1 Efficiency Curves
Efficiency tested at different loads and input voltages is shown in Figure 4. The maximum efficiency is as high as 94% at 0.5 A output. The light-load efficiency is much improved due to the PFM operation mode.

3.2 Typical Operation Waveform
Typical operating waveforms are shown in Figure 5 with \( V_{IN} = 4.5 \) V and \( I_{OUT} = 2 \) A.

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**Figure 3.** Efficiency tested at different loads and input voltages.

**Figure 4.** Typical operating waveforms.
3.3 Output Ripple Voltage and Transient Response

The output ripple is approximately 28.8 mV peak-to-peak with a 1.5 A output and is shown in Figure 4. Figure 5 shows load changes from 0.5 A to 1.5 A, where the overshooting voltage is approximately 10 mV.

Figure 5. Output Ripple

Figure 6. Transient Response
4 PCB Layout

Figures 8 and 9 show the PCB layout. All components are on the top side of the board. The bottom side of the board is the ground plane.

Figure 7. Components Placement

Figure 8. Top Side
5 List of Materials

Table 1 lists the board components and their values, which can be modified to meet the application requirements.

Table 1. Bill of Materials

<table>
<thead>
<tr>
<th>REFERENCE DESIGNATOR</th>
<th>QTY</th>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>MFG</th>
<th>SIZE</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1</td>
<td>GRM1885C1H271J K</td>
<td>Capacitor, ceramic, 270 pF, 50 V, COG, 5%</td>
<td>Murata</td>
<td>603</td>
</tr>
<tr>
<td>C2</td>
<td>1</td>
<td>GRM1885C1H3R0J K</td>
<td>Capacitor, ceramic, 3 pF, 50 V, COG, 5%</td>
<td>Murata</td>
<td>603</td>
</tr>
<tr>
<td>C3</td>
<td>1</td>
<td>GRM188R71H561J K</td>
<td>Capacitor, ceramic, 560 pF, 50 V, 5%</td>
<td>Murata</td>
<td>603</td>
</tr>
<tr>
<td>C4,C5,C6</td>
<td>3</td>
<td>JMK219R71C474K K</td>
<td>Capacitor, ceramic, 0.47 µF, 16 V, X7R, 10%</td>
<td>Murata</td>
<td>805</td>
</tr>
<tr>
<td>C7,C9</td>
<td>2</td>
<td>JMK325BJ226MM</td>
<td>Capacitor, ceramic, 22 µF, 6.3 V, 20%</td>
<td>Taiyo-Yuden</td>
<td>1210</td>
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<tr>
<td>C8</td>
<td>1</td>
<td>EEFUD0D121R</td>
<td>Capacitor, 120 µF, 4.0 V, 18 mΩ, 20%</td>
<td>Panasonic</td>
<td>7343 (D)</td>
</tr>
<tr>
<td>D1</td>
<td>1</td>
<td>ZHCS2000</td>
<td>Diode, schottky, 2 A, 40 V</td>
<td>Zetex</td>
<td>SOT23–6</td>
</tr>
<tr>
<td>J1,J2</td>
<td>2</td>
<td>PTC36SAAN</td>
<td>Header, 4-pin, 100 mil spacing, (36-pin strip)</td>
<td>Sullins</td>
<td>0.100 x 4&quot;</td>
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<tr>
<td>L1</td>
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<td>CDRH6D38</td>
<td>Inductor, SMT, 5.0 µH, 2.9 A, 24 mΩ</td>
<td>Sumida</td>
<td>6.7 X 6.7 mm</td>
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<tr>
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<td>Resistor, chip, 115 kΩ, 1/16-W, 1%</td>
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<td>603</td>
</tr>
<tr>
<td>R3</td>
<td>1</td>
<td>Std</td>
<td>Resistor, chip, 5.76 kΩ, 1/16-W, 1%</td>
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<tr>
<td>R4</td>
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<td>603</td>
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<tr>
<td>R7</td>
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<td>603</td>
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<tr>
<td>Q1*</td>
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<td>Si3442DV</td>
<td>MOSFET, N-channel, 2.5-VGS, 4 A, 70 mΩ</td>
<td>Siliconix</td>
<td>TSOP–6</td>
</tr>
<tr>
<td>Q2*</td>
<td>1</td>
<td>Si3443DV</td>
<td>MOSFET, P-channel, 2.5-VGS, 4.4 A, 90 mΩ</td>
<td>Siliconix</td>
<td>TSOP–6</td>
</tr>
<tr>
<td>U1*</td>
<td>1</td>
<td>TPS43000PW</td>
<td>Multi-topology high-frequency PWM controller</td>
<td>Texas Instruments</td>
<td>TSSOP–16</td>
</tr>
<tr>
<td>TP1,TP2,TP5</td>
<td>3</td>
<td>240–333</td>
<td>Test point, red, 1 mm</td>
<td>Farnell</td>
<td>0.038&quot;</td>
</tr>
<tr>
<td>TP3,TP4,TP6</td>
<td>3</td>
<td>240–333</td>
<td>Test point, black, 1 mm</td>
<td>Farnell</td>
<td>0.038&quot;</td>
</tr>
<tr>
<td>N/A</td>
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<td>PMP143</td>
<td>Printed circuit board, FR4, 0.032, SMOBC</td>
<td>any</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: * All components can not be substituted.
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