3.3-V to 12-V High-Efficiency Ceramic Only Non-Synchronous Boost Converter

Sophie Chen Systems Power

ABSTRACT

This reference design describes the functionality of the controller in more detail. This design explains the procedures of a non-synchronous boost converter from 3.3 V to 12.0 V with TPS43000 PWM controller.

Contents

1 Introduction ................................................. 2
2 Design Procedure ............................................ 3
3 Test Results .................................................. 5
4 PCB Layout .................................................... 7
5 List of Materials .............................................. 8

List of Figures

1 Schematic of PMP145 ........................................ 2
2 Power Stage Gain and Phase vs Frequency .................. 4
3 Efficiency vs Load Current .................................. 5
4 Typical Operation Waveforms ............................... 6
5 Output Ripple ................................................ 6
6 Transient Response .......................................... 6
7 PCB Layout .................................................... 7

List of Tables

1 List of Materials .............................................. 8

Trademarks are the property of their respective owners.
1 Introduction

The TPS43000 is a high-frequency, voltage-mode, synchronous PWM controller that can be flexibly used in buck, boost, buck-boost, and SEPIC topologies. This full-featured controller is designed to drive a pair of external MOSFETs (N/P) and can be used with a wide range of output voltages and power level. It can be widely used in networking equipment, servers, PDAs, cellular phones, and telecommunication applications.

A schematic of this board is shown in Figure 1. Recommended parts list is provided in Table 1. The layout of the PCB board is shown in Figure 7.

The specification for this board is as follows:

- $V_{IN} = 3.3 \, \text{V} \pm 10\%$
- $V_{OUT} = 12 \, \text{V}$
- $I_{OUT} = 0.2$ to $1.5 \, \text{A}$, nominal current is $1 \, \text{A}$ and no PFM.
- Ripple = $1.5\%$
- Efficiency at nominal load > $90\%$

Figure 1. Schematic of PMP145
2 Design Procedure

2.1 Frequency Setting

The TPS43000 can operate either in constant frequency, or in an automatic PFM mode. In the automatic PFM mode, the controller goes to sleep when the inductor current goes discontinuous, and wakes up when the output voltage has fallen by 2%. Please refer to the slus489 datasheet for more detail. The PFM mode is not used in this application. The converter operates at fixed 300 kHz.

A resistor $R_4$, which is connected from RT pin to ground, programs the oscillator frequency. The approximate operating frequency is calculated in equation (1).

$$f \text{ (MHz)} = \frac{38}{R_4 (k\Omega)}$$

(1)

$R_4 = 127 \text{ k}\Omega$ is chosen for 300 kHz operation.

2.2 Inductance Value

The inductance value is calculated in equation (2).

$$L_{MIN} = \frac{V_{OUT} \times D \times (1 - D)^2}{f \times 2 \times I_{OUT(min)}}$$

(2)

$I_{RIPPLE}$ is the ripple current flowing through the inductor, which affects the output voltage ripple and core losses. Based on 20% current ripple and 300 kHz, the inductance value is calculated as $5.5 \mu\text{H}$ and a $5.6-\mu\text{H}$ inductor is used.

2.3 Input and Output Capacitors

The output capacitance and the ESR needed is calculated in equations (3) and (4).

$$C_{OUTPUT(min)} = \frac{I_{OUT(max)} \times D_{MAX}}{f \times V_{RIPPLE}}$$

(3)

$$ESR_{OUT} = \frac{V_{RIPPLE}}{I_{OUT(max)} \times I_{IN(ripple)}} \left(1 - \frac{D_{MAX}}{2}\right)$$

(4)

With 1% output voltage ripple, the capacitance needed is at least $31 \mu\text{F}$ and the ESR should be less than $17 \text{ m}\Omega$. Four $10-\mu\text{F}/16-\text{V}$ ceramic capacitors are used.

The input capacitance is shown in equation (5). The calculated value is about $78-\mu\text{F}$ and a $180-\mu\text{F}$ low-ESR SP capacitor is used.

$$C_{IN(min)} = I_{IN(ripple)} \times D_{MAX} \times \frac{T_S}{V_{IN(ripple)}}$$

(5)
2.4 Compensation Design

For the boost converter, there is a right-half-plane (RHP) zero, which moves with the operating conditions. The phase starts to drop off a decade before this zero, limiting the system's bandwidth. In this circuit, the RHP zero is around 17.2 kHz. The L-C frequency of the power stage, \( f_C \), is around 2.9 kHz and the ESR zero is around 1.6 MHz, as shown in Figure 2. The overall crossover frequency, \( f_{0db} \), is chosen at 5 kHz for reasonable transient response and stability. R1 to R3 and C1 to C3 form a Type III compensator network. Both zeros \( f_{Z1} \) and \( f_{Z2} \) from the compensator are set at 0.5 \( f_C \) and \( f_C \) to compensate the phase delay caused by RHP zero. Only one pole, \( f_{P1} \), is set up at the RHP zero. C2, related to the second pole, is open because the ESR zero is as high as 1.6 MHz. The frequency of poles and zeros are defined by the following equations:

\[
\begin{align*}
  f_{Z1} &= \frac{1}{2 \times \pi \times R2 \times C1}; \\
  f_{Z2} &= \frac{1}{2 \times \pi \times R1 \times C3}, \quad \text{assuming } R1 \gg R3 \\
  f_{P1} &= \frac{1}{2 \times \pi \times R3 \times C3}; \\
  f_{P2} &= \frac{1}{2 \times \pi \times R2 \times C1}, \quad \text{assuming } C1 \gg C2
\end{align*}
\]  

(6) (7)

The compensator values are shown below:

\[ C1 = 33 \text{ nF}, \quad C2: \text{open}, \quad C3 = 1000 \text{ pF}, \quad R1 = 100 \text{ k}\Omega, \quad R2 = 1.65 \text{ k}\Omega; \quad R3 = 9.31 \text{ k}\Omega. \]

The compensator values are shown below:

C1 = 33 nF, C2: open, C3 = 1000 pF, R1 = 100 kΩ, R2 = 1.65 kΩ; R3 = 9.31 kΩ.

2.5 MOSFETs and Diode

Si4442DY (\( R_{DS(on)} = 7.5 \text{ m}\Omega \)) is chosen. MBRD835L is used for the rectify diode.
2.6 Voltage Sense Resistor

R1 and R6 operate as output voltage divider. The internal reference voltage is 0.8 V. The relationship between the output voltage and divider is shown in equation (8).

\[ \frac{V_{\text{REF}}}{R6} = \frac{V_{\text{OUT}}}{R1 + R6} \]  

(8)

With 100-kΩ R1 and 12.0-V output regulation, R6 is calculated as 7.15 kΩ.

3 Test Results

3.1 Efficiency Curves

The tested efficiency at different loads and input voltages are shown in Figure 3. The maximum efficiency is as high as 93.3% at 0.5-A output.

![Efficiency vs Load Current](image-url)
3.2 Typical Operation Waveform

Typical operation waveform is shown in Figure 4 with $V_{IN} = 3.3\, \text{V}$, $I_{OUT} = 1.0\, \text{A}$.

![TYPICAL OPERATION]

Figure 4.

Ch1: gate-source voltage of Q1; Ch2: drain-source voltage waveform of Q1.

3.3 Transient Response and Output Ripple Voltage

The output ripple is about 140 mV peak-to-peak at 1.5-A output.

When the load changes from 1.0 A to 1.2 A, the oversooting voltage is about 200 mV.

![OUTPUT RIPPLE][TRANSIENT RESPONSE]

Figure 5.

Figure 6.
4 PCB Layout

Figure 7 shows the PCB layout. All the components are on the top side of the board. The bottom side of the board is the ground plane. The PWB is made large to dissipate the losses.

Top View

Bottom View

Figure 7. PCB Layout
5 List of Material

Table 1 lists the board components and their values, which can be modified to meet the application requirements.

Table 1. List of Materials

<table>
<thead>
<tr>
<th>Size</th>
<th>Reference</th>
<th>Qty</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitor</td>
<td>C1</td>
<td>1</td>
<td>Ceramic, 33 nF, 25 V, X7R, 10%, 603</td>
<td>Murata</td>
<td>GRM188R71E333K</td>
</tr>
<tr>
<td></td>
<td>C2</td>
<td>1</td>
<td>Ceramic, open, 50 V, COG, 5%, 603</td>
<td>Murata</td>
<td>GRM1885C1HxxxJ</td>
</tr>
<tr>
<td></td>
<td>C3</td>
<td>1</td>
<td>Ceramic, 1000 pF, 50 V, X7R, 10%, 603</td>
<td>Murata</td>
<td>GRM188R71H102K</td>
</tr>
<tr>
<td></td>
<td>C4, C5, C6</td>
<td>3</td>
<td>Ceramic, 0.47 µF, 25 V, X7R, 10%, 805</td>
<td>Murata</td>
<td>GRM21BR71E474K</td>
</tr>
<tr>
<td></td>
<td>C7</td>
<td>1</td>
<td>180 µF, 4.0 V, 18 mΩ, 20%, 7343 (D)</td>
<td>Panasonic</td>
<td>EEFU0G181R</td>
</tr>
<tr>
<td></td>
<td>C8, C9, C10, C11</td>
<td>4</td>
<td>Ceramic, 10 µF, 16 V, 10%, 1210</td>
<td>Murata</td>
<td>GRM32ER61C106K</td>
</tr>
<tr>
<td>Diode</td>
<td>D1</td>
<td>1</td>
<td>Schottky, 8 A, 35 V, DPAK</td>
<td>ON Semiconductor</td>
<td>MBRD835L</td>
</tr>
<tr>
<td>Terminal Block</td>
<td>J1, J2</td>
<td>2</td>
<td>2-pin, 6 A, 3.5 mm, 0.27 x 0.25&quot;</td>
<td>OST</td>
<td>ED1514</td>
</tr>
<tr>
<td>Inductor</td>
<td>L1</td>
<td>1</td>
<td>SMT, 5.6 µH, 8.8 A, 11.4 mΩ, 12.9 mm sq</td>
<td>Sumida</td>
<td>CEP125–5R6</td>
</tr>
<tr>
<td>Resistor</td>
<td>R1</td>
<td>1</td>
<td>Chip, 100 kΩ, 1/16 W, 1%, 603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td></td>
<td>R2</td>
<td>1</td>
<td>Chip, 1.65 kΩ, 1/16 W, 1%, 603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td></td>
<td>R3</td>
<td>1</td>
<td>Chip, 9.31 kΩ, 1/16 W, 1%, 603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td></td>
<td>R4</td>
<td>1</td>
<td>Chip, 127 kΩ, 1/16 W, 1%, 603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td></td>
<td>R5</td>
<td>1</td>
<td>Chip, 1 kΩ, 1/16 W, 1%, 603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td></td>
<td>R6</td>
<td>1</td>
<td>Chip, 7.15 kΩ, 1/16 W, 1%, 603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td></td>
<td>R7</td>
<td>1</td>
<td>Chip, 49.9 Ω, 1/16 W, 1%, 603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Q1</td>
<td>1</td>
<td>N-channel, 30 V, 17 A, 7.5 mΩ, SO–8</td>
<td>Siliconix</td>
<td>Si4442DY</td>
</tr>
<tr>
<td>IC</td>
<td>U1</td>
<td>1</td>
<td>Multi-topology high-frequency, PWM controller,</td>
<td>Texas Instruments</td>
<td>TPS43000PW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TSSOP–16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test Point</td>
<td>TP1, TP2, TP3, TP4, TP5, TP6</td>
<td>6</td>
<td>Black, 1 mm, 0.038&quot;</td>
<td>Farnell</td>
<td>240–333</td>
</tr>
<tr>
<td></td>
<td>N/A</td>
<td>1</td>
<td>Printed circuit board, FR4, 0.032, SMOBC</td>
<td>any</td>
<td>PMP145</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2002, Texas Instruments Incorporated