Performance Comparison of Integrated Circuit Controllers for Hot Swap in Telecom Systems

Andrew Ripanti
System Power

ABSTRACT

Various integrated circuit controllers are currently available for implementing hot swap in telecommunication (nominal –48-V supply) systems. Two such device types are the TPS239x series and the LT1640A series. Devices from each family were placed in appropriate application circuits and exercised in different application scenarios that may typically be encountered in a working system. Comparison of the features and performance of each is presented here.

Contents

1 Introduction ................................................................. 1
2 Test Circuits ................................................................. 4
3 Evaluation Results ....................................................... 6
4 Conclusion ................................................................. 16

1 Introduction

Hot swap capability is a feature that has become pervasive in today’s electronic systems. Hot swap is the action of inserting modules or cables into a host system or backplane, without first interrupting power to the system, and without disturbing transactions that may be occurring within the system. Target systems range from small, consumer devices such as laptop peripherals, digital cameras, and PDAs to provider-level and infrastructure-scale equipment. The area of telecommunication and datacommunication (telecom/datacom) systems has long required hot swap capability. To meet the high-availability and maintainability requirements, hot swap capability has been implemented in these systems for a number of years. Consequently, solutions have evolved over time, from early proprietary, discrete-component implementations, to those based on integrated controller devices designed specifically to address this function. This application note examines two such controllers, and discusses the feature sets, performance, benefits and trade-offs of each.

One such device, or family of devices, is the TPS239x series from Texas Instruments (TI). There are presently four devices available within this family. The core devices are the TPS2390 and TPS2391. These devices offer programmable current limiting, with current slew rate control, fault protection during steady-state operation, a remote enable input, and status reporting all in an 8-pin MSOP package. The supply range is suitable to the majority of telecom applications, and it has a transient rating to 100 V. The TPS2392 and TPS2393 devices feature the same core current control circuitry, but add such features as programmable undervoltage and overvoltage lockout (UVLO and OVLO), power status reporting and insertion detection. The trade-off involves moving to a larger package, a 14-pin TSSOP, with its slightly larger PCB footprint.

Trademarks are the property of their respective owners.
For the same –48-V applications, Linear Technology Corporation offers the LT1640AL and LT1640AH devices. These also provide controlled load turn-on during hot swap, circuit-breaker protection during operation, and load power status reporting. The LT1640AL/AH provide individual input pins for user programming of the module’s UVLO and OVLO thresholds. An external three-resistor divider string can be used to set the lockout thresholds. These two devices are available in both 8-pin PDIP and SOIC.

Targeted for the same application environment, the two controller families share a number of common features and functions. However, they differ in one fundamental aspect; that is, the basic topology employed by each in order to ramp the input voltage to the load in a controlled manner. In these negative-voltage systems, the load side of the hot swap circuit is typically the input side of a power converter or several parallel converters. Usually isolated, switching DC-to-DC converters, these supplies are required to convert the bussed high-voltage to the point-of-use levels used by the module’s electronics (5-V, 3.3-V, 2.5-V, etc.). These bricks are characteristically bypassed by a large amount of input capacitance. It is this capacitance that creates the biggest issue with hot swap; discharged input bulk capacitance, when connected to the backplane, draws huge transient currents, drooping supply voltage levels, disrupting other modules in a rack, and causing both immediate damage and latent defects. It is the primary job of the hot swap controller, regardless of which one is employed, to manage the application of power to the plug-in during the hot swap event.

The TPS239x series use an external N-channel power FET and low-value current sense resistor to control load power-up. They operate as controlled-current devices. Each employs a high-gain amplifier in a closed-loop configuration in order to regulate current sourced to the load during periods of high-demand; e.g. when charging the power module bulk capacitance. A block diagram of the circuit is shown in Figure 1. A reference voltage is applied to the non-inverting input of the linear current amplifier (LCA). Load magnitude information is fed to the inverting input as the drop across the sense resistor, \( R_{SNS} \). The LCA slews the gate of the pass FET to limit the load current to the reference value. Once the load capacitance is fully charged up, and demand rolls off, the LCA drives the gate to its supply rail to fully enhance the FET and provide a low impedance supply path. The result is direct control of how much current can be drawn by the load.

![Figure 1. TPS239x Current Control Loop](UDG-03090)
During a hot swap event, two characteristics of the resultant inrush current are of concern to the system operation and reliability. High transient peaks cause concern due to the degradation and damage issues already mentioned. Current limiting protects against these spikes. However, the slew rate at which the current ramps to its peak magnitude (often referred to as the di/dt) can also disturb system operation. High slew rates are another bane of power supplies, in that there is a finite response time of a supply’s load regulation. As the supply adjusts to meet the increased demand, output voltages can momentarily droop or glitch, again jeopardizing system operation. Also, large current slew rates contribute to radiated noise levels, increasing the amount of engineering effort and component costs to meet industry emissions requirements.

In addition to peak limiting, the TPS239x architecture easily lends itself to slew rate limiting. By starting each power-up event from a zero-value voltage reference, then gradually increasing that reference value over time, the load current acquires the same ramp profile as the reference. As seen in Figure 1, the TPS239x devices provide a constant-current charging source at the IRAMP pin. By connecting a small-value capacitor between this pin and the –VIN pin, the user has easy control of the load slew rate. The constant-current charging of the capacitor results in a linear voltage ramp at the pin \( v(t) = \frac{I_1 \times dt}{C_{RAMP}} \); this ramp then translates into a linear ramp of load current, as determined by the \( C_{RAMP} \) value.

The LT1640Ax devices use a different mechanism for controlling the voltage ramp to the load. A basic block diagram is shown in Figure 2. As with the TPS239x, the LT1640 uses an external FET to turn on and off power to the load, and a sense resistor in series with the load and FET to provide load magnitude information to the device. During the insertion process, when the power pin contacts are bouncing, the LT1640 senses an undervoltage condition, and maintains a pull-down (to VEE node) on the FET gate. Once input power stabilizes, the pull-down is released, and the FET gate is charged via a nominal 45-µA source. Resistor \( R_{FB} \) and capacitor \( C_{FB} \) act as a feedback network to control current. When the FET turns on, the GATE voltage is held virtually constant by this network. Current to the load is limited according to the equation:

\[
I_{LOAD} = 45 \, \mu A \times \left( \frac{C_{LOAD}}{C_{FB}} \right)
\]  

The SENSE pin voltage is continuously monitored during this voltage ramp period. The 45-µA source is applied to the FET as long as the current remains below the selected fault level. If current should exceed this level, as with a shorted load, the internal source is switched off and the GATE pin is rapidly pulled low again. For a good load, when the drain voltage has finished ramping, the device charges the gate voltage to its final value, completing the current path.
This configuration also requires the use of a second capacitor, C2 in Figure 2, placed in parallel with the gate-to-source capacitance of the FET. During hot swap events, capacitor C2 prevents the FET gate from being momentarily pulled high until such time as the LT1640A can actively pull it low.

2 Test Circuits

A sample device from each of the two groups was connected in comparable test circuits, such as may be used for a 50-W load, with an input supply range of \(-36\) V to \(-72\) V. The load is assumed to be an integrated switching converter with either an input UVLO function, or in the case of the LT1640, having an enable input connected to the PWRGD/PWRGD pin, such that the module is off during voltage ramp. In this case, the hot swap load is characterized primarily by the input bulk capacitance.

The schematic for the TPS239x circuit is shown in Figure 3. The LT1640A-based circuit is shown in Figure 4. These schematics are essentially the typical application circuits shown in each manufacturer’s respective data sheets.

For the circuit in Figure 4, the VSRC node was generally tied to a separate 6-V voltage source referenced to the VOUT-node. Exceptions to this configuration are noted in the descriptions of the related tests.
Figure 3. TPS2390/TPS2391 Test Circuit Schematic

Figure 4. LT1640AL/LT1640AH Test Circuit Schematic
3 Evaluation Results
The devices were tested under the events and conditions described in this section.

3.1 Hot Swap Performance
The first area of functionality compared was the primary function, hot swap control with subsequent ramp-up of voltage to the load. Figures 5 and 6 show each device turning on into a 100-µF load capacitor after being hot swapped into a live –48-V backplane. Each device serves to inhibit any current flow during the contact bounce period, and until the input has stabilized. Also, each device limits the peak inrush current to the load as predicted by their data sheet equations. Note that because of the fundamental difference in architectures (capacitive feedback versus active current control), the LT1640A-based design must be configured to limit below its fault, or circuit breaker, threshold. Otherwise, inrush trips the fault comparator and causes the output to be shut down. On the other hand, with the TPS239x, the current limit level is the fault level, which must be set to a value greater than the anticipated load.

As discussed in the Introduction section, the TPS239x solution also features externally settable slew rate control. Figure 6 demonstrates the two-slope nature of this profile. (In practice, two different current sources are applied at the IRAMP pin, each switched in at different times.) Each ramp period produces very linear current ramps. This yields a predicable slew rate over operating conditions of load and input voltage, and from one board to another.

One benefit of the TPS2390–based design is that current slew rate, and peak current limiting are independent of the magnitude of the load capacitor. By definition equation (1), peak inrush current with the LT1640A is directly proportional to load capacitance. (Bench testing confirms this.) On the other hand, as capacitance varies over temperature and tolerance, or if a plug-in is populated with the wrong value, the TPS239x continues to provide consistent control (see Figure 7). Notice that with the larger 147-µF load, the voltage ramp-time is extended accordingly, however, the peak current magnitude is maintained at the programmed 2 A level.
Independence from load characteristics becomes increasingly important when a faulty, or especially a shorted load is powered. Figures 8 and 9 show each device starting-up into a shorted load. The LT1640A detects the fault as current exceeds the circuit breaker threshold, and shuts down. However, both the peak magnitude and slew rate are increased considerably over the normal load condition (Figure 5). With the TPS239x, the load current follows the same profile, limits at the programmed level, then turns off when its fault timer expires (Figure 9). This time period, denoted by $t_W$ on the waveform, is set by the user with a small capacitor at the FLTTIME pin.
3.2 Circuit Breaker Function

Once supply voltage has been ramped to the load electronics and the load begins normal operation, each of these devices continuously monitors the current level. If a fault condition is detected, they have the ability via the pass FET, to rapidly disable power to the load. This provides a useful circuit breaker function which generally preserves any one-shot, mechanical fuse that typically is used as a back-up. As an electronic circuit breaker, it has the added benefit of being resettable, saving on service calls and repair work. Figures 10 and 11 compare the short circuit responses of the two circuits. Each provides a rapid circuit break function. However, it takes more than 25 µs for the LT1640A to bring the current spike back below the fault level. The TPS239x responded in approximately 3.5 µs, which closely approximates the specified glitch filter delay time. Total time to return the current to below the fault level is approximately 3.9 µs. Under this condition, the added R-C time constant on the FET gate, resultant from the LT1640A topology, is detrimental to the performance of the circuit.

Figure 10. LT1640AL Short Circuit Response

Figure 11. TPS2390 Short Circuit Response
3.3 Load Surge Response

Another consideration in designing the power interface section for a hot-swap-capable board is how it should handle momentary load surges. These surges may have various causes, such as hard-disk spin-up, input power brown-outs, or switchover from battery-backed to off-line operation. The devices tested provide two different types of response. The LT1640A, with its voltage-only detection, provides a rapid shut-down of the load if the current level ever exceeds the programmed fault threshold. This is shown in Figure 12. The LT1640A applies a 3-µs deglitching filter to the signal, but any additional filtering requires an external filter on the SENSE signal, as described in the manufacturer’s data sheet.

![Figure 12. LT1640AL Load Surge or Current Spike Response](image1)

In contrast, the TPS239x response to the same overcurrent condition is shown in Figure 13. The TPS239x devices distinguish between an overcurrent condition exceeding the current limit threshold, and a severe overcurrent condition (referred to as overload in the device data sheets). An example of such an overload is a short circuit. The TPS239x family of devices fixes this overload threshold at nominally 2.5 times the current limit level. For an overcurrent condition, the TPS239x provides a current-regulated output for a period of time, before shutting down the load. If the fault subsides prior to the filter time, the circuit returns to low resistance switch operation, and power to the load continues uninterrupted. This filter time is the same delay period set by the capacitor at the FLTTIME pin, as mentioned in the Figure 9 discussion. This feature allows the plug-in to ride out some transient current glitches. This operation was demonstrated here using the TPS2392 in order to display the response of the PG output in this situation. Note that the PG assertion status is constant; PG is not reset for load faults unless an actual fault timeout occurs.

![Figure 13. TPS2392 Load Surge or Current Spike Response](image2)
3.4 Remote Enable

Another aspect of the system level power management that should be addressed is the need for remote control of a module's powered status. A system host-level controller may be desirable, and can be implemented with a system board or backplane hot plug controller. This capability can be useful in several instances; for example, system control of when a plug-in powers up after insertion, the ability to electrically isolate a faulty card from the power bus without an immediate service call, power management or load sharing, particularly during periods of reduced capacity, such as during an AC power interruption, memory and driver resource reallocation, and finally, a controlled power down prior to a pending board extraction.

The TPS239x devices provide a dedicated input for this enable function. Logic thresholds for this pin are referenced to the –VIN pin, so interface to the input requires some type of isolated or level-translated signal. However, once implemented, this provides a simple logic-level control for the system host.

Ostensibly, the same logic control should be available with the LT1640Ax, using the UV input pin. Again, thresholds are referenced to the negative rail, so a similar interface is required. However, one issue found with the LT1640A, is that once input power is applied, the device does not lend itself well to being held off externally. This is because the bias current of the DRAIN pin provides a low-current path back to the supply negative rail. Although small in magnitude, if the load itself, in the off state, does not present a low-enough impedance to the hot swap output, the output terminals can charge up to an unacceptable voltage level. The sample of devices tested leaked about 91 µA on average, at a 48-V supply potential. So for example, if the load looks like 10 kΩ, then only about 1 V develops across the output terminals. However, if the load should fail open-circuit, then the load capacitance ultimately charges to nearly the input DC level. Perhaps more importantly, this loading applies regardless of why the load is inhibited; i.e., even if an external enable is not used, the current path is also active when the controller has switched off the load due to a supply undervoltage, overvoltage, or load current fault.

3.5 Fault Retry Operation

As with any hot swap implementation, the designer on a telecom application needs to consider the circuit's response after a load fault. Should the circuit latch off the load, or is it preferable to enter a retry mode? Latch-off operation offers the security of preventing power-up if there's possibly something wrong with a board. On the other hand, a controlled retry mode can protect against load faults, while offering the possibility of recovering from transient fault conditions, even without a service call or debug.

With the TPS-series of devices, both options are readily available. The TPS2390 features latch-off operation; after a load fault timeout, the pass FET is held off. The output can only be reset by toggling the EN input low, then high, or by cycling input power to the device. The TPS2391 is the same device as the TPS2390, with the exception that, after a load fault, the device periodically retries the load to check for the continued existence of the fault condition. The pass FET is switched on and off at approximately a 1% duty cycle, to limit average power dissipation in the external FET. In addition, each time the load is disabled, the ramp control cap is discharged, which resets the soft-start feature for each subsequent FET enable.
The LT1640Ax are strictly latch-off devices. Fault retry operation can be implemented with an external one-shot circuit. The manufacturer’s suggested discrete implementation is shown in Figure 14. During normal operation, Q3 keeps capacitor C3 discharged and Q2 is off; the device UV and OV pins are biased by the resistor divider. After occurrence of a load fault, when the GATE pin pulls low, Q2 turns on and pulls the UV pin low, resetting the LT1640A fault logic. Once C3 charges completely, the UV pin is released, and the GATE pin retries the load. The off time delay is user-programmable via the selection of R7 and C3. Notice that the implementation requires the addition of 6 additional components, including a 100-V FET and capacitor.

![Figure 14: Adding Automatic Retry Operation to the LT1640Ax](UDG-03087)

### 3.6 UVLO/OVLO Protection and Additional Features

Each type of hot swap controller can provide UVLO and OVLO protection. The LT1640Ax facilitates this function by providing dedicated inputs for setting these thresholds, the UV and OV pins. As shown in the application schematic (Figure 4), the thresholds are programmed with a three-resistor divider network off the input supply rails. To enable power to the load, the UV input must be above the internal reference, and OV must be below reference.

The TPS2390 and TPS2391 do not offer these dedicated inputs. However, they do feature an internal UVLO circuit set for turn-on at a nominal −30-V input level, targeted at a majority of telecom applications. This can simplify circuit design for those who can use the internal setting.

The TPS2390 and TPS2391 EN input is provided with a fairly precise comparator, as opposed to a strictly logic input. Because of this, it can be used as either a UVLO or OVLO programming pin. The external UVLO threshold, in order to be effective, must be set higher than the device-internal threshold. Figure 15 shows how an external divider can be used to set the new threshold. Figure 16 shows EN being used to establish a threshold for overvoltage shutdown. The LT1640A implementation still provides the better threshold accuracies.
Figure 15. EN Used for UVLO Shutdown

For improved lockout accuracy, the TPS239x family offers easy migration to the TPS2392 or TPS2393 device. The TPS2392 and TPS2393 contain the same core functional blocks as the TYP2390/TPS2391 (LCA, ramp control circuit, fault timer, circuit breaker). However, they add several key features, such as programmable UVLO/OVLO thresholds, a powergood output (PG), and insertion detection inputs.

Figure 17 shows the external connections and basic functional blocks of the UV and OV circuitry. The operation is analogous to that of the LT1640Ax in that the thresholds are easily established via a three-resistor divider connected across the supply rails. However, a useful feature of this circuit is the easy programming of the UV and OV hysteresis values. As shown in the Figure 17 diagram, the input comparators each contain switched current sources, which after comparator trip, generate additional bias on the input nodes. This allows user-programming of the hysteresis through selection of the divider R1 value as follows:

\[ V_{HYS_{UV}} = V_{HYS_{OV}} = 10 \text{ } \mu A \times R1 \]  \hspace{1cm} (2)

In addition, UV and OV threshold tolerance is improved over the TPS2390/91 solution. The UV/OV reference tolerance, over temperature, is 2.86%, for performance comparable to the 2.4% tolerance of the LT1640Ax.
Like the LT1640Ax, the TPS2392/93 also provide an open-drain, active-low power good output (PG). With either device type, these signals provide a simple method for holding off downstream converters until input voltage to the converters has ramped to near input-DC levels. This brick-enable scheme allows decreasing current limit and fault current thresholds, as the supply doesn’t have to provide inrush and load current at the same time.

One practical aspect of using the active-low powergood outputs is to be aware of the circuit response when operating close to supply UV levels. Switching noise of the high-to-low transition on PWRGD (LT1640AL) or PG (TPS2392/93) can couple into the UV comparator circuit, causing oscillations as the FET drain voltage passes through the power good threshold. Figure 18 shows an example of the LT1640AL oscillating during a load ramp event. In this instance, the test circuit of Figure 4 had a measured UV threshold (rising supply) of 32.8 V. For this test, the input supply was set to –35.8 VDC. The PWRGD pin was pulled up via 750-kΩ resistor to a secondary 8-V supply which was referenced to the VOUT-node, simulating direct connection to a micro-ampere-level converter pull-up. Even with this 3-V input supply margin, the repeated fault causes the GATE pin to cease driving at each transition, with the load voltage hovering about the powergood threshold indefinitely, until a clean transition eventually occurs with a final current pulse to finish charging the load.
It is possible to stabilize the LT1640Ax operation near the UV threshold. A 3300 pF capacitor on the UV input, connected to VEE, allowed smooth operation of the test board down to a supply voltage of \(-33\, \text{V}_{\text{DC}}\).

For comparison, Figure 19 shows the TPS2392 operation under similar conditions. The tested device was placed in the typical application circuit shown in the TI data sheet, with the PG pin connected as shown in either Figure 28 or 29 of that data sheet. This test circuit was also set up for a nominal 32.8 V UVLO threshold, with a measured threshold of 32.5 V. The input supply was set to \(-32.5\, \text{V}_{\text{DC}}\) for the scope plots of Figures 19 and 20. Even with this lack of any supply margin, both the load voltage ramp and PG output assertion are free of oscillations, including at the time of PG switching.

**Figure 18. LT1640AL Operation Near UVLO Threshold**

**Figure 19. TPS2392 PG Weak (\(-10\, \mu\text{A}\)) Pull-Up**

**Figure 20. TPS2392 PG High-Voltage Pull-Up**
The stability of the circuit at powergood assertion has two primary influences, the strength of the pull-up on the output pin, and also the dV/dt of the high-to-low transition. Therefore, another circuit configuration worth testing is when this output is opto-coupled to the converter enable, as shown in both manufacturers' data sheets. In this situation, drive for the opto LED is commonly obtained from the input supply high rail. The high-voltage input can produce a large dV/dt when the output is switched. Figure 20 shows the TPS2392 operating in this configuration, with PG pulled up to \(-48\text{V}_\text{RTN}\) through a 30-k\(\Omega\) resistor. Notice that this event is also free from oscillations, whereas the LT1640AL was found to oscillate in this configuration also.

Another potential issue with the PWRGD/PWRGD output is that its status appears, from testing, to be a function of DRAIN pin voltage only. Unlike the TPS2392 and TPS2393, which inhibit or reset PG assertion under supply UV/OV, or load current fault conditions, the LT1640Ax asserts the powergood output if the DRAIN pin voltage is below the threshold, regardless of whether the UV pin is pulled low, for example, or a load fault has been detected. Therefore, if the FET drain is not pulled above \(V_{PG}\), a false powergood can be indicated. See the earlier discussion regarding DRAIN pin leakage, in the Remote Enable section, for one potential scenario in which this can occur.

Another feature of the TPS2392 and TPS2393 devices is the independent insertion detection inputs. In order to enable a load ramp, both of these pins must be pulled low (below 1 V, referenced to the \(-\text{VIN}\) pin). These pins facilitate a plug-in design that requires full seating of the card in its slot prior to load enable. This is accomplished by connecting each input to connector pins, preferably at opposite ends of the card connector edge. The pull-downs are applied on the backplane side of the interface. Thus, as the card may be rocked back and forth during insertions, the insertion filter is reset anytime either contact breaks. When both contacts are solidly mated, the timer can expire and, if all other input conditions are met, the current ramp sequence is initiated. Note that once power pins have mated, the controller maintains small pull-ups on these pins; therefore, no additional circuitry is needed to establish the high logic level (pins unmated). The scope plot in Figure 21 shows an example of the insertion detection function. In this example, all other enable requirements are established prior to the time window of the sweep. The load power-up is initiated on the transition of the INSA pin.

![Figure 21. TPS2392/TPS2393 Insertion Detection and Filtering](image-url)
4 Conclusion

Sample devices from each manufacturer’s product line were placed in correlating application circuits. Testing demonstrated that each device type is capable of controlling load turn-on during a hot swap event, including limiting inrush current and minimizing droops on the input supply. However, the TPS239x series, due to the active current control, produces a more consistent response when the load is other than nominal, particularly in the case of a short circuit. In addition, the TPS239x has the feature of simple programming of the charging current slew rate, using a single, inexpensive ceramic capacitor. Slew rate with the LT1640A was also fairly low under the load and peak current conditions tested; however, for a given configuration it is still dependent on the load status.

Circuit breaker response was faster with the TPS239x devices. The extra capacitance on the LT1640Ax GATE pin, a direct consequence of the control topology, has to have a negative effect on the circuit’s response time.

In the case of non-catastrophic load surges, the LT1640A circuit generally provides the faster FET turn-off. With the TPS239x, the device fault time is user-programmable; however, each application has some minimum fault time-out requirement to allow for initial start-up of the load. What this does provide though, is a nice glitch filter against current spikes, such that the circuit can ride out transients caused by other expected noise events within the system.

One benefit of the LT1640A is that two key features are made available in the simplest device, an 8-pin controller. These features are the programmable UVLO and OVLO thresholds, and a powergood output. These are also available within the TPS239x series if the user selects the TPS2392 or TPS2393 in the 14-pin version. However, the package trade-off is between an 8-pin SOIC and a 14-pin TSSOP; which have nearly the same outermost dimensions.

Finally, two other comparisons were made: usage with a fault retry mode of operation, and stability with the powergood output switching when operating with low input supplies, close to the UVLO threshold. One useful feature of the TPS239x series is that retry operation is simply a question of selecting the retry-mode device (either TPS2391 or TPS2393). For the LT1640A, implementing a retry mode increases circuit complexity and component count, as shown in the Figure 14 schematic. Regarding the sensitivity to powergood switching, each device type can be made stable over the full UV/OV window. However, no precautions or circuit recommendations are addressed in the LT1640A data sheet, leaving the user to a trial and error process.

In summary, both controller types are capable of the basic functions of hot swap. The TPS239x, with its active current limiting, has the edge in consistent inrush profiles, independent of load condition. Also, its incorporation of the current ramp pin (IRAMP) enables a significant feature of user control of the soft-start or current slew rate. Under catastrophic fault conditions, the circuit breaker operation of the TPS239x was found to be faster than that of the LT1640Ax. But at the same time, less severe load faults can be current limited for a user-selectable time period, prior to turning off the load. This should make the TPS239x less sensitive to nuisance trips in noisy environments. In either case, if a fault retry mode is wanted, it is simply a case of device selection with the TPS239x series.
Probably the biggest benefit to the LT1640A–based solution is that it integrates the most useful features in the lowest pin-count package. User programming of the UVLO and OVLO thresholds, and a powergood output are available in an 8-pin device. In addition, the tolerance of these thresholds is tighter than what’s offered in the TPS239x series, although the TPS2392 and TPS2393 tolerances are very close. An application scenario in which the LT1640Ax solution may be more appropriate is one in which a rapid shut-down of the load is wanted anytime the current exceeds the fault threshold. As long as this doesn’t produce an overly sensitive response, some systems may benefit from this.

But on a final note, if feature set is going to be the determinant in foregoing active current control, then the designer should reconsider the TPS2392 (or TPS2393, as required). This is a solution to gaining the flexibility of programmable UV and OV lockouts, and a powergood output, while retaining the benefits of closed-loop control. In addition, the voltage lockout circuitry provides easy hysteresis programmability, a more discriminate powergood function, and two-point insertion detection. When all the results of this comparison are considered together, the overall advantage seems to go to the TPS239x family of devices.

5 References
1. TPS2390/TPS2391 Simple –48-V Hot Swap Controller, Data Sheet (SLUS471)
2. TPS2392/TPS2393 Full-Featured –48-V Hot Swap Power Manager, Data Sheet (SLUS536)
3. LT1640AL/LT1640AH Negative Voltage Hot Swap Controller, Data Sheet; Linear Technology Corp. Literature No. 1640alahf.
4. Universal Telecommunication Hot Swap Family, Application Report (SLUA283)
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI’s standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifiers</td>
<td>amplifier.ti.com</td>
</tr>
<tr>
<td>Data Converters</td>
<td>dataconverter.ti.com</td>
</tr>
<tr>
<td>DSP</td>
<td>dsp.ti.com</td>
</tr>
<tr>
<td>Interface</td>
<td>interface.ti.com</td>
</tr>
<tr>
<td>Logic</td>
<td>logic.ti.com</td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>power.ti.com</td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>microcontroller.ti.com</td>
</tr>
<tr>
<td>Audio</td>
<td><a href="http://www.ti.com/audio">www.ti.com/audio</a></td>
</tr>
<tr>
<td>Automotive</td>
<td><a href="http://www.ti.com/automotive">www.ti.com/automotive</a></td>
</tr>
<tr>
<td>Broadband</td>
<td><a href="http://www.ti.com/broadband">www.ti.com/broadband</a></td>
</tr>
<tr>
<td>Digital Control</td>
<td><a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a></td>
</tr>
<tr>
<td>Military</td>
<td><a href="http://www.ti.com/military">www.ti.com/military</a></td>
</tr>
<tr>
<td>Optical Networking</td>
<td><a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a></td>
</tr>
<tr>
<td>Security</td>
<td><a href="http://www.ti.com/security">www.ti.com/security</a></td>
</tr>
<tr>
<td>Telephony</td>
<td><a href="http://www.ti.com/telephony">www.ti.com/telephony</a></td>
</tr>
<tr>
<td>Video &amp; Imaging</td>
<td><a href="http://www.ti.com/video">www.ti.com/video</a></td>
</tr>
<tr>
<td>Wireless</td>
<td><a href="http://www.ti.com/wireless">www.ti.com/wireless</a></td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated