Application Report
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Designing the Digital Compensator for a UCD91xx-Based Digital Power Supply

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ABSTRACT
This application report discusses a UCD91xx-based digital controller design for a high-frequency dc-dc switching power supply. Starting with a dc-dc buck converter power stage and a given set of performance specifications, different control blocks and parameters, used as in the analog control design approach, are reviewed prior to the digital controller design. The control loop is then analyzed and the digital controller is designed using the well-known PID controller template. Design examples are provided and validated with test results from prototype converters.

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1 Introduction
Digital control of switching power supplies is becoming more common in industry today. This technology is enabled by low-cost, high-performance digital PWM controllers with enhanced and integrated power conversion control peripherals such as high-speed error analog-to-digital converters (EADC), software-configurable digital voltage loop controllers or control law accelerators (CLA), and high-resolution digital pulse-width modulators (DPWM).

The UCD91xx family of digital pulse-width-modulation (PWM) controllers from Texas Instruments provides low-cost, high-performance digital control solutions for various types of power-supply applications. These digital PWM controllers are designed with various on-chip peripherals in order to implement high-bandwidth power supplies running at PWM frequencies of up to 1 MHz. These peripherals include a differential EADC with a 50-ns acquisition time; a CLA-based, digital PID compensator with two programmable coefficient lookup tables; a high-resolution, DPWM module with 175-ps duty-cycle resolution; and fault-counting, fast overcurrent protection.
For other system management functions, the UCD91xx depends on its 4-MHz microcontroller core with an on-chip oscillator; an 8-channel, 10-bit ADC; 24 general-purpose input-output (GPIO) ports; and communications peripherals such as PMBus, SMBus, and UART. These peripherals provide power supply designers with the benefits of digital control and allow the implementation of low-cost, high-bandwidth, high-frequency power supplies. To accelerate digital power supply application development, a user-friendly, graphical user interface (GUI) is provided for power designers using the UCD91xx controllers. This GUI allows designers to configure easily the UCD91xx and its digital compensator in order to implement essential power supply features and, at the same time, to meet the desired dynamic performance. Although the GUI provides a simple way to configure the digital compensator, power supply engineers who are primarily familiar with analog control design may want to explore the digital control design method that is integrated into the GUI-based development platforms. This application report presents details of this design method and allows the designers to review and gain insight into the various steps involved in designing digital PID controllers.

Digital PWM controllers have just recently received serious consideration for controlling power supplies. Therefore, pertinent factors in the design of a power-supply control loop must be revisited prior to their implementation in the digital domain. Accurate representation of the control blocks and the associated control parameters is critical for analog designers in order for them to analyze the digital control design method using the well-known analog control design approach. This application report, therefore, describes a step-by-step digital control design and implementation of a high-frequency, dc-dc power converter using the UCD91xx digital PWM controllers. Starting with a dc-dc buck converter and a given set of performance specifications, this document discusses different control blocks and then specifies a suitable PID controller in the s-domain. Following this, the s-domain PID controller is discretized to a z-domain controller using well-known s-to-z domain-mapping techniques. This approach to the digital control design is commonly known as design by emulation. Finally, design examples are provided and verified by experimental results.

2 Digital Control Implementation for DC-DC Converter

Figure 1 shows a simplified schematic of a digitally-controlled, dc-dc converter interfaced to a UCD91xx digital PWM controller. The dc-dc converter switching transistors are shown as Q1 and Q2. The input to the buck converter is \( V_{in} \) and its output is \( V_o \) with a load resistance of \( R_L \). The output filter inductor is \( L \). In Figure 1, \( R \) represents the equivalent dc resistance of the series combination of the inductor dc resistance and the on resistances of the switching transistors, Q1 and Q2. The output capacitors, C1 and C2, have ESRs denoted by \( R_{C1} \) and \( R_{C2} \), respectively. The equivalent series inductance (ESL) values of the output capacitors are denoted as \( L_{C1} \) and \( L_{C2} \), respectively. The UCD91xx PWM outputs drive the buck converter switching transistors through the gate-driver IC UCD7230.
The digital PWM controller measures the power-supply output voltage and implements the voltage-mode control loop of the power converter. The three essential elements in the UCD91xx PWM control loop are the EADC, the lookup-table-based digital PID controller (CLA), and the DPWM module. In Figure 1, the EADC, the CLA, and the DPWM module gains are indicated as $K_{ead}$, $G_C$, and $K_{dpwm}$, respectively. $G_{dly}$ represents the gain of the computation-delay block, which takes into account the effects of sampling and the computation delay in a digital control loop. The instantaneous output voltage $V_o$ is conditioned by the voltage-sense circuit and then input to the UCD91xx via the EADC channel. The EADC measures the error voltage $E$, given by $E = V_{out} - V_{ref}$. In order to maintain the negative feedback, the sign of the error voltage must be reversed before implementing the control loop. This reversal is done by generating the appropriate sign of the error voltage $E$ and storing the value in the CLA lookup table. For a positive error, $+E (= V_{out} - V_{ref})$, the UCD91xx CLA generates the control output by using the row of the lookup table that has the same error $E$ with the opposite sign. The digitized error voltage $-E$ is thus applied to the input of the CLA. The coefficients of the CLA are designed to make the scaled output voltage (Vout) track the reference (Vref) and, at the same time, achieve the desired dynamic performance. The digitized output U of the CLA provides the duty-ratio command for the on-chip digital PWM module. The DPWM module finally generates the PWM signal for the buck regulator switching transistors, Q1 and Q2.

3 DC-DC Controller Design

The design approach for digital-controllers is known as design by emulation or the digital redesign approach. In this method, an analog controller is first designed in the continuous-time domain as if one were building a continuous-time control system. The analog controller is then converted to a discrete-time compensator by an approximation technique. Figure 2 represents a simplified block diagram of the system in Figure 1. Figure 2 shows all the components of this closed-loop control system in the s-domain.
3.1 Power Stage Model \( G_p(s) \)

For the buck converter shown in Figure 1, the small signal output voltage to the PWM duty-ratio power-stage model \( (V_o/d) \), in s-domain, is indicated as \( G_p(s) \) in Figure 2. This power stage can be modeled with a single lumped output-filter capacitor branch or with multiple capacitor branches as shown in Figure 1.

3.1.1 \( G_p(s) \) with Lumped Output Capacitor C

For the lumped-capacitor branch, assume that \( C = C_1 + C_2 \), \( R_C = R_{C1} \times R_{C2}/(R_{C1} + R_{C2}) \) and \( L_{C1} = L_{C2} = 0 \), and then the power stage model is derived as

\[
G_p(s) = \frac{V_{in}(sR_C + 1)}{s^2L_C \times \frac{R_L + \frac{R_C}{R_L}}{R_L} + s \left( \frac{R_C}{R_L} \times \frac{R + \frac{R_L}{R_L} + L + RC}{R_L} + \frac{R + \frac{R_L}{R_L}}{R_L} \right)}
\]

\[
= V_{in} \times \frac{\frac{R_L}{R + \frac{R_L}{R_L}} \times \frac{(s/\omega_{ESR}) + 1}{(s^2/\omega_0^2) + s/(Q\omega_0) + 1}}
\]

(1)

where \( \omega_{ESR} \) is the output capacitor ESR zero frequency in rad/s; \( \omega_0 \) is the output LC filter cutoff frequency in rad/s; and \( R \) is the equivalent series resistance of the inductor dc resistance and the on-resistances of the converter switching transistors. The on-resistances are denoted as \( R_{ds1} \) and \( R_{ds2} \) for the switching transistors \( Q1 \) and \( Q2 \), respectively. Also, \( Q \) represents the combined \( Q \) factor of the LC filter and the output load. These parameters are derived as

\[
\omega_{ESR} = \frac{1}{R_C}, \omega_0 = \sqrt{\frac{R + \frac{R_L}{R_L}}{LC(R_L + R_C)}}, \quad R = DCR + d \times R_{ds1} + (1-d)R_{ds2}, \quad d = V_o / V_{in}
\]

\[
Q = \left( Q_{LOAD} \times Q_{LOSS} \right) / \left( Q_{LOAD} + Q_{LOSS} \right) = \frac{1}{\omega_0 \left( \frac{R_C}{R + \frac{R_L}{R_L}} + \frac{R_L}{R + \frac{R_L}{R_L}} \right)}
\]

\[
Q_{LOAD} = \left( R + \frac{R_L}{L} \right) \sqrt{\frac{C(R + \frac{R_C}{R})}{R + \frac{R_L}{R_L}}}, \quad Q_{LOSS} = \left( \frac{1}{R_C + \frac{R_L}{R + \frac{R_L}{R_L}}} \right) \sqrt{\frac{L(R + \frac{R_C}{R})}{C(R + \frac{R_L}{R_L})}}
\]

(2)
For \( R_C \ll R_L \) and \( R < R_L \), the simplified parameters can be written as

\[
\omega_{ESR} = \frac{1}{R_C C}, \quad \omega_0 = \frac{1}{\sqrt{LC}},
\]

\[
Q = \frac{Q_{LOAD} \times Q_{LOSS}}{Q_{LOAD} + Q_{LOSS}} = \frac{1}{\omega_0 (R_C C + L / R_L + RC)},
\]

\[
Q_{LOAD} = R_L \frac{C}{\sqrt{L}}, \quad Q_{LOSS} = \frac{\sqrt{L / C}}{R + R_C}
\]

(3)

### 3.1.2 \( G_p(s) \) With Multiple Output Capacitor Branches

To derive the power stage model for multiple capacitor branches with parasitic components, first define the impedance for the individual circuits. The filter inductor and the capacitor impedances are expressed as

\[
Z = R + sL
\]

\[
Z_{c1} = R_{c1} + sL_{c1} + \frac{1}{sC_1}, \quad Z_{c2} = R_{c2} + sL_{c2} + \frac{1}{sC_2}
\]

Then, the equivalent capacitor impedance is computed from

\[
Z_C = \frac{Z_{c1} \cdot Z_{c2}}{Z_{c1} + Z_{c2}}
\]

(4)

Therefore, the power stage model is

\[
G_p(s) = V_{in} \times \frac{Z_C \times R_L}{Z (Z_C + R_L) + Z_C \cdot R_L}
\]

(5)

### 3.2 Output-Voltage Sensing Gain \( K_{ead} \)

The output-voltage sensing gain \( K_{ead} \) models the gain from the power-supply output terminal to the EADC output. Thus, \( K_{ead} \) includes the EADC internal gain \( K_{ead} \) and the external voltage divider gain \( K_{div} \), which is used to scale the output voltage. This gain varies with the EADC and the external attenuator settings and is defined as

\[
K_{ead} = K_{ead} \cdot K_{div} = K_{ead} (V_{out} / V_o)
\]

(6)

### 3.3 DPWM Modulator Gain \( K_{dpwm} \)

The DPWM module gain \( K_{dpwm} \) is defined as

\[
K_{dpwm} = \frac{1}{2^{n_{pwm}} - 1}
\]

(8)

where \( n_{pwm} \) is the bit resolution of the selected DPWM channel in the UCD91xx for the specified PWM frequency. UCD91xx digital PWM controllers have a proprietary high-resolution PWM implementation with a duty-cycle time resolution of 175 ps. Therefore, the PWM bit resolution is calculated as

\[
n_{pwm} = \log_2 \left( 10^{12} \times t_{pwm} / 175 \right)
\]

(9)

where \( t_{pwm} \) is the PWM time period in seconds corresponding to the PWM switching frequency \( f_{pwm} \). For calculating the UCD91xx-based digital controller coefficients, initially assume unity gain for the EADC and the DPWM module (\( K_{ead} = 1, K_{dpwm} = 1 \)) and then design the digital PID controller. After the initial values of the coefficients of the digital PID are determined, they are then scaled appropriately by taking into account the actual values of \( K_{ead} \) and \( K_{dpwm} \) in the loop gain equation.
3.4 The Computation Delay $G_{dly}$

The gain of the computation delay block is given by

$$G_{dly}(s) = e^{-\theta_d} \tag{10}$$

where $\theta_d$ is the time delay associated with the EADC sampling, CLA computation, and DPWM duty ratio update, as illustrated in Figure 3.

![Computation Delay in UCD91xx Digital Control Loop](image)

This time delay causes an additional phase lag in the control loop. This phase lag, in degrees, is calculated as

$$\theta_{dly} = -360 \times f \times \theta_d \tag{11}$$

3.5 Continuous-Time PID Controller $G_C(s)$

The controller $G_C(s)$ in Figure 2 represents the s-domain counterpart of the z-domain controller, or the digital controller, in the UCD91xx digital PWM ICs. $G_C(s)$ is designed to achieve a desired control-loop bandwidth and dynamic performance of the power supply. For UCD91xx, the digital controller $G_C(z)$, (that is, the CLA) has been implemented in the digital PID format. Therefore, the z-domain transfer function and the discrete-time difference equation is given by

$$G_C(z) = \frac{U}{E} = \frac{b_0 z^2 + b_1 z + b_2}{z(z - 1)}$$

$$\Rightarrow U(n) = U(n-1) + b_0 \times E(n) + b_1 \times E(n-1) + b_2 \times E(n-2) \tag{12}$$

To determine the coefficients $b_0$, $b_1$, and $b_2$ of this digital PID controller, first choose the template for the continuous-time PID compensator. This compensator can be chosen in two different forms: (Case 1) PID controller $G_C(s)$ with complex s-plane zeros and (Case 2) PID controller $G_C(s)$ with real s-plane zeros.
Case 1:
The PID controller with complex s-plane zeros can be written as

\[
G_c(s) = \frac{U}{E} = \frac{\omega_k}{s} \times \left( \frac{s^2 + \omega_z^2}{\omega_z^2 + Q_c\omega_z} + 1 \right) = \frac{\omega_k}{s\omega_z^2} \times (s + \alpha + j\beta)(s + \alpha - j\beta)
\]

(13)

where the pair of complex zeros of the compensator on the complex s-plane is at \(s_1 = -\alpha + j\beta\) and \(s_2 = -\alpha - j\beta\). The real and imaginary parts of these complex zeros are given by

\[
\alpha = \frac{\pi f_z}{Q_c}, \quad \beta = 2\pi f_z \sqrt{1 - \frac{1}{4Q_c^2}}
\]

(14)

The magnitude of both compensator zero frequencies is \(\omega_z\) where \(\omega_z = 2\pi f_z\), \(\omega_z\) is in rad/s and \(f_z\) is in Hz. The frequency \(f_z\) is chosen slightly below the corner frequency of the LC filter to provide the necessary phase lead. The compensator quality factor \(Q_c\) is chosen to be comparable to the power stage \(Q\) at maximum load current. When using complex zeros, \(Q_c\) should also satisfy the condition \(Q_c > 0.5\). The term \(\omega_k\) represents the integral gain of the PID. This gain is adjusted to achieve the desired crossover frequency of the power-supply control loop. If the desired crossover frequency is denoted as \(f_{COV}\) then

\[
s_{COV} = j2\pi f_{COV}
\]

(15)

Because the magnitude of the computation delay gain \(G_{dy}\) is unity, the required \(\omega_k\) is calculated by

\[
G_p(s) \bigg|_{s = s_{COV}} \times G_c(s) \bigg|_{s = s_{COV}} = 1
\]

\[
\Rightarrow \omega_k \bigg|_{s = s_{COV}} = \frac{s\omega_z^2}{(s + \alpha + j\beta)(s + \alpha - j\beta)} \times \frac{1}{G_p(s) \bigg|_{s = s_{COV}}}
\]

(16)

Case 2:
The PID controller with real s-plane zeros can be written as

\[
G_{Cr}(s) = \frac{U}{E} = \frac{\omega_kz}{s} \times (s + \omega_{z1})(s + \omega_{z2})
\]

(17)

where the real zeros of the compensator on the complex s-plane are given by

\[
s_1 = -\omega_{z1} = -2\pi f_{z1} \quad s_2 = -\omega_{z2} = -2\pi f_{z2}
\]

(18)

The magnitudes of the compensator zero frequencies \(f_{z1}\) and \(f_{z2}\) are usually chosen slightly below the corner frequency of the LC filter to provide the necessary phase lead. However, depending on the power stage design, these may have to be chosen differently to achieve the desired dynamic performance. The term \(\omega_{kr}\), in this case, represents the differential gain of the PID. This gain is adjusted to achieve the desired crossover frequency of the power supply control loop. For a desired crossover frequency of \(f_{COV}\), the required gain \(\omega_{kr}\) is calculated from

\[
G_p(s) \bigg|_{s = s_{COV}} \times G_{Cr}(s) \bigg|_{s = s_{COV}} = 1
\]

\[
\Rightarrow \omega_{kr} \bigg|_{s = s_{COV}} = \frac{s}{(s + \omega_{z1})(s + \omega_{z2})} \times \frac{1}{G_p(s) \bigg|_{s = s_{COV}}}
\]

(19)
3.6 Digital PID Controller \( G_C(z) \)

After the s-domain PID compensator parameters are chosen, the next step is to discretize \( G_C(s) \) to derive its discrete-time format before it is implemented using the UCD91xx CLA module.

For discretization, use the mapping

\[
    z = e^{st_s}
\]

(20)

where \( t_s \) represents the sampling period. For UCD91xx controllers, the sampling frequency and the PWM frequency are always the same. Hence, \( t_s \) is equal to the PWM period \( t_{pwm} \). Applying this transformation or mapping, the pair of s-plane zeros, \( s_1 \) and \( s_2 \), map to the corresponding z-domain locations, \( z_1 \) and \( z_2 \) as

\[
    z_1 = e^{s_1 t_s}, \quad z_2 = e^{s_2 t_s}
\]

(21)

For the two choices of the s-domain PID controller mentioned previously, the coefficients of the digital PID controller are calculated using a different set of equations, as explained in the following two cases.

**Case 1:**

For the PID controller with complex s-plane zeros, the corresponding z-domain zeros are mapped as

\[
    z_1 = e^{-\alpha t_s + j\beta t_s}, \quad z_2 = e^{-\alpha t_s - j\beta t_s}
\]

(22)

These zeros are the roots of the polynomial

\[
    (z - z_1)(z - z_2) = 0
\]

\[
    \Rightarrow z^2 - 2e^{-\alpha t_s} \cos(\beta t_s)z + e^{-2\alpha t_s} = 0
\]

(23)

The z-domain PID compensator and its discrete-time difference equation also can be written as

\[
    G_C(z) = \frac{U}{E} = K_C \frac{z^2 + k_1 z + k_2}{z(z - 1)}
\]

\[
    \Rightarrow U(n) = U(n-1) + K_C \times E(n) + K_C \times k_1 \times E(n-1) + K_C \times k_2 \times E(n-2)
\]

(24)

where, \( K_C \) is the gain of the compensator. The coefficients \( k_1 \) and \( k_2 \) determine the zeros of the compensator. These zeros are given by the roots of the polynomial

\[
    z^2 + k_1 z + k_2 = 0
\]

(25)

Comparing this equation with the last polynomial, the z-domain PID coefficients are defined in terms of s-domain PID parameters as

\[
    k_1 = -2e^{-\alpha t_s} \times \cos(\beta t_s), \quad k_2 = e^{-2\alpha t_s}
\]

(26)

The gain \( K_C \) of the z-domain PID is selected such that the magnitudes of \( G_C(s) \) and \( G_C(z) \) are the same at the desired loop crossover frequency. Denoting the crossover frequency as \( f_{cov} \) yields

\[
    s_{cov} = j2\pi f_{cov}, \quad z_{cov} = e^{j2\pi f_{cov} t_s}
\]

(27)

Therefore, \( K_C \) is calculated from

\[
    G_C(z) \big|_{z = z_{cov}} = \frac{G_C(s)}{s = s_{cov}}
\]

\[
    \Rightarrow K_C = \frac{z(z - 1)}{z^2 + k_1 z + k_2} \big|_{z = z_{cov}} \times \frac{G_C(s)}{s = s_{cov}}
\]

(28)

After \( K_C \) is determined based on the loop crossover frequency requirements, the final coefficients of the UCD91xx CLA, taking into account the actual values of \( K_{fdbk} \) and \( K_{dpwm} \), are calculated as

\[
    b_0 = K_C \left( K_{fdbk} \times K_{dpwm} \right)
\]

\[
    b_1 = K_C \times k_1 \left( K_{fdbk} \times K_{dpwm} \right)
\]

\[
    b_2 = K_C \times k_2 \left( K_{fdbk} \times K_{dpwm} \right)
\]

(29)
Case 2:
For a PID controller with real s-plane zeros, the corresponding z-domain zeros are mapped to
\[ z_1 = e^{-\omega z_1 t_s}, \quad z_2 = e^{-\omega z_2 t_s} \]  
(30)

These zeros are the roots of the polynomial
\[ (z - z_1)(z - z_2) = 0 \]
\[ \Rightarrow z^2 - (e^{-\omega z_1 t_s} + e^{-\omega z_2 t_s})z + e^{-(\omega z_1 + \omega z_2) t_s} = 0 \]  
(31)
The z-domain PID compensator and its discrete-time difference equation is written as
\[ G_{Cr}(z) = \frac{U}{E} = K_{Cr} \frac{z^2 + k_1 z + k_2 r}{z(z - 1)} \]
\[ \Rightarrow U(n) = U(n - 1) + K_{Cr} \times E(n) + K_{Cr} \times k_1 r \times E(n - 1) + K_{Cr} \times k_2 r \times E(n - 2) \]  
(32)
Following the same procedure as in case 1, the z-domain PID coefficients are defined in terms of s-domain PID parameters as
\[ k_{1r} = -(e^{-\omega z_1 t_s} + e^{-\omega z_2 t_s}), \quad k_{2r} = e^{-(\omega z_1 + \omega z_2) t_s} \]  
(33)
For a crossover frequency of \( f_{COV} \), the gain \( K_{Cr} \) of the digital PID is calculated from
\[ K_{Cr} = \left| \frac{z(z - 1)}{z^2 + k_{1r} z + k_{2r}} \right|_{z = z_{COV}} \times G_{Cr}(s) \bigg|_{s = s_{COV}} \]  
(34)
Taking into account the actual values of \( K_{fdbk} \) and \( K_{dpwm} \), the final coefficients of the UCD91xx CLA, are calculated as
\[ b_0 = K_{Cr} / (K_{fdbk} \times K_{dpwm}), \]
\[ b_1 = K_{Cr} \times k_{1r} / (K_{fdbk} \times K_{dpwm}), \]
\[ b_2 = K_{Cr} \times k_{2r} / (K_{fdbk} \times K_{dpwm}) \]  
(35)
UCD91xx error ADC converted outputs can have one of 17 levels (-8 to +8, including 0). These errors (-8 ~ +8) are multiplied by the CLA coefficients and stored in memory. Thus, \( b_0 \) is multiplied by the most recent error \( E(n) \), and the 17 possible combinations are stored in memory as one of the three columns of the CLA table. The second and third columns of the CLA table contain the product terms \( b_1 \times E(n - 1) \) and \( b_2 \times E(n - 2) \), respectively, each having 17 entries. Thus, one complete CLA table contains 51 entries of the product terms. The UCD91xx has two such lookup tables for its CLA.
4 Design Example

Case 1:
The system parameters used in this design are
- \( V_{in} = 8 \text{ V} - 12 \text{ V}, V_{out} = 1.8 \text{ V} \), maximum output current \( I_{out} = 20 \text{ A} \), \( R_L = V_{out}/I_{out} = 0.09 \Omega \) (minimum)
- EADC resolution \( V_{ead} = 5 \text{ mV} \Rightarrow K_{ead} = 1/V_{ead} = 200 \), \( K_{div} = 1/1.6 \)
- PWM frequency \( f_{pwm} = 500 \text{ kHz} \); \( R_{ds1} = R_{ds2} = 0 \)
- The computation delay \( t_d = 0.5 \text{ } f_{pwm} = 1.0 \times 10^{-6} \text{ s} \)
- Output filter components: \( L = 1 \mu \text{H}, R = DCR = 0.897 \text{ m}\Omega, C = 110 \mu \text{F}, R_C = 2 \text{ m}\Omega \)
- Desired voltage-loop bandwidth or crossover frequency \( f_{COV} = 65 \text{ kHz} \)
- Minimum phase margin = 45°

For \( V_{in} = 12 \text{ V} \), the power-stage parameters and transfer function are calculated as
\[
\omega_{ESR} = 4.5455 \times 10^6 \text{ rad/s}, \quad \omega_0 = 9.4773 \times 10^4, \quad Q = 0.9322
\]
\[
G_p(s) = \frac{11.88 \times 0.22 	imes 10^{-6}}{1 + 1.113 \times 10^{-16} s^2 + 1.132 \times 10^{-5} s + 1}
\]

The sensing gain is computed as
\[
K_{fbk} = K_{ead} \times K_{div} = 125
\]

The DPWM module gain is calculated as
\[
K_{dpwm} = 8.751 \times 10^{-5}
\]

To design the \( s \)-domain PID controller, start with the zero frequency selection of the controller. Choose the magnitude of the complex zero frequencies slightly below the corner frequency of the LC filter to provide the necessary phase lead. Therefore, set
\[
f_z = 0.8 \times f_0 = 0.8 \times \omega_0 / (2 \times \pi) = 1.2067 \times 10^4
\]

The controller Q-factor \( Q_c \) is made comparable to power stage \( Q \). Therefore, set \( Q_c = 1 = Q \). Thus, the real and imaginary parts of the PID controller complex zeros in \( s \)-plane are calculated as
\[
\alpha = 3.7909 \times 10^4, \quad \beta = 6.5661 \times 10^4
\]

To calculate the integral gain \( \omega_k \) of the PID controller, substitute \( s_{COV} = j6.2832 f_{COV} = j4.0841 \times 10^5 \) in the following equation:
\[
\omega_k = \frac{s \omega^2}{(s + \alpha + j\beta)(s + \alpha - j\beta)} \bigg|_{s = s_{COV}} \times \frac{1}{G_p(s)} \bigg|_{s = s_{COV}}
\]
\[
= 14315.37 \times \frac{1}{0.6566} = 2.1802 \times 10^4
\]

Thus the \( s \)-domain PID controller is
\[
G_C(s) = 3.793 \times 10^{-6}s^2 + 0.2876s + 21802
\]

The coefficients of the corresponding \( z \)-domain PID controller are calculated as
\[
k_1 = -1.838, \quad k_2 = 0.8593
\]

To calculate the gain \( K_C \) of the \( z \)-domain PID controller, substitute \( s_{COV} = j6.2832 f_{COV} = j4.0841 \times 10^5 \) and \( z_{COV} = \exp(j4.0841 \times 10^5 t_d) = \exp(j0.8168) \) in the following equation:
\[
K_C = \left[ \frac{z(z - 1)}{z^2 + k_1z + k_2} \right]_{z = z_{COV}} \times G_C(s) \bigg|_{s = s_{COV}}
\]
\[
= 1.3827 \times 1.523 = 2.1058
\]
Finally, the coefficients of the UCD91xx CLA are calculated as
\[ b_0 = 193, \quad b_1 = -354, \quad b_2 = 165 \]  
(46)

Thus, for this example, UCD91xx CLA executes the following digital controller:
\[ U(n) = U(n - 1) + 193 \times E(n) - 354 \times E(n - 1) + 165 \times E(n - 2) \]  
(47)

The discrete-time system loop-gain Bode plot for this controller at full load is shown in Figure 4.

![Bode Diagram](image)

**Figure 4. Discrete-Time System Loop-Gain Bode Plot (BW = 63.5 kHz, PM = 53.8°, GM = 10.3 dB)**

The Bode plot shows that the digital controller achieves a loop bandwidth of 63.5 kHz with a phase margin of 53.8° and a gain margin of 10.3 dB.

**Case 2:**
The system parameters used in this case are
- \( V_{in} = 8 \text{ V} \rightarrow 12 \text{ V}, \ V_{out} = 1.5 \text{ V}, \ I_{out} \text{ (max)} = 40 \text{ A}, \ R_L = V_{out}/I_{out} = 0.0375 \Omega \) (minimum)
- EADC resolution \( V_{ead} = 5 \text{ mV} \Rightarrow K_{ead} = 1/V_{ead} = 200, \ K_{div} = 1/1.604 \)
- PWM frequency \( f_{pwm} = 600 \text{ kHz} \)
- The computation delay = \( t_d = 0.24 \times t_{pwm} = 0.4 \times 10^{-6} \text{ s} \)
- Output filter components, \( L = 0.5 \mu\text{H}, \ DCR = 0.6 \text{ m}\Omega, \ R_{ds_{on_{lo}}} = R_{ds_{on_{hi}}} = 2.2 \text{ m}\Omega \)
- \( C = 3100 \mu\text{F}, \ R_C = 5 \text{ m}\Omega \)
- Desired voltage-loop bandwidth or crossover frequency \( f_{COV} = 70 \text{ kHz} \)
- Minimum phase margin = 45°

For \( V_{in} = 10 \text{ V} \), the power-stage parameters and transfer function are calculated as
\[ \omega_{ESR} = 6.4516 \times 10^4 \text{rad/s}, \ \omega_0 = 2.4734 \times 10^4, \ Q = 1.1236 \]  
(48)

\[ G_P(s) = \frac{144.2 \times 10^{-6}s + 9.305}{1.635 \times 10^{-9}s^2 + 3.598 \times 10^{-5}s + 1} \]  
(49)

The sensing gain is computed as
\[ K_{fbk} = K_{ead} \times K_{div} = 124.69 \]  
(50)
Design Example

The DPWM module gain is calculated as

$$K_{dpwm} = 1.05 \times 10^{-4}$$  \hspace{1cm} (51)

The two real zero frequencies of the s-domain PID controller are chosen as

$$f_{z1} = 2800.0 \text{ Hz}, \quad f_{z2} = 100,000.00 \text{ Hz}$$  \hspace{1cm} (52)

To calculate the gain $\omega_{kr}$ of the PID controller, substitute $s_{COV} = j6.2832f_{COV}$ in the following equation:

$$\omega_{kr} = \frac{s}{(s + \omega_{z1})(s + \omega_{z2})} \bigg|_{s = s_{COV}} \times \frac{1}{G_p(s)} \bigg|_{s = s_{COV}}$$  \hspace{1cm} (53)

Thus, the s-domain PID controller is

$$G_C(s) = \frac{1}{s} \times \left(6.413 \times 10^{-6} s^2 + 4.142s + 7.089 \times 10^4\right)$$  \hspace{1cm} (54)

The coefficients of the corresponding z-domain PID controller are calculated as

$$k_{1r} = -1.322, \quad k_{2r} = 0.3408$$  \hspace{1cm} (55)

To calculate the gain $K_{Cr}$ of the z-domain PID controller, substitute $s_{COV} = j6.2832f_{COV}$, and $z_{COV} = \exp(j6.2832f_{COV}Ts)$ in the following equation:

$$K_{Cr} = \frac{z(z-1)}{z^2 + k_1z + k_2} \bigg|_{z = z_{COV}} \times G_C(s) \bigg|_{s = s_{COV}}$$  \hspace{1cm} (56)

Finally, the coefficients of the UCD91xx CLA are calculated as

$$b_0 = 491.45, \quad b_1 = -649.71, \quad b_2 = 167.48$$  \hspace{1cm} (57)

Thus, for this example, the UCD91xx CLA executes the following digital controller:

$$U(n) = U(n-1) + 492 \times E(n) - 650 \times E(n-1) + 168 \times E(n-2)$$  \hspace{1cm} (58)

The discrete-time system loop-gain Bode plot for this controller at full load is shown in Figure 5. The bandwidth and the phase margin from this plot are 69 kHz and 70°, respectively. Figure 6 and Figure 7 show the output voltage transient response for a load step of 20 A. The response shows a transient settling time of about 25 µs.
Figure 5. Discrete-Time System Loop-Gain Bode Plot (BW = 69 kHz, PM = 70°, GM = 9 dB)

Figure 6. Output Voltage Transient Response (Load Step 10 A to 30 A to 10 A, Slew Rate 1 A/µs)

Figure 7. Output Voltage Transient Response (Load Step 10 A to 30 A, Slew Rate 1 A/µs)
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