A Robust Solution for 100-A Hot Swap of 12-V Supply Rails

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ABSTRACT

As intermediate bus voltages decrease, a corresponding increase in line card load currents further complicates the design of power distribution and control sub-systems in networking equipment. As one part of the overall power system, designers need a hot swap solution capable of performing its required functions while reliably surviving both normal module operation and fault conditions. But as load currents reach 60 A, 80 A, or even more, protecting power supplies on one end, loads on the other end, and the pass FET’s between them becomes increasingly tricky.

This application note presents one solution for robust hot swap of such a high-current plug-in module, operating at a nominal 12-V input, with a 100-A fault trip threshold. The solution schematic is given, along with component selection criteria and equations, such that the reader can appropriately scale the solution to his own requirements. The document also provides several scope waveform captures from an actual implementation, under various operating scenarios.

1 Introduction

As intermediate bus voltages decrease, a corresponding increase in line card load currents further complicates the design of power distribution and control sub-systems in networking equipment. In some applications, 24-V and even 12-V primary power busses have replaced the historical 48-V supplies or batteries. Blade servers are one example of systems migrating to these lower bus voltages. One function adversely impacted by this migration is the hot swap capability crucial to meeting the high up-time ratios required of these systems. As load rail currents reach 40, 50 and even 80 A, the details of the hot swap circuit design become ever more critical.

Hot swap solutions for these applications are faced with a variety of technical issues. A number of integrated 12-V controllers are available on the market, but many have insufficient pin voltage ratings to survive the large transients which can be encountered when interrupting such high currents. The high currents drawn by line and interface cards, which can be upwards of 80 A, suggest parallel FET’s to reduce the I²R losses and dissipate the associated heat. However, the nuances of paralleling FET’s must be understood, especially if the FET’s will be periodically subjected to linear mode operation, such as during inrush limiting. With some controllers, insufficient gate drive voltage leads to greater-than-optimal $R_{DS(on)}$ Characteristics for the selected FET type.

This application note presents a hot swap solution which addresses these issues and many more.
2 A 12-V, High-Current Solution

The hot swap circuit presented here is based on the Texas Instruments (TI) TPS2490 High-Voltage Hot Swap Controller integrated circuit. Designed as a hot swap controller for positive 48-V systems, its wide operating voltage range makes it suitable for controlling a 12-V rail. The 100-V absolute maximum pin voltage rating exceeds realistic needs; however, with a shortage of suitably-rated devices available between the 12-V and 48-V application spaces, this rating makes it extremely robust in this low-voltage/high-current environment. Also, the typical 14-V gate drive voltage, (gate-to-source, or output ) fully enhances the pass FET’s, ensuring the application achieves the FET manufacturer’s advertised R\textsubscript{DS(on)} characteristic.

The solution schematic is shown in Figure 1.

In the schematic, the TPS2490 is shown controlling five IRL7843 N-Channel MOSFET’s. The number and type of pass FET is easily tailored to the load requirements of the target application. Load current magnitude is fed to the TPS2490 SNS pin via the scaling network of R1, R2 and R3. The current sense network determines the circuit threshold for fault current detection and limiting. Other circuit parameters (turn-on voltage threshold, fault timer interval) are programmed by the passives to the left of the U1 symbol (i.e., R7, R8, R9, C1). Output sensing, inrush control, and a fast gate pull-down circuit are to the right (i.e., Q6, R17, C3, D2, R23, and Q7). The details of component selection and sub-circuit operation are discussed in detail in later sections of this document. Finally, the bank of large capacitors connected across the output (P12V) to GND (C5 – C10) represents the load capacitance which may be present as the input bulk capacitance of downstream circuitry, such as Point-of-Load (POL) converters.

3 Design Requirements

The circuit presented in Figure 1 was designed for the following system requirements and load description:

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input supply voltage, V\textsubscript{IN}</td>
<td>12 V, 10%</td>
</tr>
<tr>
<td>Maximum steady-state load, I\textsubscript{L(max)}</td>
<td>80 A</td>
</tr>
<tr>
<td>Load input bulk capacitance</td>
<td>10,000 (\mu)F, (\pm) 20%</td>
</tr>
<tr>
<td>Output turn-on threshold</td>
<td>10.5 V maximum</td>
</tr>
<tr>
<td>Logic-level PowerGood (PG) output</td>
<td>active-high, LVC/ALVC CMOS compatible, 3.3-V system</td>
</tr>
<tr>
<td>Max. ambient operating temperature</td>
<td>60°C</td>
</tr>
<tr>
<td>No external heat sinks</td>
<td></td>
</tr>
</tbody>
</table>
Figure 1. TPS2490 12-V, High-Current Hot Swap Schematic
4 Preliminary Design Considerations -- Inrush Control Scheme

Given the high current which the hot swap circuit must be able to source, some thought should be given up front to what type of inrush control scheme to use. Control methods basically fall into two main categories; constant current, in which the pass FET is operated as a limited current source, and voltage mode (or dV/dt), in which the load voltage rate of rise is controlled in such a manner that the resultant bulk cap charging current is limited below a pre-determined level. There are of course variants of each type.

Traditional constant-current controllers are beneficial in that they offer very predictable and repeatable current limiting, regardless of variations in input voltage or load capacitance, or the fault status of the load. They do have a drawback though, in that they must be allowed at start-up to operate at least long enough to account for the anticipated worst-case bulk charging time. For applications with high nominal input voltages, or large load capacitance, this may lead to setting extended fault time-out delays. Unfortunately, extended delay periods make it difficult to protect the pass FET(s) in other scenarios, such as turning on into a shorted load, or overcurrent faults during steady-state operation. So at least at first glance, one reason for selecting the TPS2490 for this application is that it adds pass FET V_{DS} sensing, and uses this information to vary the current limit threshold to maintain a constant power dissipation in the FET. This foldback mechanism protects the pass FET from excessive stresses in the case of a faulted load.

In order to set the limits for the internal constant-power engine, an appropriate dissipation limit must be established for the FET. Generally, this is done by considering the maximum operating junction temperature (T\text{J}) rating of the device, and selecting limit values to remain below that temperature at extremes of ambient operating temperature and load range. A number of thermal calculators, from simple spreadsheets to complex PCB thermal analysis tools, are available for this purpose. On the simpler side, one might consult the design procedure in the APPLICATION INFORMATION section of the TPS2490 data sheet[1]. Alternatively, an Excel spreadsheet calculator tool is available from TI which automates calculation of a FET transient power limit[2]. Links to these resources are listed in the reference section of this document. The reader is referred to these, as a determination of a dissipation limit is beyond the scope of this application note. However, Chapter A contains some important background information regarding the technique of using parallel FET’s to reduce overall R_{DS(on)}, and increase the dissipation capability of, the hot swap “switch”.

Applying the guidelines in Chapter A, a maximum transient dissipation limit of 48 W was established for this example design. This limit is based on the following FET selection and specifications:

<table>
<thead>
<tr>
<th>Table 2. FET Selection and Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PARAMETER</strong></td>
</tr>
<tr>
<td>FET type</td>
</tr>
<tr>
<td>Maximum junction temp, T\text{J(max)}</td>
</tr>
<tr>
<td>Maximum R_{DS(on)}</td>
</tr>
<tr>
<td>Package</td>
</tr>
<tr>
<td>Max. Thermal Impedance, J - A, R_{thA}</td>
</tr>
</tbody>
</table>

Using the equations in the TPS2490 data sheet, it was determined that a programming voltage of less than 50 mV must be applied to the PROG pin to establish the above power limit. Given normal device tolerances as stated in the data sheet, it was considered that the resultant power limit percent variation from board to board may be unacceptable. Therefore this circuit actually disables the constant power feature of the TPS2490, and configures the device in a dV/dt control scheme for turn-on events. The device’s current limiting control still manages load faults during subsequent steady-state operation. The 47-kΩ pull-up on the PROG input to the VREF pin disables power limiting.
5 Design Procedure

5.1 Setting the Fault Trip (Current Limit) Threshold

The load current sense signal is developed as the voltage drop across sense resistor R1, and applied across the VCC and SNS pins of the TPS2490. The TPS2490 has a fixed current limit threshold. The action of the internal control amplifier is to slew the pass FET gates to limit the sense voltage to this threshold, typically 50 mV. Despite the fixed device threshold, and even with a potentially limited set of discrete sense resistor values, a fine degree of limit resolution can still be achieved. If needed, the divider network of R2 and R3 can be used to scale the input to the TPS2490 to obtain the desired set point, which is demonstrated in the below design process.

The current sourcing limit should be selected to allow some margin over the steady-state load current for system noise and component tolerances. For this solution, a margin of 25% was chosen, for a nominal current limit of 100 A. The sense resistor value is then determined as:

\[
R1 = \frac{V_{SNS}}{I_{LIM}} = \frac{50 \text{mV}}{100 \text{A}} \times 0.5 \Omega
\]  

(1)

If the calculated value of sense resistor is not readily available, first determine an acceptable combination resulting in a somewhat higher equivalent resistance. For example, the four (4) 3-mΩ sense resistors shown in the Figure 1 schematic yield an effective 0.75-mΩ sense resistor. Resistors R2 and R3 are then selected to scale the voltage applied to the TPS2490 inputs. Referring to Figure 1, the voltage across R2 is applied to the TPS2490 pins, so the divider equation yields:

\[
R2 = \frac{V_{SNS}}{V_{SNS1} - V_{SNS}} \times R3 = \frac{V_{SNS}}{I_{LIM} \times R1 - V_{SNS}} \times R3
\]  

(2)

Where:
- \(V_{SNS}\) is the TPS2490 internal threshold (50 mV nominal)
- \(V_{SNS1}\) is the drop across element R1, in mV, and
- \(I_{LIM}\) is the desired sourcing limit in amps.

Note that SNS pin bias current through resistor R2 produces an error component in the measured current. Therefore, the divider impedance must be kept low in order to minimize this error contribution. As a general guideline, an overall impedance of 100 Ω or less is good. For this example, setting R3 to 20 Ω, 1% value produces an R2 value of 40 Ω. The 1% value of 39.2 Ω was selected.
Once the actual resistor values are selected, it’s a good practice to calculate the worst-case minimum threshold that may be encountered, accounting for sense resistor and TPS2490 threshold tolerances. This minimum sourcing level must be greater than the maximum load to prevent unwanted limiting operation (and potential load shutdown) during normal operation of the card. For the sense voltage divider configuration, this minimum current is given by Equation 3.

\[
I_{\text{LIM(min)}} = \frac{V_{\text{LIM(min)}}}{R_{1\text{MAX}}} = \frac{(V_{\text{SNS(min)}} - I_{\text{BIAS}} \times R_{2\text{MAX}})}{R_{1\text{MAX}}} \times A_{\text{DIV}}
\]

Where:
- \(I_{\text{LIM(min)}}\) is the minimum sourcing level of the circuit, in amps,
- \(V_{\text{SNS(min)}}\) is the TPS2490 minimum current sense threshold,
- \(R_{1\text{MAX}}\) is the maximum sense resistor value, in milliohms, and
- \(A_{\text{DIV}}\) is the gain of the divider.

The TPS2490 data sheet specifies \(V_{\text{SNS(min)}}\) (without power limiting) to be 45 mV; the sense pin bias current is 7.5 µA typical, 20 µA maximum. Substituting the circuit values into Equation 3 yields Equation 4:

\[
I_{\text{LIM(min)}} = \frac{[45\text{mV} - (20\mu\text{A}) \times (1.01) \times (39.2\Omega)]}{(39.2/59.2)} \\
= \frac{(1.01) \times (0.75m\Omega)}{88.1A}
\]

Even with the (1%) resistor tolerances applied to the divider factor in the above, Equation 4 still returns a result of 87.56 A, indicating sufficient margin exists over the expected load.

### 5.2 Establishing the Inrush Limit

This section discusses the procedure for choosing the value of the gate capacitor (C3 in Figure 1) to set the inrush current limit. The circuit charges up the load bulk capacitance by ramping the common FET gates node at a constant rate, with the sources following by one \(V_{\text{OS}}\) drop. A maximum charging current is established according to the primary application criteria. Then, the rate of rise is limited to maintain the sourced current below this maximum. The calculation process works by considering that turning on the load in this fashion requires delivering a certain amount of charge to the FETs' gate capacitance in a fixed amount of time. The fact that multiple FET’s are paralleled, due to steady-state dissipation requirements, is actually beneficial with this method, due to the amount of capacitance already present on the node. The maximum rate at which charge can be delivered by the TPS2490 is considered, and if needed, C3 is selected as an additional reservoir in which to dump charge.

As discussed earlier, the dominant criteria in selecting the inrush current limit was to limit the power dissipated in any one of the pass FET’s to 48 W during turn-on events. Assuming constant-current charging of the load bulk capacitance (a reasonable approximation), the instantaneous FET dissipation will start at some quantity \(P_{\text{MAX}}\), then decay linearly (with decreasing \(V_{\text{DS}}\)), to zero watts at the end of the ramp period. Therefore, the average dissipation during start-up can be simplistically represented as:

\[
P_{\text{AVG}} = \frac{P_{\text{MAX}} + 0}{2}
\]

This relationship indicates an allowable peak power of \(P_{\text{MAX}} = 2 \times P_{\text{AVG}}\), or 96 W.

Since, for a given current through the FET, the worst-case stress will occur at the maximum drain-to-source voltage, the maximum supply condition was used to establish the current limit. So this maximum current was set to \(I_{\text{MAX}} = \frac{P_{\text{MAX}}}{V_{\text{MAX}} = 96\text{ W} / 13.2\text{ V}}\), or 7.27 A. For a primarily capacitive load at start-up, the time required to charge the load cap at this rate, \(t_{\text{ON}}\), is given by Equation 6.

\[
t_{\text{ON}} = \frac{C_{\text{LOAD}} \times dV_{\text{OUT}}}{I_{\text{MAX}}}
\]
If the downstream load on the hot swap circuit is better modeled as an RC-type load (at load turn-on), Equation 7 is an alternate form which may more accurately estimate the start-up time, $t_{ON}$. However, the designer must take precautions that a certain fundamental relationship is maintained. If the resistive component of the load model is such that $V_{IN(max)}/R_{LOAD} > I_{MAX}$, the implication is that the current-limited source cannot develop the input supply potential across the load. The programmed sourcing limit may be exceeded in order to fully charge the load.

$$
t_{ON} = (-1) \times R_{LOAD} \times C_{LOAD} \times \ln \left[ \frac{I_{MAX} \times R_{LOAD} - dV_{OUT}}{I_{MAX} \times R_{LOAD}} \right]
$$

Equation 7

For this design, with the use of the circuit PWRGOOD output to enable downstream converters, the load was considered primarily capacitive. For the nominal supply voltage of 12 V (and therefore, $dV_{OUT} = 12$ V), Equation 6 returns an interval of $t_{ON} = 16.5$ ms. To keep actual, in-circuit dissipation conservative relative to calculated results, the target start-up interval was rounded up to 20 ms.

Referring to the IRLR7843 data sheet, the typical gate charge curve shows a total gate charge, from 0 V to the end of the plateau at $V_{GS} \approx 3$ V, of 30 nC. (A rough interpolation is fine for this calculation.) Also, to maintain this $V_{GS}$ throughout the output ramp-up event, the gate will have to be ramped to 12 V + 3 V = 15 V. Summing the charge that must be delivered to bring up the load, and equating that to the maximum charge that could be delivered by the TPS490, the relationship can be rewritten to determine the minimum external gate capacitance needed to limit the ramp-up rate. The result is Equation 8.

$$
C_{EXT} = \frac{i_{CHG(max)} \times t_{ON} - dQ_{G}}{dV_{G}}
$$

Equation 8

Where:

- $i_{CHG(max)}$ is the maximum sourcing current of the TPS2490 GATE pin, 35 $\mu$A per the data sheet,
- $t_{ON}$ is the calculated start-up interval from Equation 6 or Equation 7, as adjusted,
- $dQ_{G}$ is the total FET gate charge, and
- $dV_{G}$ is the delta-V at the common gates node during the output ramp.

Substituting the application values into Equation 8 produces:

$$
C_{EXT} = \frac{[35\mu A \times (20mS) - 5 \times 30nC]}{15V} = 0.037 \mu F
$$

Equation 9

The next higher standard available value of 0.047 $\mu$F was selected for C3.
Figure 2 is a scope capture of a circuit turn-on event from the TPS2490 EN pin assertion (TP5 node in Figure 1), with a nominal 12-V input supply potential. The test load, as shown in Figure 1, was 12,000 μF, to look at performance allowing for the 20% bulk capacitor tolerance indicated in the design specification.

Figure 2. Start-Up Event Into 12,000-μF Load, From EN Pin Assertion.

Note that the circuit maintains a constant current to the load during bulk capacitor charging (inrush current). The current limit level was about 4.4 A, significantly lower than the target of 7.27 A. Accordingly, the load ramp-up time, from 0 V to 12 V, was measured (with scope cursors, not shown) to be slower than the targeted interval, at 32.4 ms. The bulk of this difference can be attributed to the C3 selected value 27% larger than the calculated result, and what's most likely a much more nominal GATE pin sourced current versus the maximum value used. This shows the level of conservatism built into the component selection, and one could even argue that there’s margin to reduce the value of C3. On the other hand, the start-up waveforms clearly demonstrate that inrush current is managed to such a benign level that it’s easily handled by any one of the five FET's, even after operation at elevated junction temperatures.
5.3 **Circuit UVLO Considerations and Threshold**

The input voltage range in this application is such that the TPS2490 is operated fairly close to its own supply UVLO threshold. Experience has shown that, in a situation of decreasing supply voltage, the output shutdown action is more definitive if performed prior to reaching the VCC UVLO, as opposed to relying on the UVLO shutdown response. The solution uses the device enable pin (EN) with the resistive divider of R7 and R8 to establish a circuit UVLO threshold. The design goal then was to keep the minimum falling UV threshold, as established by the EN pin, above the maximum VCC falling UVLO threshold. Note that the TPS2490 data sheet does not specify a maximum limit for the “V\text{VCC turn off}” parameter, nor a minimum hysteresis for this pin. Without these specifications, one way to guardband the external programmed threshold is to use the maximum “V\text{VCC turn on}” limit, 8.8 V; the input falling threshold has to be less than that.

A value for resistor R8 is calculated from Equation 10.

\[
R8 = \frac{V_{EN \_L}}{V_{UVF(12V)} - V_{EN \_L}} \times R7
\]  

(10)

Where:
- \(V_{EN \_L}\) is the EN pin switching threshold, for falling input voltage, 1.22 V min., and
- \(V_{UVF(12V)}\) is the desired UV threshold at the input supply rail.

To calculate the divider string values, a secondary guideline is to establish a minimum divider load of 50 \(\mu\)A, as this minimizes errors due to EN pin bias current. For this application, this translates to a total divider impedance of less than 170 k\(\Omega\) (at 8.5 V). With R7 set to 76.8 k\(\Omega\), and using the voltage values indicated above, this produces a value for R8 of 12.36 k\(\Omega\). By opting for the closest value less than the calculated result, the minimum \(V_{UVF(12V)}\) threshold is kept above the target value.
5.4 Setting the Fault Timeout Period

As discussed previously, one of the caveats of constant-current inrush control is that any fault timer must be set long enough to allow fully discharged bulk capacitance to charge during turn-on events. Conversely, a benefit of the dV/dt load ramp as used here is that the inrush limit can be set below the overload fault threshold. This can be beneficial in applications where a large amount of input bulk capacitance must be charged. Maintaining inrush below the fault threshold holds the timer off during start-up of a valid, non-faulted load. Therefore, fault time-out periods can be kept short enough to keep FET dissipation within the SOA rating of the FET, but long enough to avoid nuisance trips due to load surges or system noise. As always, the FET manufacturer’s data sheet should be consulted to verify applicable pulse duration limits will not be exceeded in the situation of a load short at the card’s operating voltage. Referring to the IRLR7843 data sheet Maximum Safe Operating Area graph, for a VDS of 10 V, safe operation limit is indicated as just over 100 A for up to 100 µs. Therefore, the fault time selected was a nominal 100 µs.

Since fault timing is accomplished by the constant-current charging of the external timing capacitor (C1) to a trip threshold, the timing capacitor value is determined from Equation 11.

\[ C_{FLT} = \frac{i_{CHG} \times t_{FLT}}{dV} \]

(11)

Where:
- \( C_{FLT} \) is the fault capacitor value,
- \( i_{CHG} \) is the TIMER pin sourced current during faults,
- \( t_{FLT} \) is the desired fault time-out period, in seconds and
- \( dV \) is the delta-V to be developed across the capacitor, charging from 0 V to the TPS2490 fault threshold.

TIMER pin current in µA returns a capacitor value in µF. Substituting the TPS2490 data sheet values into Equation 11 produces:

\[ C_{FLT} = \frac{(25 \mu A) \times (100 \mu S)}{4V} = 625pF \]

(12)

The next higher standard value of 680 pF was selected for C1.
5.5 Powergood Output Generation

The TPS2490 PG pin is an active-high, open-drain output which, after a deglitch delay, becomes high impedance when output voltage conditions meet the criteria. (Please refer to the TPS2490 data sheet.) The PG pin can be pulled up to essentially any available supply to generate the logic high output level. For this design, it was decided to use the 12-V output to provide the bias, and simply divide the voltage down for the desired signal levels.

The TPS2490 data sheet indicates an absolute maximum sink current for this pin of 10 mA. For the maximum input supply in this application of 13.2 V, this limit suggests a minimum value for R18 of around 1400 Ω (allowing for a 5 % tolerance). Setting R18 to 8.2 kΩ sets a nominal output current of about 1.5 mA.

Presuming this output should remain a valid logic high level down to the minimum circuit UVLO voltage, then the value of the bottom leg of the divider can be calculated from:

\[
R_{19\,\text{MIN}} = \frac{V_{\text{OH}(\text{min})}}{V_{P\,12\,\text{V}(\text{min})} - V_{\text{OH}(\text{min})}} \times R_{18}
\]

(13)

Where:

- \( V_{\text{OH}} \) is the high-level output voltage of the PWRGOOD signal, and
- \( V_{P\,12\,\text{V}} \) is the output voltage rail potential.

Substituting in a minimum \( V_{\text{OH}} \) of 2 V, and the minimum UV threshold of 8.8 V as designed in Section 5.3, Equation 13 returns a value of 2.4 kΩ for R19. R19 was set to 3 kΩ to provide some margin above the absolute minimum input voltage requirement for the selected logic family.

The selected resistor values produce a nominal \( V_{\text{OH}} \) of 3.21 V at the nominal 12-V output voltage.
6 Enhancing Shutdown Performance

6.1 OUT Pin “Isolation”

The TPS2490 gate drive circuitry includes an active clamp at the output (GATE pin). Functionally, this clamp can be represented as a 14-V Zener connected from GATE (cathode) to OUT. (See Figure 3.) This clamp serves the purpose of protecting the external pass FET’s against damage from excessive gate voltage. However, in a load shutdown event, regardless of trigger, this “diode” becomes forward biased, now clamping the GATE pin, and hence, the FET gate(s), one diode drop below the output potential. In a traditional TPS2490 application, where the input supply is most often a nominal 48 volts, this also serves a purpose, protecting the FET gates from excessive negative VGS excursions. However, for low voltage applications, the turn-off performance can be improved with a simple trick.

![Figure 3. Gate Drive with Output Clamp](image)

Figure 4 and Figure 5 shows a comparison of the shut-down response of the circuit of Figure 1, for two different configurations. In both events, 12,000 µF of bulk capacitance is connected to the output (P12V), and a 20-A constant-current load is applied. Figure 4 shows the resultant GATE and output waveforms when the OUT sense pin is connected directly to the output node (i.e., if R20 were 0 Ω). Note that the total decay time of the output from 12 V to 0 V was about 6.9 ms; this corresponds quite well to the calculated period of 7.2 ms, indicating that the discharge profile is dictated by the load current. But because of the now forward-biased clamp, the FET gates follow this linear decay all the way down, offset by one diode drop. So in effect, the load bulk capacitance “holds up” the FET gates.
While in the event of Figure 4 the pass FETs are technically off, there is a drawback to this characteristic, particularly when operating close to the TPS2490 input UVLO threshold, as in this application. In the relatively benign lab environment, where perhaps only one input is exercised in any test, the turn-off action (GATE pin pull-down) is smooth and consistent. However, in a much noisier actual system, or under heavier load where the input supply may make a step recovery when the current is interrupted, the event may not be as clean. More specifically, if the input potential drops below VCC UVLO, the GATE pull-down may not be as consistent. Considering the gate potential is not much below the FETs’ VGS(TH) voltage, of a typical power MOSFET, it doesn’t take much for the decaying output voltage to pull the common FET sources below the ON threshold. The worst-case is if the input supply begins to oscillate about the UVLO window. In order to better protect the FET’s from indefinite operation in linear mode, it’s highly preferable to get the FET gates pulled low as quickly as possible.

Therefore, it is recommended to insert FET Q6 between the TPS2490 OUT pin and the actual output node (R20 is not installed). Driven by the same output as the pass FET’s, Q6 acts as a switch to perform an output disconnect function, or “isolate” the pin from the bulk cap during shut-down. During a turn-on event and subsequent card operation, Q6 is on, and connects OUT to P12V for powergood sensing. However, in a shutdown event, when Q6 turns off, the OUT pin is disconnected from the load. The GATE pin is no longer pinned to the output potential and inherent hold-up action of the potentially large bulk capacitance.

Figure 5 is an example of the same type of shutdown event when Q6 is installed. Note that while the output decay time (6.8 ms) is still dictated by the load on the circuit, the gates are pulled rapidly to ground. Consequently, the shutdown response is much more definitive than in Figure 4.
As a figure of merit for comparing different OUT pin “isolation” tricks, the residual gate discharge time, that is, the time to bring the gates from a condition of “FET’s off” to a gate voltage of 1 V, was examined. Figure 6 is a scope capture of a similar shutdown event, under the same conditions as in Figure 4 and Figure 5, on an expanded time base. Taking the FET’s off condition to be the point at which the GATE trace passes through the output potential (i.e., $V_{GS} = 0$ V), the discharge time to $V_{GATE} = 1$ V was measured to be 890 µs. This results in a significant safety margin for the hot swap circuit. Note that the residual gate discharge time is very consistent at 850 – 900 µs under the full range of load currents.
6.2 **Fast Gate Pull-down Circuit**

An additional though unintended benefit of using multiple, large pass FET’s as done here is the inherent large amount of gate capacitance, which is conducive to the dV/dt ramp control. However, that extra capacitance is detrimental to turning the FET’s off quickly. While the TPS2490 GATE pin sink capability can discharge the FET gates, turn-off under severe fault conditions may not be fast enough. A simple, three component circuit should be added to the gate drive circuit to easily address this.

The circuit of D2, R23 and Q7 comprises a fast gate pull-down mechanism to quickly turn off the pass FET’s. D2 simply performs a blocking function. When the TPS2490 GATE pin pulls low (in response to any condition), rather than discharging the FETs’ input capacitance directly, the GATE pin now pulls base current from transistor Q7, which in turn applies a much stronger discharge current to the gates.

The fast pull-down is beneficial in a couple of circumstances, with one of these situations being the more critical. For example, during shutdown from EN pin command as discussed in Section 6.1, the fast pull-down greatly reduces the time to turn the FET’s off. Referring to Figure 4, Figure 5 and Figure 6, this is the interval from EN deassertion until the gate is pulled below the FET ON threshold; at the time base of these figures, essentially the point at which the gate trace passes through output node potential. The typical turn-off time of 450 to 600 µs without the external circuit is reduced to only about 2.5 µs when the pull-down circuit is added.

More importantly though is the corresponding improvement in response to a severe overload, or output short-circuit condition. Figure 7 and Figure 8 are waveform captures of various nodes and the load current during short-circuit events. In both tests, the output is ramped up, then an initial operating load of 40 A is applied via electronic load. The short-circuit condition is then generated by depressing the load SHORT button.

In both instances, the fault current profile is essentially as expected. The sudden excursion over the fault threshold causes a hard gate pull-down to clip the current as quickly as possible. Once the current is brought back below threshold, the TPS2490 turns the FET’s back on slowly, in linear mode to “test” the persistence of the fault. This is when the fault timer is started. If the fault condition endures beyond the period of the timer, as below, the FET’s are turned off.

![Figure 7. Short-Circuit Event, With 40-A Pre-Fault Steady-State Load (without gate pull-down circuit)](image1)

![Figure 8. Short-Circuit Event, With 40-A Pre-Fault Steady-State Load (external gate pull-down installed)](image2)

(Channel 4 (load current) baseline is two-tenths of a division from the bottom of the screen.)
However, there are differences in the severity of the event between the two cases. In Figure 7, without the external pull-down circuit, the initial peak current spike reached about 230 A. Also, during the linear mode portion of the event, when the GATE tries to follow the decaying output node to slew the load current, the sourced current remains high. In fact, by the end of the fault timer period, the “regulated” load current is still 170 – 180 A. Compare this to the magnitudes captured in Figure 8, where the fast pull-down was used. Using scope cursors (not shown), the initial spike peak amplitude was measured to be 194 A, a significant reduction over the Figure 7 spike. Also, the TPS2490 is able to fold back the current to 112 A during the ensuing linear mode operation. Ultimately, the total interval elapsed above the programmed 100-A trip point, including the initial spike, is only 127 µs.

Figure 9 shows another short-circuit event. In this instance, the initial steady-state (pre-fault) load was 80 A. Again, using scope cursors (not shown) to obtain numeric results, the peak current was found to be only 181 A, with a final regulation point of 106 A.

Figure 9. Short-circuit event with 80-A initial load, and fast gate pull-down installed.

(Channel 4 (load current) baseline is two-tenths of a division from the bottom of the screen.)
Power Dissipation Data

The circuit of Figure 1 was laid out on a PCB and assembled for testing, primarily to validate the concept of passing up to 80 A through the hot swap circuit without the use of heat sinks. Recall that the feasibility of the design is predicated to some degree on the ability to achieve the FET manufacturer’s stated $R_{DUA}$, or better, even with five co-located drain tabs discharging heat into the PCB copper pours. Eight layers of PCB thermal plane were used, with 2 oz. copper. Thermal planes were split essentially equally (4 each) between the supply high-side current path and the return (GND) node. The overall dimensions of the planes were approximately 5.5” x 3.5”, but also encompassed patterns and keep-outs for the following large-size components:

- Six (2 supply, 4 load) 0.800” x 0.600” patterns for #2 solderless connector lugs
- Eight patterns for 12.5-mm dia. aluminum electrolytic radial-lead capacitors (test load)

Table 3 shows the dissipation associated with the various voltage drops across the high-current path of the PCB, both high-side components and plane areas, and the return plane. Dissipation was determined by measuring the voltage drops across each element in the current path, and calculating the power loss as the VxI product. Note that at these load currents, the voltage drops across not only components such as sense resistors and FET’s but also copper pours themselves are significant, and contribute to the heat which must be dissipated by the PCB. Table 4 lists the definitions of the various dissipation nodes (Table 3 column headings) recorded. The circuit and layout were found to have a minimum efficiency (at 80 A) of 98.6%.

### Table 3. Dissipation Losses Across PCB High-current Path

<table>
<thead>
<tr>
<th>$I_{LOAD}$ (A)</th>
<th>$P_{INP}$ (mW)</th>
<th>$P_{RSNS (each)}$ (mW)</th>
<th>$P_{THP}$ (mW)</th>
<th>$P_{SW (each)}$ (mW)</th>
<th>$P_{OUTP}$ (mW)</th>
<th>$P_{RTN}$ (mW)</th>
<th>$P_{D_TOT}$ (mW)</th>
<th>EFFICIENCY (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>3.3</td>
<td>18.7</td>
<td>2.6</td>
<td>11.1</td>
<td>14.0</td>
<td>41.4</td>
<td>192</td>
<td>99.8</td>
</tr>
<tr>
<td>20</td>
<td>14.2</td>
<td>75.2</td>
<td>10.6</td>
<td>44.9</td>
<td>55.9</td>
<td>167.0</td>
<td>773</td>
<td>99.7</td>
</tr>
<tr>
<td>30</td>
<td>30.6</td>
<td>168.9</td>
<td>24.3</td>
<td>102.3</td>
<td>127.8</td>
<td>379.5</td>
<td>1749</td>
<td>99.5</td>
</tr>
<tr>
<td>40</td>
<td>56.0</td>
<td>300.2</td>
<td>44.0</td>
<td>185.3</td>
<td>228.2</td>
<td>684.8</td>
<td>3140</td>
<td>99.4</td>
</tr>
<tr>
<td>50</td>
<td>79.5</td>
<td>469.4</td>
<td>71.0</td>
<td>297.0</td>
<td>357.0</td>
<td>1092.0</td>
<td>4962</td>
<td>99.2</td>
</tr>
<tr>
<td>60</td>
<td>116.4</td>
<td>675.6</td>
<td>105.0</td>
<td>438.5</td>
<td>527.7</td>
<td>1605.0</td>
<td>7249</td>
<td>99.0</td>
</tr>
<tr>
<td>70</td>
<td>161.0</td>
<td>918.6</td>
<td>145.6</td>
<td>619.8</td>
<td>728.7</td>
<td>2246.3</td>
<td>10055</td>
<td>98.8</td>
</tr>
<tr>
<td>80</td>
<td>218.4</td>
<td>1200.6</td>
<td>198.4</td>
<td>843.8</td>
<td>964.0</td>
<td>3019.2</td>
<td>13422</td>
<td>98.6</td>
</tr>
</tbody>
</table>

(1) Tests conducted with PCB resting on a lab bench at room ambient temperature (~25 °C), natural convection only.

(2) At each test current, input supply margined to maintain 12.00 ± 0.02 VDC at PCB input terminal lugs.

### Table 4. Power Dissipation Element Definitions

<table>
<thead>
<tr>
<th>NAME</th>
<th>ASSOCIATED POWER DISSIPATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{INP}$</td>
<td>Input copper plane, from P12VIN connector pattern sensed at lug, to thermal via centrally located within sense resistor patterns.</td>
</tr>
<tr>
<td>$P_{RSNS}$</td>
<td>Sense resistors (each), measured across Kelvin-connected TP3 to TP4.</td>
</tr>
<tr>
<td>$P_{THP}$</td>
<td>Component thermal plane, from thermal via centrally located within sense resistor patterns, to Q3 (center FET) drain tab.</td>
</tr>
<tr>
<td>$P_{SW}$</td>
<td>FET switches (each), measured across Q1 (largest drop of the 5 FET’s)</td>
</tr>
<tr>
<td>$P_{OUTP}$</td>
<td>Output copper plane, average from FET sources to J3/J4 patterns sensed at lugs.</td>
</tr>
<tr>
<td>$P_{RTN}$</td>
<td>Current return plane, from a Kelvin “average” sense of J5/J6, to 12V_RTN sensed at input connector lug.</td>
</tr>
<tr>
<td>$P_{D_TOT}$</td>
<td>Total, sum of the losses across the board.</td>
</tr>
</tbody>
</table>
Infrared camera measurements taken at 80-A load indicated that the hottest components were actually the sense resistors. The temperature of the FET cases and immediately surrounding PCB areas was about 70°C, suggesting junction temperatures not much higher than that. Given the maximum operating junction temperature of the IRL7843 of 150°C, these results suggest sufficient margin to operate the circuit at full load at the specified design target $T_A$ of 60°C. The forced air convection typical of the target rack and chassis environments would of course enhance thermal performance, further protecting the hot swap FET’s.

For comparison with competing hot swap controllers and solutions, Table 5 summarizes the test results for the same circuit and PCB layout, but with only a 5-V gate drive. To conduct the test, a 5.1-V Zener diode was connected from FET gate to source nodes, to clamp the GATE output voltage of the TPS2490. Test results demonstrated that FET dissipation was 21 to ~25% higher than with the full gate drive, exacerbating heating of the FET junctions. The relative increases for given load currents are shown in the table, along with the net change in total dissipation of the board ($P_{D-TOT}$). The dissipation of the other resistive drops was essentially unchanged, so those values are not shown in the table.

### Table 5. Comparative Dissipation with 5-V Gate Drive

<table>
<thead>
<tr>
<th>$I_{LOAD}$ (A)</th>
<th>DISSIPATION, $V_{GS} = 5$ V</th>
<th>% DELTAS vs. TPS2490 GATE DRIVE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_{SW}$ (each) (mW)</td>
<td>$P_{D-TOT}$ (mW)</td>
</tr>
<tr>
<td>10</td>
<td>13.5</td>
<td>21.0</td>
</tr>
<tr>
<td>20</td>
<td>54.6</td>
<td>822</td>
</tr>
<tr>
<td>30</td>
<td>124.1</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>226.1</td>
<td>3337</td>
</tr>
<tr>
<td>50</td>
<td>364</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>540.1</td>
<td>7761</td>
</tr>
<tr>
<td>70</td>
<td>766.4</td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>1051.4</td>
<td>14484</td>
</tr>
</tbody>
</table>

Table 6 lists the dissipation values with only 4 parallel FET’s installed on the board, to examine the feasibility of reducing the number of FET’s. To maintain the layout symmetry, the middle FET of the original 5-FET pattern was removed from the board to conduct this test. As shown in Table 6, the power loss in the FET’s rose sharply, 59% higher than in the 5-FET configuration at the 70 and 80 A points. Also, unlike the results with the reduced gate drive, this experiment resulted in increases in the two adjacent plane areas. While any of the absolute data values are specific to the layout of the test board, the percent changes provide designers with a relative comparison for determining how many FET’s to use in their application. A smaller number of FET’s may be appropriate where a given cooling airflow rate or different FET package will produce a better effective thermal impedance. Also, the table below may serve as a reference for determining number of FET’s when the target load is something less than 80 A.

### Table 6. Circuit Dissipation Results Using Four Parallel FET’s

<table>
<thead>
<tr>
<th>$I_{LOAD}$ (A)</th>
<th>DISSIPATION, 4-FET CONFIGURATION</th>
<th>PERCENT DELTAS VS. 5-FET RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_{THP}$ (mW)</td>
<td>$P_{SW}$ (each) (mW)</td>
</tr>
<tr>
<td>10</td>
<td>2.8</td>
<td>17.2</td>
</tr>
<tr>
<td>20</td>
<td>11.4</td>
<td>69.4</td>
</tr>
<tr>
<td>30</td>
<td>25.5</td>
<td>158.7</td>
</tr>
<tr>
<td>40</td>
<td>47.2</td>
<td>290.2</td>
</tr>
<tr>
<td>50</td>
<td>75.5</td>
<td>463.4</td>
</tr>
<tr>
<td>60</td>
<td>111</td>
<td>687.2</td>
</tr>
<tr>
<td>70</td>
<td>158.9</td>
<td>985.3</td>
</tr>
<tr>
<td>80</td>
<td>215.2</td>
<td>1340.4</td>
</tr>
</tbody>
</table>
8  **Conclusion**

A solution schematic was presented for hot swap control of a 12-V rail with up to 80-A load, based on the TPS2490 Hot Swap Controller. A design process was outlined, with appropriate equations, for designers to tailor the solution to the requirements of their own systems. Some related topics, such as choice of inrush limiting scheme, circuit UVLO considerations, and improving the shutdown response were discussed, so that the reader can understand how to configure the TPS2490 for this type of application. A few scope captures of operational events were presented to demonstrate circuit performance. Finally, some power loss data from a representative layout was presented, for comparison against alternate solutions, and to help the reader tailor the number of FET’s for the load level, cooling provisions, and MOSFET thermal characteristics specific to his or her design.

In summary, the scope plots and data presented here demonstrate that the TPS2490 device can be configured as the foundation for a very robust hot swap circuit for 12-V rails at very high currents.

9  **Footnotes**

1. The TPS2490 device data sheet is available from the Texas Instruments web site. A download link can be found on the product page at [http://focus.ti.com/docs/prod/folders/print/tps2490.html](http://focus.ti.com/docs/prod/folders/print/tps2490.html).

2. A download .zip file with the TPS2490 Calculator Tool Excel spreadsheet is available from the Texas Instruments web site at [http://focus.ti.com/docs/toolsw/folders/print/tps2490or91calc.html](http://focus.ti.com/docs/toolsw/folders/print/tps2490or91calc.html).

3. The transient dissipation limit of 48 W arrived at through calculations is based on the assumption that this effective thermal impedance (40°C/W) can be achieved with the D-PAK package, through a combination of dissipative layout techniques and airflow in the target system.

10  **References**


Appendix A Parallel FET's in Current-Limiting Hot Swap

This appendix contains an important note regarding the use of multiple, parallel FET's as the limiting "switch" in hot swap applications, such as the one presented in this application note. When evaluating potential devices to be used for this purpose, two different operating scenarios must be considered: limiting mode as during inrush control, and load steady-state.

Once the input bulk capacitance of the load has been charged up, the hot swap circuit output is essentially at the input supply potential, and the load is operating in steady-state, the parallel FET's are an effective means of reducing the IR drop of the hot swap switch. The effective resistance of the switch is the equivalent resistance of N resistors of R_{DS(on)} value in parallel, where N is the number of FET's used. As long as good, symmetrical layout practice is used, the FET's will share current approximately equally, and the power loss can be calculated as the sum of the resistive losses of I_{LOAD}/N through the R_{DS(on)} of each FET. Consider the situation in which the card or module has been operating indefinitely at maximum power, and at the maximum allowed ambient temperature. This dissipation can be used to estimate a worst-case starting junction temperature at which the FET's may be subjected to the stresses of a turn-on event.

A load turn-on or output ramping event, however, presents a different situation. During a turn-on event, the FET's will be operated in the linear region for some period. While in linear mode, there's no guarantee the FET's will share current equally, ON-thresholds and transfer characteristics will vary slightly from device to device. Also, once any one device starts conducting, the typically negative temperature coefficient of the V_{GS(TH)} parameter will decrease the threshold as the device heats up. Therefore, for a robust design, the assumption must be that one FET will turn on first, and conduct all the load current during ramp up.

This characteristic of the parallel FET configuration, along with the worst-case, steady-state junction temperature determined per the above, must be used to establish the transient FET power limit during start-up events, and in evaluation of SOA ratings of the selected device.
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