

# How to Review a Multicell Switching Charger Schematic

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## ABSTRACT

This application report provides a checklist for reviewing a switching charger schematic and explains each item in the list.

Before beginning the checklist, it is prudent to obtain the following charger information:

1. Battery chemistry information
2. How many cell in parallel or series?
3. Charge current rate, voltage rate
4. Does the charger have system load? Does the charger system need power path management? Does the charger need a dynamic power management?
5. Input voltage range and transience
6. Output voltage range and transience
7. What is the final product using the charger? Does it have any special requirement?
8. Host control or stand-alone charger
9. Smart charger or non-SMBus charger

After a multicell switching charger solution is selected, several general common design guide lines are applicable. The following paragraphs pertain to the checklist for schematic review. If anything violates the rule or is unclear, contact TI technical support.

## 1 PGND and AGND

PGND means power ground; it serves as a ground connection for a high-current power converter node. On a printed-circuit board (PCB) layout, it must be connected directly to the source of low-side power MOSFET.

AGND means analog ground; it serves as ground connection for low-current sensitive analog and digital signals. On a PCB layout, it must be connected to the analog ground plane, and only connect to PGND through the Power Pad underneath the integrated circuit (IC).

To make PCB ground layout clear, the PGND and AGND are separated and are connected with a short jumper wire on the schematic.

## 2 Common and Differentiate Mode Capacitor Around Current Sense

Place a 0.1- $\mu$ F ceramic capacitor from ACN/CSSN/SRN/CSON to ACP/CSSP/SRP/CSOP to provide differential mode filtering. Place an optional 0.1- $\mu$ F capacitor from ACP/CSSP/SRP/CSOP or ACN/CSSN/SRN/CSON to GND for common-mode filtering.

## 3 Vcc Filter; Resistor Package

Place a 1- $\mu$ F ceramic capacitor from PVCC to PGND pin close to the IC. To reduce the overvoltage spike or high dv/dt on the Vcc pin, add a 10- $\Omega$  1206 package resistor in front of the Vcc capacitor to give a 10- $\mu$ s RC time constant. Another pair of RC value can also be used on this filter, 0.47- $\mu$ F capacitor and 20- $\Omega$  0805 package resistor.

#### 4 Input Snubber

During the adapter hot plug-in, the input FETs have not been enabled, the ac switch is off, and the simplified equivalent circuit of the input is shown in Figure 1.

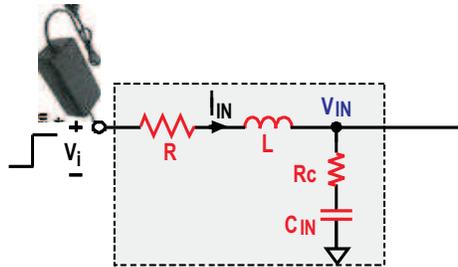


Figure 1. Simplified Equivalent Circuit During Adapter Insertion

Figure 2 depicts the recommended input filter design for a typical wall notebook adaptor input source. The measured input voltage and current waveforms are shown in Figure 3. The input voltage spike has been well damped by adding a 2-Ω resistor, while keeping the capacitance low.

If the input is not a typical notebook adaptor, the resistor and capacitor value may be changed according to the test result.

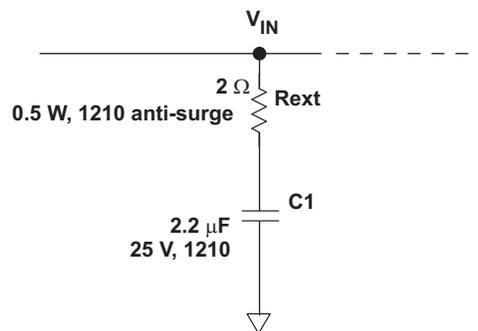


Figure 2. Recommended Input Filter Design

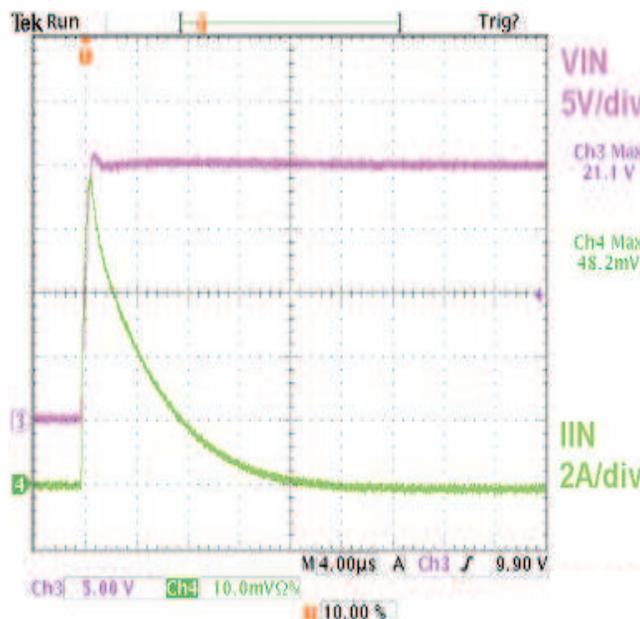


Figure 3. Adapter dc Side Hot Plug-in Test Waveforms

## 5 Charge Pump Circuit

If the switching charger has a charge pump circuit for driving the high-side FET, place a bootstrap capacitor close to the IC. Typically, a 0.047- $\mu\text{F}$  capacitor and a Schottky bootstrap diode are used in most application circuits (the  $C_g$  of high-side MOSFET is less than 4.7 nF).

## 6 Reverse Input Protection

If a reverse input source is plugged in, the charger should survive. Every IC pin must be protected for that condition. In Figure 4, the input has a pair of back-to-back P-channel MOSFETs, which is driven by ACDRV. It provides the reverse input protection. All IC pins are isolated by ACFET.

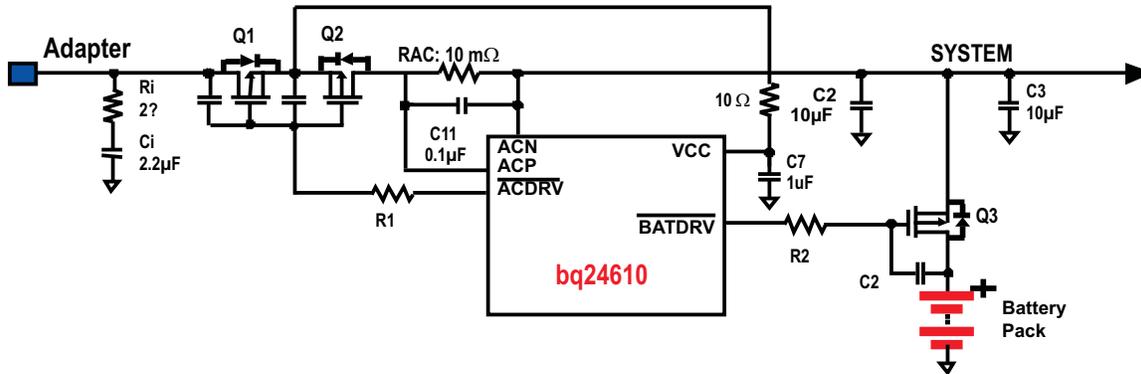


Figure 4. P-FETs Reverse Input Protection

In Figure 5, the new charger IC drives the N-Channel MOSFETs. The external reverse input protection circuit (Q6, R6 and R7) has to turn off the RBFET (Q2) and limit the current flowing out from CMSRC and ACDRV. In normal operation, Q6 is turned off by negative  $V_{gs}$ . When adapter voltage is reversed, Q6  $V_{gs}$  is positive. As a result, Q6 turns on to short gate and source of Q2 so that Q2 is off. Q2 body diode blocks negative voltage to system. However, the CMSRC and ACDRV pins need R3 and R4 to limit the current due to the ESD diode of these pins when turned on. Q6 must have low  $V_{gs}$  threshold voltage and low  $Q_{gs}$  gate charge so it turns on before Q2 turns on. R3 and R4 must have enough power rating due to power dissipation when the ESD diode is on. In Figure 6, the Schottky diode D3 gives the reverse adapter voltage protection, no extra small MOSFET or resistors are needed.

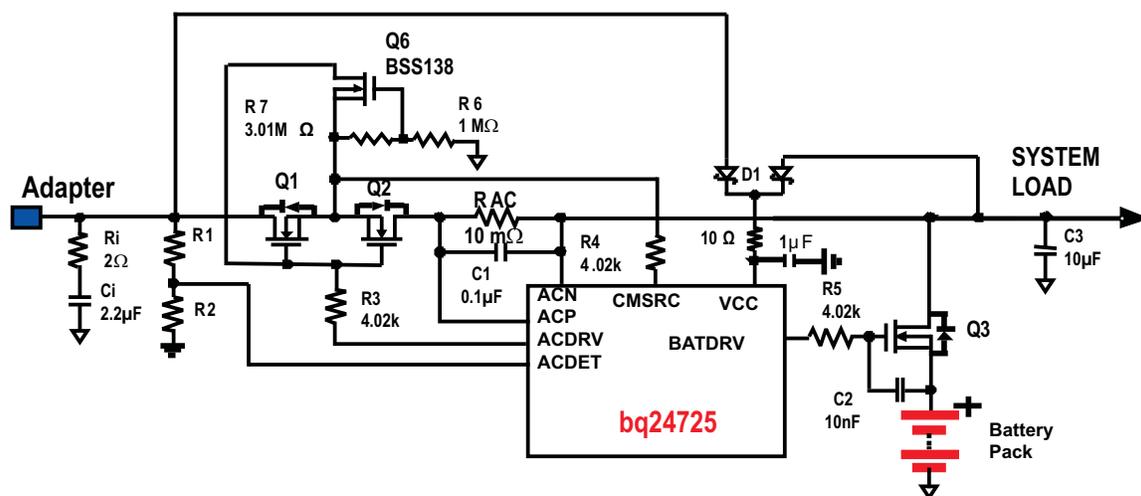
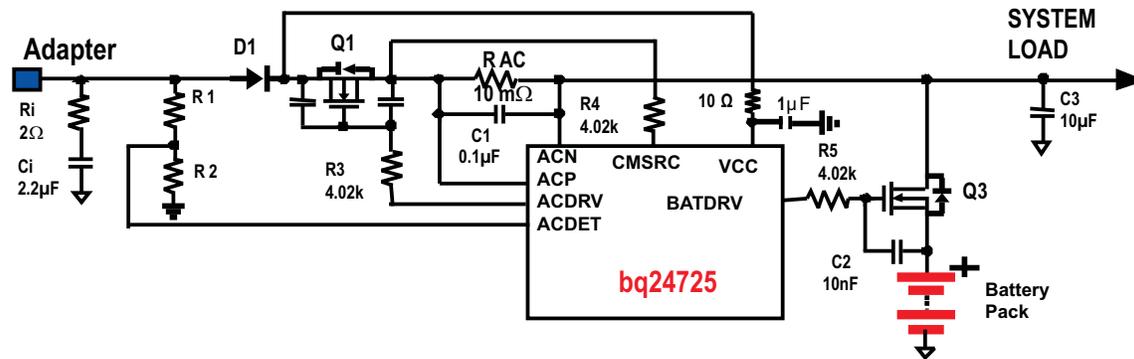


Figure 5. N-FETs Reverse Input Protection


**Figure 6. One Diode Reverse Protection**

## 7 Input FET and BATFET Gate Drive Capability

If there is an internal charger pump that drives the N-Channel input FET or BATFET, such as the bq24725 (see [Figure 5](#) and [Figure 6](#)), the minimum load resistance between BATDRV and SRN or minimum load resistance between ACDRV and CMSRC is 500kΩ because of the gate drive (charge pump circuit) capability.

## 8 Capacitor Voltage Rate and Material

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. This effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

Check the REGN or PVCC capacitor voltage rating.

## 9 Check Current Limit Type, Cycle-by-Cycle Current Limit or Average Current Limit

The bq24725/707/726, bq24745/747/765, bq246xx, and bq2417x/13x have cycle-by-cycle current limit. The output capacitance must be placed between the outside of current sense resistor and the battery package terminal. An optional 0.1-μF capacitor between SRP or CSOP and ground is for common mode filtering. Meanwhile, the capacitance on SRP must not be higher than 0.1 μF in order to properly sense the voltage across SRP and SRN for cycle-by-cycle under-current and over current detection.

The bq2410x/11x/12x, bq24702/703, bq24704/605, and bq2475x have average current limit. The charge-current sense resistor  $R_{SR}$  must be positioned with half or more of the total output capacitance placed before  $R_{SR}$ , contacting both  $R_{SR}$  and the output inductor; and the remaining capacitance placed after  $R_{SR}$ . The output capacitance must be divided and placed on either side of  $R_{SR}$ . A ratio of 50:50 gives the best performance, but the node in which the output inductor and  $R_{SR}$  connect must have a minimum of 50% of the total capacitance. This capacitance provides sufficient filtering to remove the switching noise and give better accuracy.

## 10 Add Series Resistor in Front of ACDRV and BATDRV

To limit the in-rush current on ACDRV pin, BATDRV pin, and CMSRC pin, a few kilo-ohm resistor is recommended on each of the three pins. Refer to [Figure 4](#), [Figure 5](#), and [Figure 6](#). Also, set the VCC or PVCC filter RC time constant much smaller than this ACDRV or BATDRV RC time constant.

## 11 HIDRV Turnon Speed to Reduce EMI

If the product has an EMI concern on switching charger circuit, reserve a resistor between the IC's high-side gate drive pin and MOSFET's gate. The resistor can slow down the high-side FET turnon speed and reduce the spike and ringing on switch node voltage waveform.

### 12 Check That Inductor Ripple Does Not Hit Current Limit

Calculate the maximum peak to peak inductor ripple current at worst condition.

$$I_{ripple\_p-p} = (V_{in\_max} - V_{out}) \times V_{out} / (V_{in\_max} \times L_{min} \times f_{s\_min})$$

$V_{in\_max}$ : maximum input voltage,

$f_{s\_min}$ : minimum switching frequency,

$L_{min}$ : minimum inductance

$V_{out}$ : pick the possible output voltage that close to half maximum input voltage

The IC has a charge over current limit threshold,  $V_{oc}$  that is 145% or 165% of  $R_{sns} \times I_{REG\_CHG}$ . Please make sure the  $I_{ripple\_p-p}$  is lower than  $2 \times (V_{oc} - R_{sns} \times I_{REG\_CHG})$ . So, the charge current can run at  $I_{REG\_CHG}$  without triggering over current protection first.

### 13 Input FET Power Rating and In-Rush Current Control

A large volume system capacitor or system load needs high-power rating input FET to handle the power dissipation during a soft start (inrush current control).

Figure 7 is soft start waveform on Figure 8 circuit. Use "transient thermal impedance" chart from data sheet to verify the junction temperature. If the junction temperature is lower than  $T_{j\_max}$ , the input FET is safe.

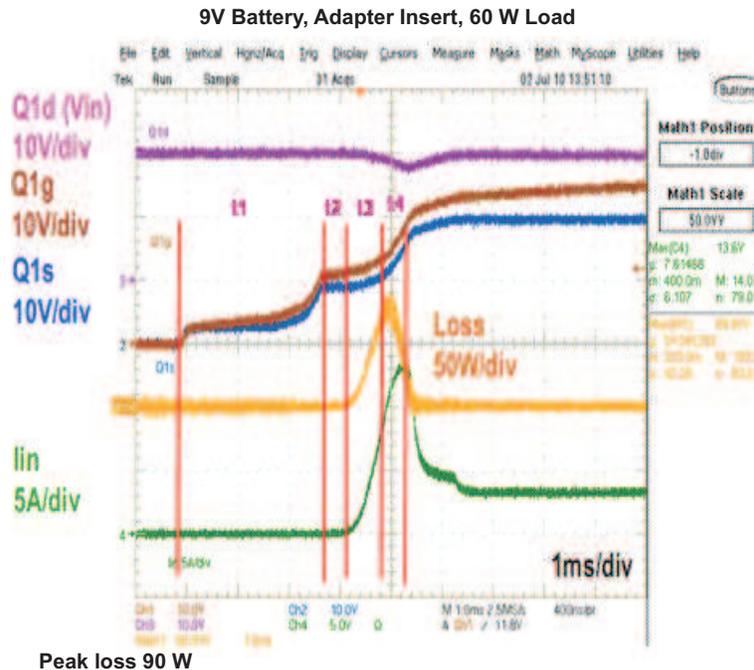


Figure 7. Input FET Power Loss During Soft Start

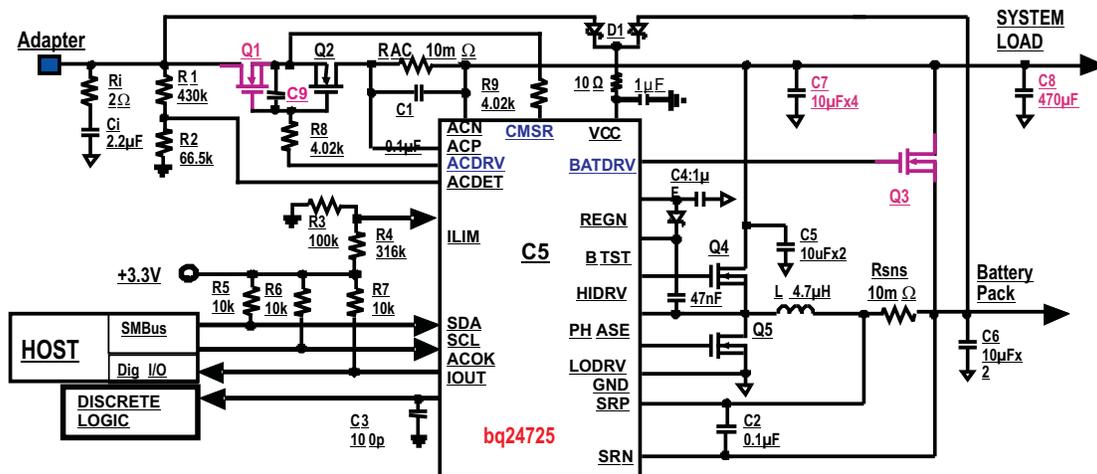


Figure 8. A Typical Charger Circuit With Power Path Management

#### 14 BAT Output Capacitor or Resistance is Out of Range

For host control charger, a data sheet will give a recommended inductor and capacitor value based on the LC resonant range.

For stand-alone charger, it not only has a LC resonant range, but also has  $C_{max\_wake}$  or  $C_{max\_dis}$  calculation which is derived from the battery detection parameter [see bq24610 data sheet ([SLUS892](#))]. If the output capacitor is over  $C_{max}$ , the status pin will flash even when battery is absent.

Also, if the resistance is too high between charger output and battery terminal, the charger will run in and out of charger termination.

$$R_{bat\_max} = V_{rch} / I_{term}$$

$V_{rch}$ : Recharge threshold voltage; mV/Cell  
 $I_{term}$ : Termination current.

#### 15 Iout Stability 100 pF

For bq24725/707/726, place a 100-pF or less ceramic decoupling capacitor from IOOUT pin to GND.

For bq2475x; bq24704/705 and bq740/741, place a 100-pF or less ceramic decoupling capacitor from IADAPT pin to GND.

For bq24745/747/765, place a 100-pF or less ceramic decoupling capacitor from VICM pin to GND.

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