Application Report
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Using a Single-Output Gate-Driver for High-Side or Low-Side Drive

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High Performance Isolated Power

ABSTRACT

In many isolated power-supply applications, power MOSFETs are often arranged in some form of bridge configuration for optimization of both the power switches as well as the power transformer. These bridge configurations create two classifications of switches: high-side (HS) and low-side (LS). Dedicated HS and LS gate-driver ICs, such as the UCC27210, offer an output for HS switches as well as an output for LS switches in a single IC.

Some applications see great benefit, however, from using single-output gate drivers such as the UCC27531 instead of combination HS and LS drivers. Single output drivers can be located closer to the power switches for more optimum switching performance. Their small size allows for more flexibility in layout and the ability to drive many different types of switches in the system allowing cost savings from high-volume orders.

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1 Introduction

HS switches refer to Q1 and Q2 in Figure 1. These switches have a source connection that is floating and the voltage on this reference changes during the switching cycle. Q3 and Q4 are considered LS switches as their source reference connection is tied to input ground and does not change voltage during the switching period. Power is delivered to Vout when Q1 and Q3 are on at once, or when Q2 and Q4 are on together. For our circuit examples in section 2, we will focus only on the bridge portion using Q1 and Q3.

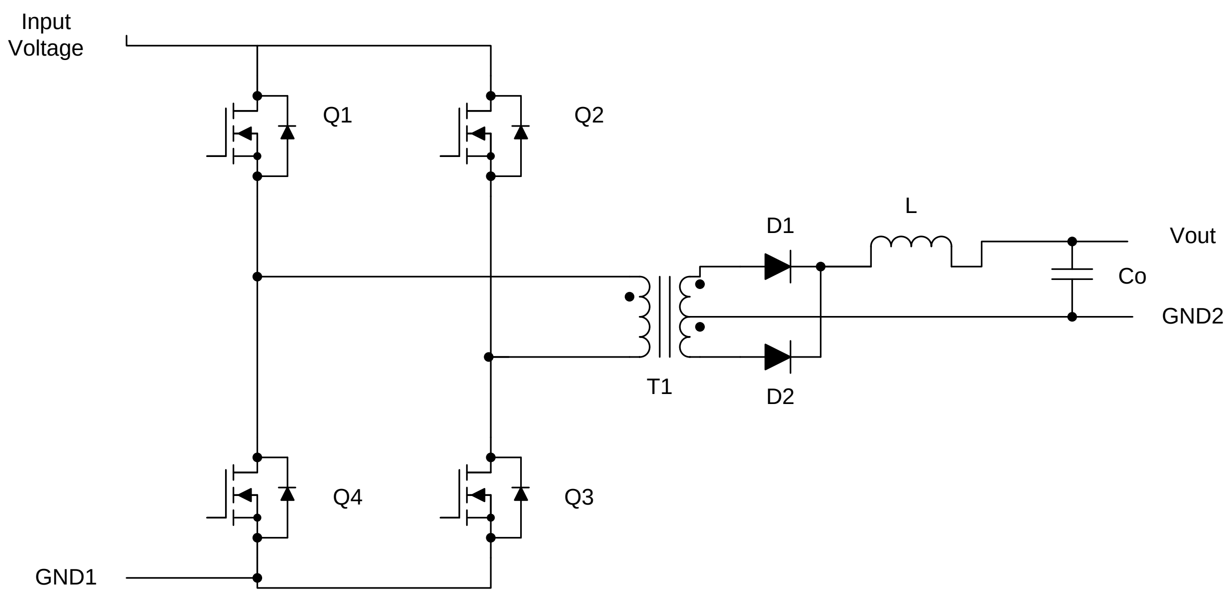

Figure 1. Full-Bridge Powerstage with both High-Side and Low-Side Primary MOSFETs

To properly turn-on these switches in high-power applications, gate-drive ICs are often required. To properly drive a LS power switch, it is usually simple enough in that the output of the gate driver can be tied directly to the gate of the switch with the GND of the Driver IC tied to the source of the switch. To drive a HS switch, however, a few more considerations must be made:

1. For the **gate driver output signal** itself, a level-shifter or isolated signal transceiver such as a digital isolator or opto-coupler is needed to ensure the gate maintains the proper voltage above the source to properly turn-on the HS switch. As the source of Q1 (GND of gate driver) rises during Q1 turn-on, the driver needs its reference voltage to follow the Q1 source closely and maintain the difference between the signal voltage and the reference. Further, the GND of this driver needs to be isolated from the controller ground because the Q1 source moves between 0 V and some higher voltage such as 400 V.

2. The HS gate driver also needs some sort of **bias supply** that can float and maintain the proper turn-on bias when the source rises to the input voltage. Otherwise, the gate driver would shutdown when the Q1 source voltage increases. This is usually accomplished by using a bootstrap circuit, an isolated bias supply, or using gate-drive transformers to isolate the gate driver from the switch-node reference.

2 Methods For High-Side Drive

2.1 Bootstrap Bias Supply with Optically-Isolated Signals

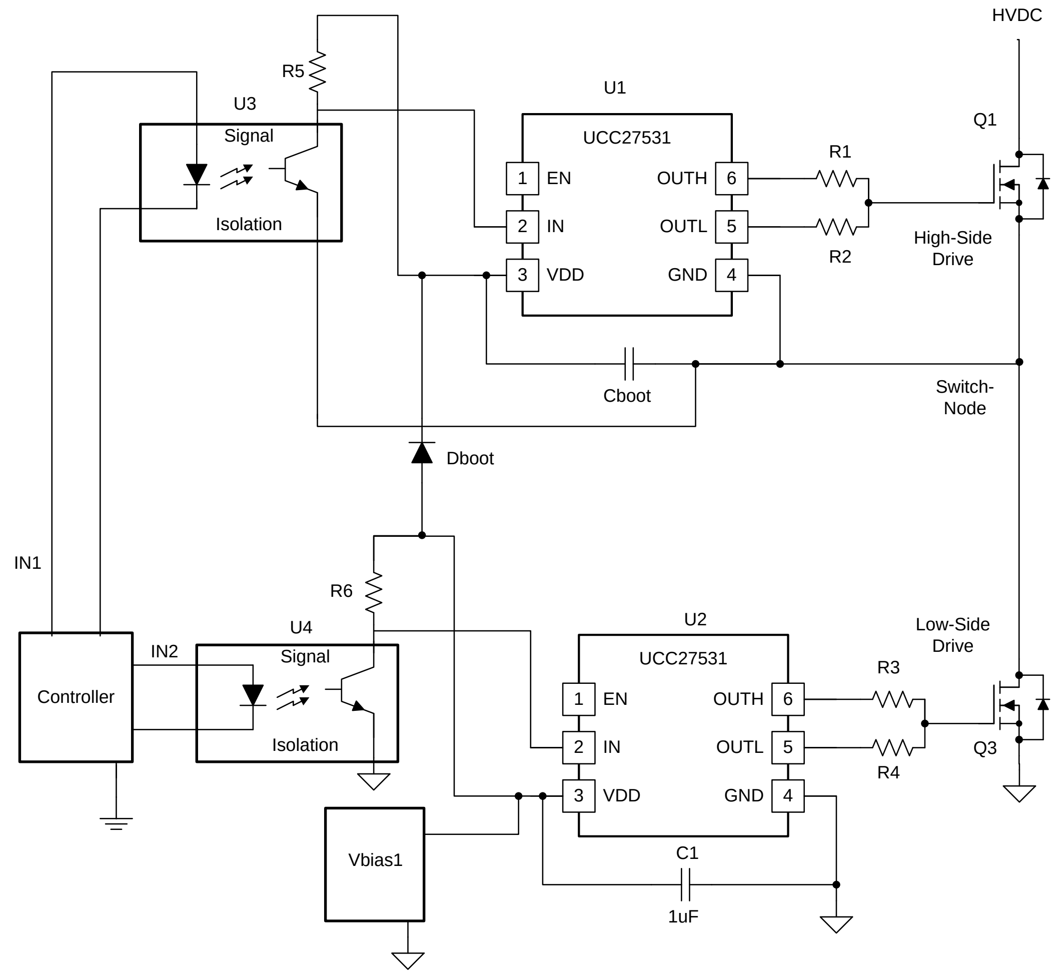

Figure 2. High-Side Bootstrap Circuit using Optical Signal Isolation

Signal Isolation

In Figure 2, the input to U1 is isolated using U3. This allows the signal to operate properly, even as the signal reference (switch-node) changes voltage throughout the switching period. It also isolates the controller ground from the switch-node.

Bias

In Figure 2, Dboot and Cboot are used as a bootstrap circuit to bias U1 properly when Q1 is turned on. When Q1 is off, Dboot is forward biased and U1 is supplied directly from Vbias1 while Cboot is charged. When Q1 turns on, the switch-node voltage increases to HVDC, Dboot is reverse-biased protecting Vbias1, and U1 is powered as Cboot empties its charge into the VDD pin of U1. This charge from Cboot must be adequate to keep U1 on throughout the entire time that Q1 is on. Sizing of Dboot and Cboot are beyond the scope of this article but there are numerous publications on how to select these components.

2.2 Bootstrap Bias Supply with Capacitive Signal Isolation

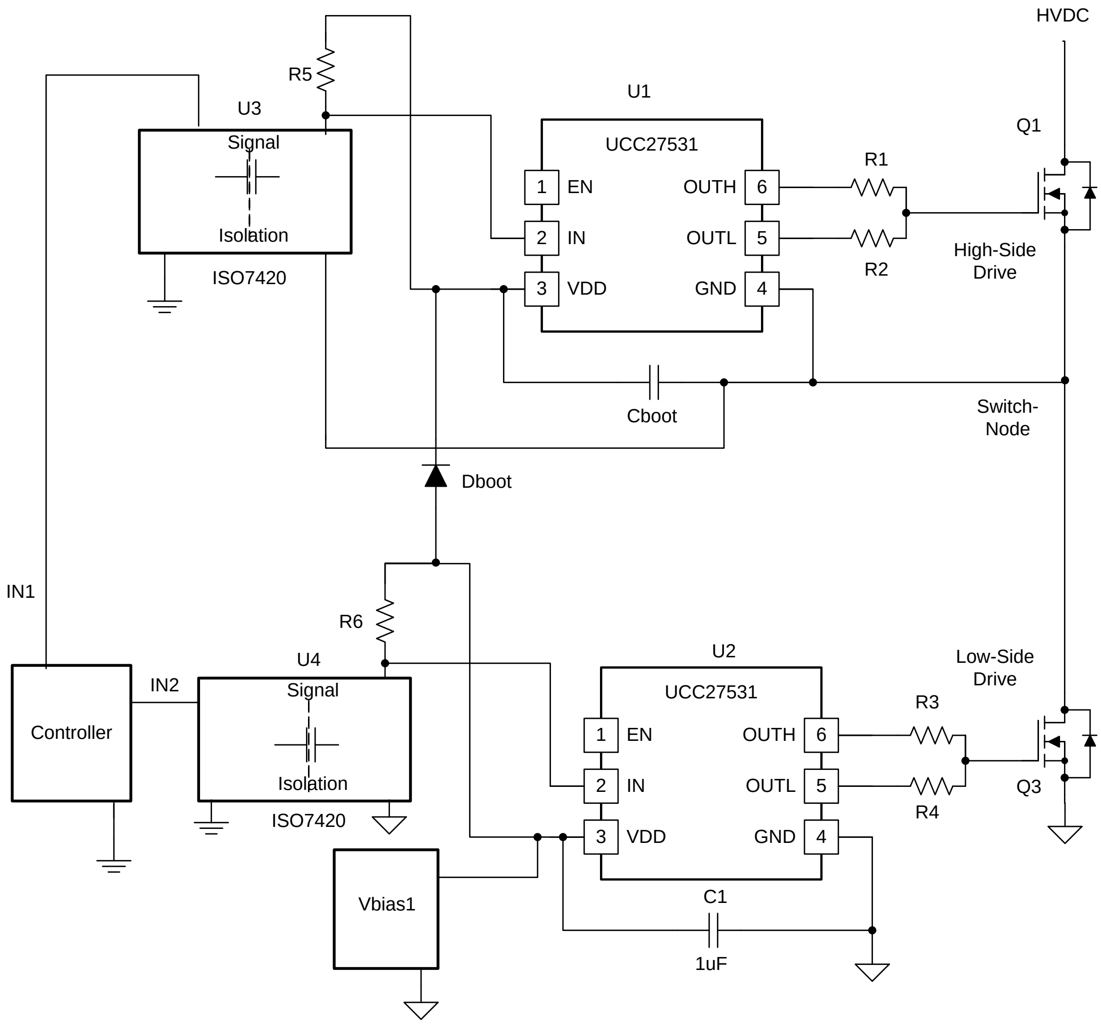

Figure 3. High-Side Bootstrap Circuit using Capacitor-Based Signal Isolation

Signal Isolation

In Figure 3, the input to U1 is isolated using U3. U3 is capacitive signal isolator ISO7420. Capacitive-based isolators can signal properly even with large common-mode ground slew-rates, they are more stable over life and temperature compared to optocouplers, and they do not have the duty cycle limitations of gate-drive transformers.

Bias

In Figure 3, Dboot and Cboot are still used as a bootstrap circuit to bias U1 properly the same as in Figure 2.

2.3 Bias Supply with Integrated Transformer and Optical Signal Isolation

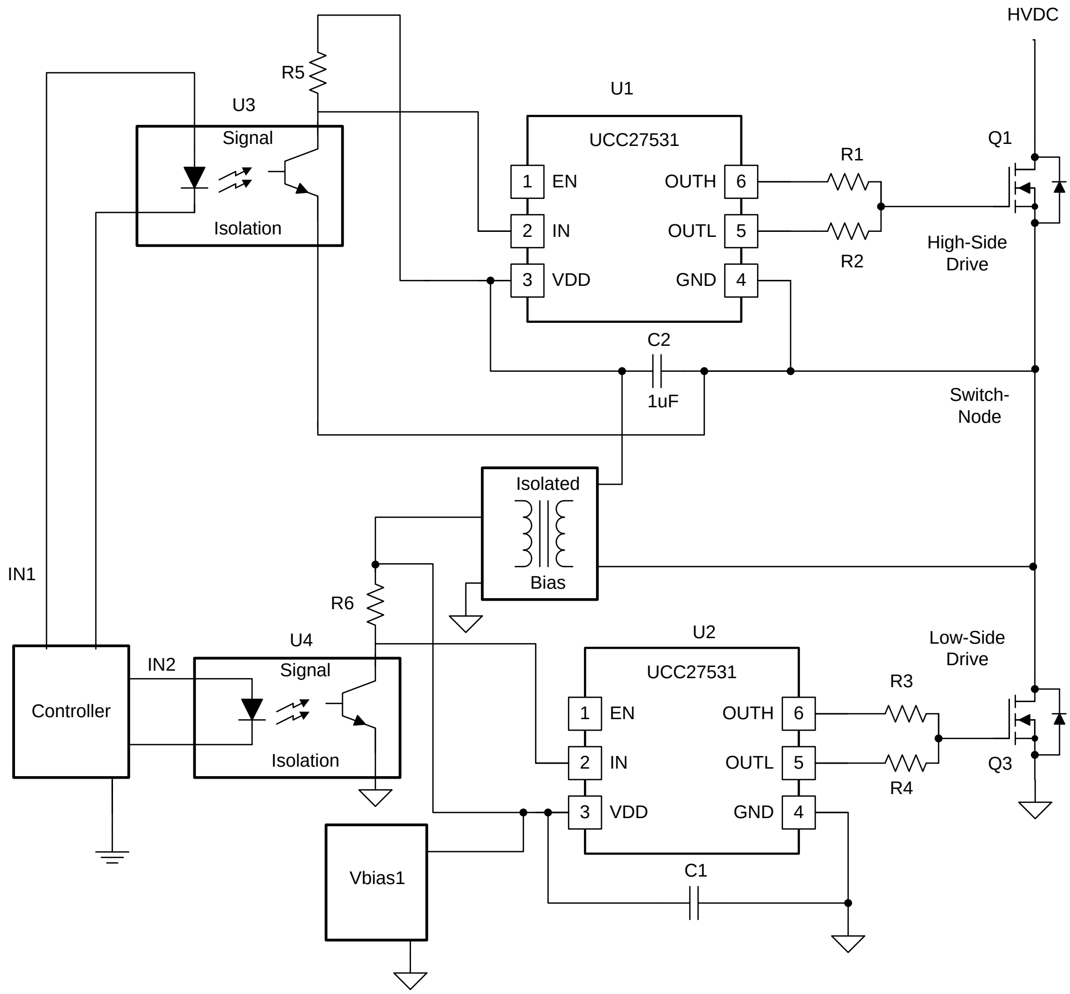

Figure 4. High-Side Isolated Supply

Signal Isolation

In Figure 4, the input to U1 is again isolated using U3.

Bias

In Figure 4, U1 is supplied using an isolated supply. This is similar to the configuration in the UCC27531EVM-184, where non-regulated, isolated supplies from Recom (RP-120X series) are used.

2.4 Gate-Drive Transformer Solution

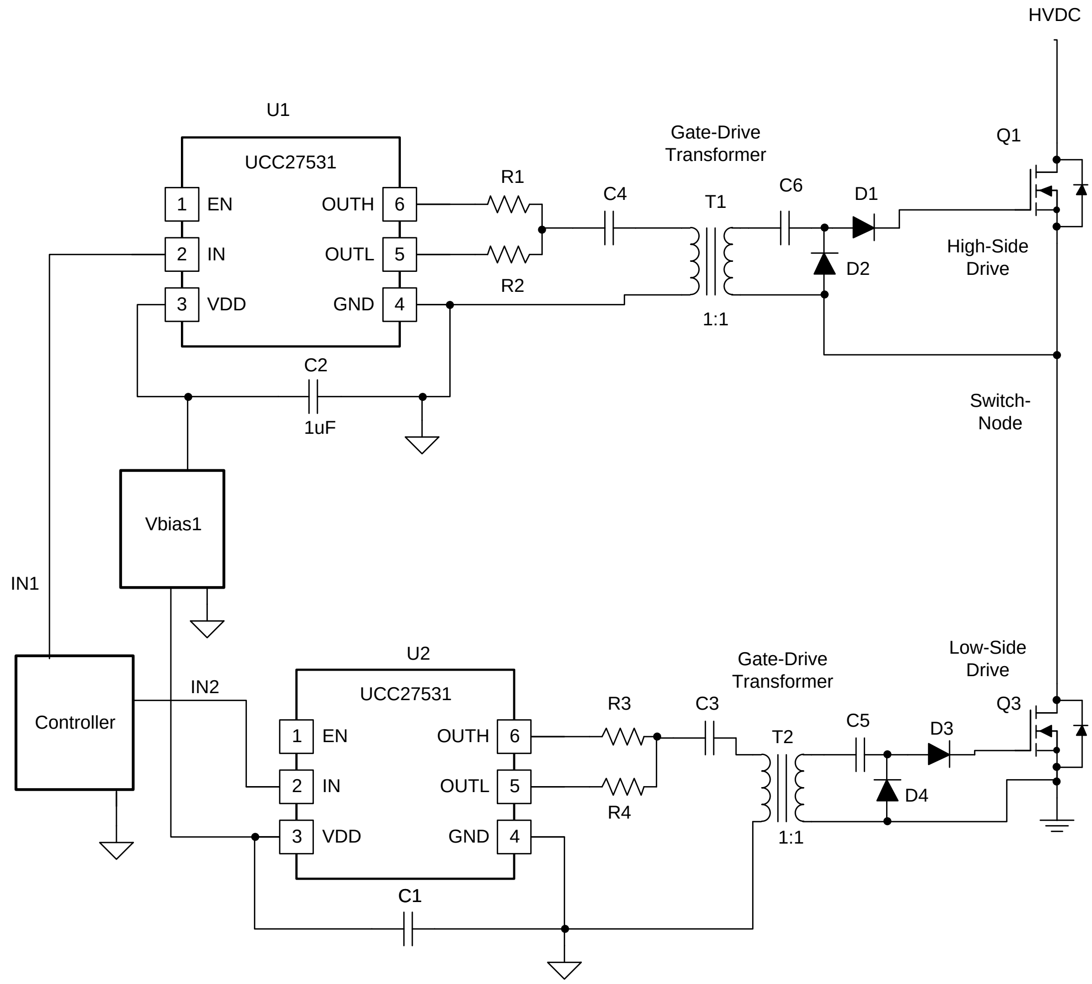

Figure 5. High-Side Gate-Drive Transformer

Signal Isolation

The output signals of U1 are isolated now in Figure 5, not the inputs as before, with the use of T1. The transformer allows the gate signal to Q1 to have a floating reference that can move as the switch-node moves in voltage. DC blocking capacitors like C4 and C6 are added, as well as rectifier D1, and D2 to add offset to C6, preventing imbalance.

Bias

In Figure 5, an isolated or bootstrap supply is not needed. In this configuration the gate drivers are referenced to the same ground as the controller and Vbias1. Therefore, bias voltage can be directly supplied by Vbias1.

Conclusions

Driving the gates of LS power switches is fairly simple in terms of signal path and proper biasing. Driving floating-source switches such as HS MOSFETs in bridge configurations, however, presents some challenges in terms of both signal path and bias for the HS gate driver. This paper has presented numerous circuit examples that have shown different methods of achieving HS gate driving using a single-output gate driver.

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