Enabling High-Current Hotswap Applications Using the TPS2393A

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ABSTRACT

The TPS2393A integrated circuit is a hotswap controller optimized for the application of ~48 V systems. The TPS2393A, which is widely used in numerous applications, introduces the following competitive features:

- Wide input supply range
- Programmable current limit
- UV/OV protection
- Insertion detection
- Power good indication
- Alert

The TPS2393A is designed to provide load current slew rate control to manage inrush into the load and also has peak magnitude current limiting. Normally, the actual nominal load current is always smaller than current limit threshold with a safe margin. However, in some situations, the application needs much higher nominal current into the load. This situation can create a lot of stress on the FET used to control inrush into the application (for example, in a system requiring ~48 V at a nominal 10 A). At initial turn-on, the $V_{DS}$ across the FET is 48 V if the current is limited to 10 A, which would be 480 W initially. Of course, as $V_{DS}$ decreases the power also decreases. This makes FET selection very problematic for the application.

This paper provides a simple and efficient method to solve this problem and an easy-to-use way to extend the application of the TPS2393A.
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Introduction

TPS2393A is a full-featured –48 V hotswap power management IC. As the most popular hotswap controller, TPS2393A uses an external N-channel power FET and a low-value current sensing resistor to control load power up, which operates as controlled-current. Figure 1 is a block diagram of the circuit. A reference voltage is applied to the noninverting input of the linear current amplifier (LCA). Load magnitude information is fed to the inverting input as the drop across sensing resistor $R_{SNS}$. The LCA slews the gate of the pass FET to limit the load current to reference value. The VREF reference is clamped at 40 mV, as shown in Figure 2. Therefore, current flowing in the load during turn-on is limited to the value given by $I_{MAX} \leq 40mV / R_{SNS}$.

(IMAX is the maximum load current.)

Figure 1. TPS2393 Current Control Loop
Figure 2. Ramp Generator Block

Figure 3 shows the typical hotswap schematic. Figure 4 is a waveform with current limit at 2 A.

Figure 3. Typical Hotswap Schematic
NOTE:

$V_{OUT}$ is actually $V_{DRAIN}$ of the FET. At $T = 0$ the VDS is approximately 48 V; as the FET turns on this approaches zero. The contact bouncing shows a hotswap or board insertion event. This is why to the left of the graph VDS is 0 (no power to board). Upon insertion, the voltage bounces and then rises to 48 V. The gate starts to slew and let current into the load, and during this time $V_{DS}$ decreases as $I_{DS}$ increases.

Achieve a High-Load Hotswap

To avoid violating the safety operation area (SOA) curve with much higher load current, the maximum current amplitude must be limited during inrush to a reasonable value.
For example, the typical charging current in bulk capacitor during turn-on is 2A (40mV/20mohm); therefore, the actual load current must be less than 2 A, as shown in upper diagram in Figure 4. But in some applications, the load current can be much higher, from 5 to 50 A of load current, as shown in lower diagram in Figure 4. Of course, this requires a very low value for sensor resistor $R_{\text{sns}}$ to set the maximum current limit into the load. However, at these higher currents, $I_{\text{MAX}}$ is also very high. It is difficult to select a proper current limit FET. For example, the normal load current is 10 A, and the value of $R_{\text{sns}}$ must be lower than 4mohm (40mV/10A). $I_{\text{MAX}}$ will exceed 10 A as well.

**Figure 5. Ideal Current Waveform in Different Requirement**

Assuming the normal load current is 10 A and considering the thermal rise of FET, we should choose a correct Rdson. For example, choose FDB047N10: $R_{\text{dson}} = 4.7\, m\Omega$;

$$R_{\text{egsa}} = 62.5 \, ^{\circ}\text{C/NW};$$

Assuming an ambient temperature of $T_A = 40 \, ^{\circ}\text{C}$, the junction temperature of FET can be calculated as follows:

$$T_{\text{mosfet}} = T_{\text{rise}} + T_A = (I_{\text{load}})^2 \times R_{\text{dson}} \times R_{\text{egsa}} + T_A = 69.4 \, ^{\circ}\text{C}$$

At steady state, the thermal rise is okay. Also, it is necessary to review the SOA graphs to determine if FET can handle the transient power dissipation at startup. Figure 5 show the typical maximum SOA of FDB047N10.
At 25°C case temperature and 48 V input condition, the running time should be less than 1 mS with 10 A constant current (see the red dashed line in Figure 5) but it can support approximately 10 mS running time with 2 A constant current (see the blue dashed line in Figure 5). In another way, small current will need more time to charger bulk capacitor to input voltage. So, we should balance the reliability and charger time to choose a suitable current level.

Also, remember that the SOA graph on the FET data sheet is based on 25°C ambient case temperature. In an actual power system, the ambient case temperature is higher than this, thus we must consider the temperature derating. Application note *Hotswap Design using TPS2490/91 and FET Transient Thermal Response* is a good reference.

![Figure 6. SOA Curve of FDB047N10](image)

A simple way to meet the requirement of a high-output current hotswap is to separate the LCA current limit threshold from over current (OC) limit threshold. Unfortunately, they are combined in TPS2393A.
When reading the data sheet carefully, we can find that the power good indication pin (/PG) is active-low when the following two conditions are met:

- The voltage at the DRAINSNS pin is below the power good threshold (1.35 V).
- The voltage at the IRAMP pin is above 5 V.

Therefore we can use the /PG signal to change the current level of pass FET at LCA current limit condition and the overcurrent condition. Figure 6 is the simple schematic.

![Figure 6. Simple Schematic](image)

**Figure 7. Adding Bias Current to Change the Actual Load**

Because we know that ISENS pin is the negative terminal of LCA, which is clamped to 40 mV, then we can get an equation:

\[
40mV = \frac{4V - 40mV}{R1 + R2} \times R3 = \left( \frac{4V - 40mV}{R1 + R2} + Io \right) \times R4
\]

Io can be simplified as:

\[
Io = \frac{40mV - \frac{4V}{R1 + R2} \times R3}{R4}
\]

In Figure 6, R1 = R2 = 470K, R3 = 680ohm, R4 = 4mohm. So, at startup, the actual load current \(Io \approx 1.3\ \text{A}\). From SOA curve in Figure 5 (see the yellow dashed line), the maximum SOA time with 1.3 A constant load current is close to 100 mS.

Suppose the total output capacitor CLoad = 100 µF, the minimum charger time is:

\[
T_{\text{charge}} = \frac{48V \times 100uF}{1.3A} = 3.7\text{mS}
\]
The TPS2393A also can program the Inrush Slew Rate by a capacitor on the IRAMP pin, thus the actual charge time will be higher than this. The time to charge the load capacitor is less than the maximum SOA time, so the FET is suitable for current design.

The TPS2393A also includes a programmable Fault Timer to protect FET. From the preceding analysis, the value of Fault Time can be set in the range of 3.7 to 100 mS. The timer capacitor can be calculated by the following equation:

\[ C_{FAULT} (\mu F) = 14.4 \times T_{FAULT} \text{ (in } \text{ Seconds}) \]

Figure 7 shows the startup waveform, which was tested on EVM board.

![Image of startup waveform](image)

CH1 = Vdrain; CH2 = 48V; CH3 = /PG;

**Figure 8. Startup With Bias Current**

When the start-up process completes, the /PG signal turns low. The bias current through R2 can be ignored. The maximum load can go up to \( \frac{40mV}{R4} \approx 10A \).

The bias current will change with the bus voltage because R1 is connected directly to bus voltage. If the voltage range on bus is wide, we can add external circuit to provide a fixed reference voltage to R1, and then the bias current will also be fixed.
Conclusion

Even though the TPS2393A has only one relatively low threshold of current limitation, it can be designed for more applications, where load current at steady state must be higher than the charging current during the startup ramping. This paper discusses a method to change to current limit at different operation stages, from rising to settle down.

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