

UCD3138 PFC Tuning

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High Performance Isolated

ABSTRACT

PFC current loop tuning is a time consuming and challenging task for the PFC design engineer. It requires the current waveform not only to be stable, but also to be smooth with very low total harmonic distortion (THD) and high power factor (PF). It gets more and more challenging with the ever increasing THD and PF requirements. Although digital controller provides more flexibility and better performance, loop tuning still requires significant effort, especially for the engineers new to PFC design, the word “digital” may also sounds scary for people switching from analog control to a digital solution. This application note provides a step by step guide of how to tune the current loop of a UCD3138 [1] controlled PFC, as well as some techniques to reduce THD and improve PF.

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1 PFC Current Loop Bode Plot

1.1 How to use network analyzer to measure bode plot

Current loop bode plot provides a straight forward guide of how good the loop performance is. Although the bode plot can be derived by mathematical modeling, the accuracy of power stage components parameters, along with the lack of knowledge of parasite capacitance/inductance of PCB will affect the accuracy of the model. Using network analyzer (such as Venable machine) is still a widely used method to get accurate bode plot. The following procedure shows how to use Venable to measure PFC current loop bode plot:

Step 1. Insert a 50Ω resistor in current feedback. It is important that this resistor be placed between a high impedance and low impedance node. If not the true loop gain will not be measured. Also be sure there is a local cap at the current sensing input pin of UCD3138. It will minimize unwanted noise injected by network analyzer connection.

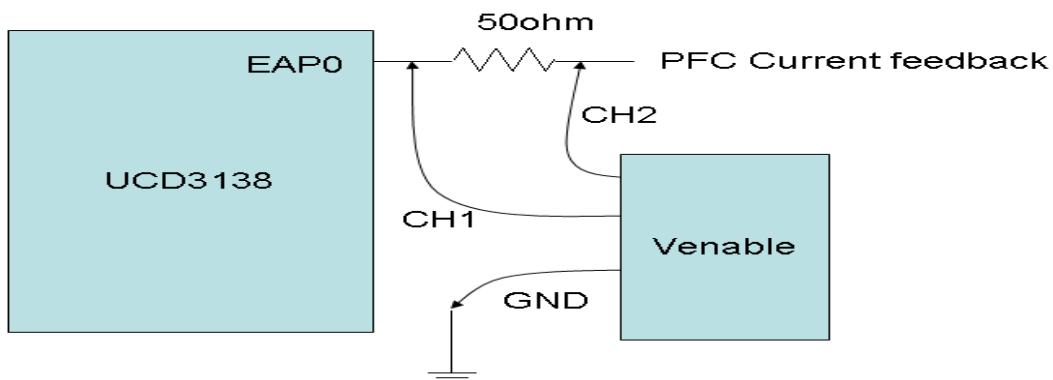


Fig. 1. Venable connection setup

Step 2. Open Venable control menu, configure the following settings:

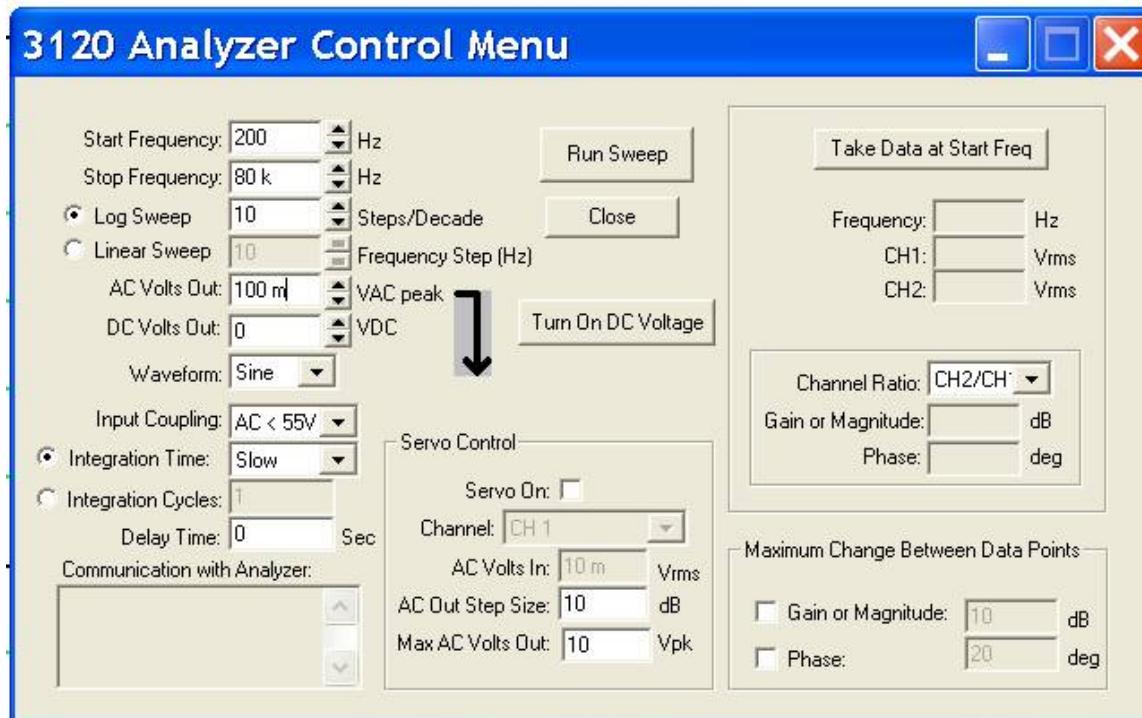


Fig. 2. Venable bode plot measurement setting

Step 3. Click “Take Data at Start Freq” first and wait for the measurements to settle, then click “Run Sweep”, it will measure the current loop bode plot.

1.2 Voltage loop effects on current loop bode plot

There are some concerns of how to accurately measure PFC current loop bode plot. The first concern is how the voltage loop will affect the current loop. PFC has two loops: a current loop which regulates the inductor current, and a voltage loop which regulates output voltage at a much lower (normally over 100 times) bandwidth than current loop. The output of voltage loop is involved in the current reference calculation. To investigate the effects of the voltage loop on the current loop bode plot measurement, the current loop bode plot is measured with voltage loop open and closed. A fixed value is used to represent voltage loop output when it is open. It can be seen from Fig. 3 that these two bode plots almost overlap, a well tuned voltage loop almost has no effects on the current loop. Based on this, to simplify the measurement in real application, the voltage loop can be closed when measuring current loop.

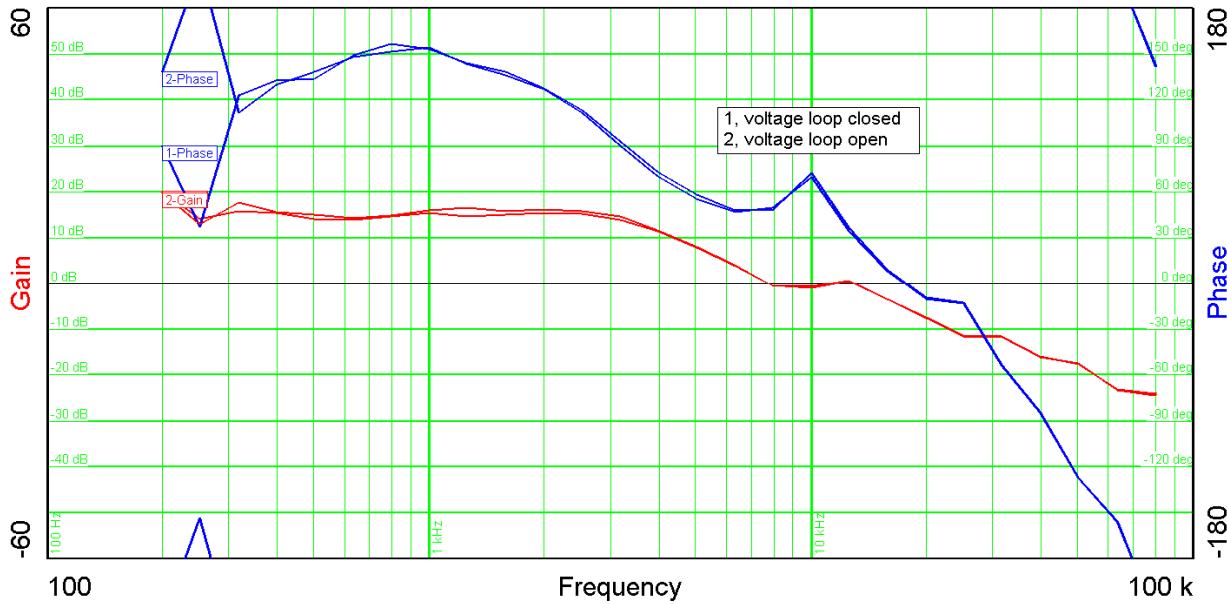


Fig. 3. Voltage loop effects on current loop

1.3 Input source effects on current loop bode plot

Another big concern is the input source when measuring current loop Bode plot. With AC input, the varying input causes the varying PWM duty cycle, what the frequency analyzer measures is the small signal response plus the variation of PWM duty cycle, which may not represent the real characteristic of the system. To investigate the effects of the input source on the current loop Bode plot measurement, Fig. 4 shows a comparison of current loop Bode plot with AC and DC input. The Bode plots show that at low frequencies (which we don't care about), the Bode plots are quite different. At higher frequency range, they get closer and closer and eventually overlapped each other. They also show the same bandwidth and similar phase margin. Based on this, to simplify the measurement in real application, we can use AC input when measuring current loop Bode plot.

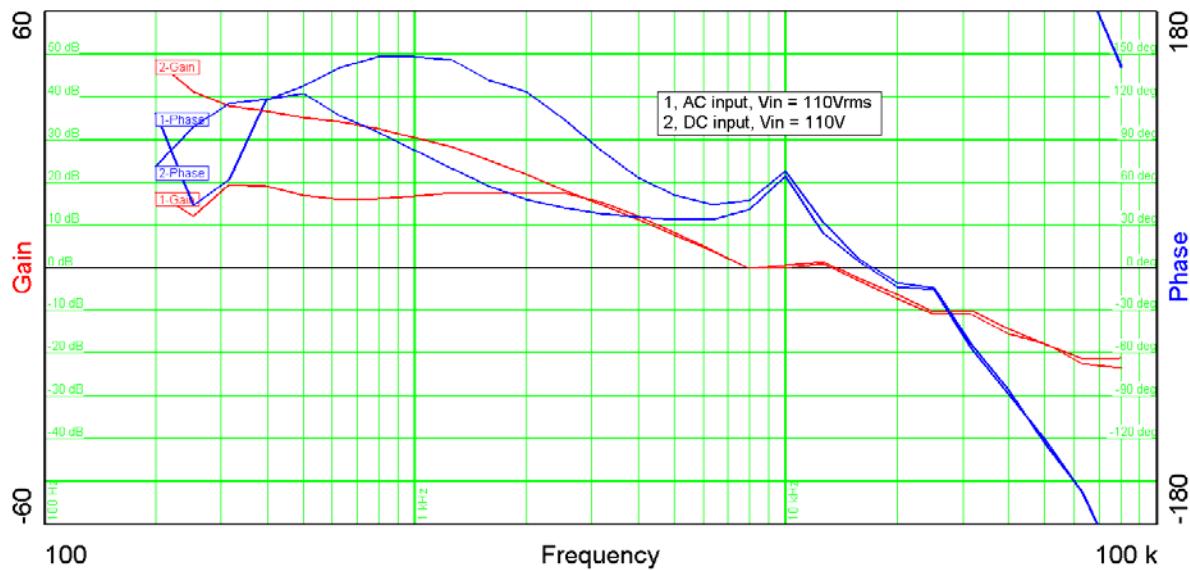


Fig. 4. Input source effects on current loop

1.4 CCM vs. DCM

An average current mode controlled PFC normally operates at continuous conduction mode (CCM), therefore the PFC is normally tuned at CCM mode. At light load, the PFC may enter discontinuous conduction mode (DCM), the loop gain and bandwidth reduce significantly, as shown in Fig. 5. The loop gain and bandwidth can be increased by increasing the control gain, however, the bandwidth will be too high once PFC enters CCM mode. This fact makes the compensator very sensitive to noise. The phase margin is also reduced with this high gain in CCM mode. In fact, the deteriorated waveform with high THD in DCM mode is not only caused by the low bandwidth, but also by other factors. Special techniques will be used to reduce THD at DCM, these will be addressed in section 5, 6, 7.

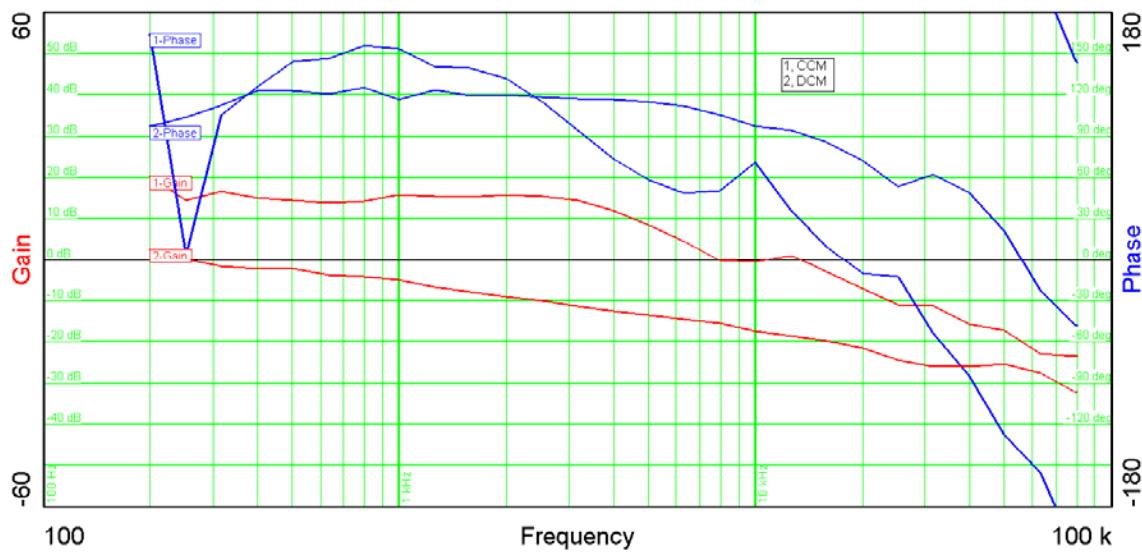


Fig. 5. Bode plot at CCM vs. DCM

2 UCD3138 Digital Compensator

UCD3138 digital compensator is a PID based structure with an additional α coefficient to provide 2-pole, 2-zero compensation. The compensator structure is shown in Fig. 6.

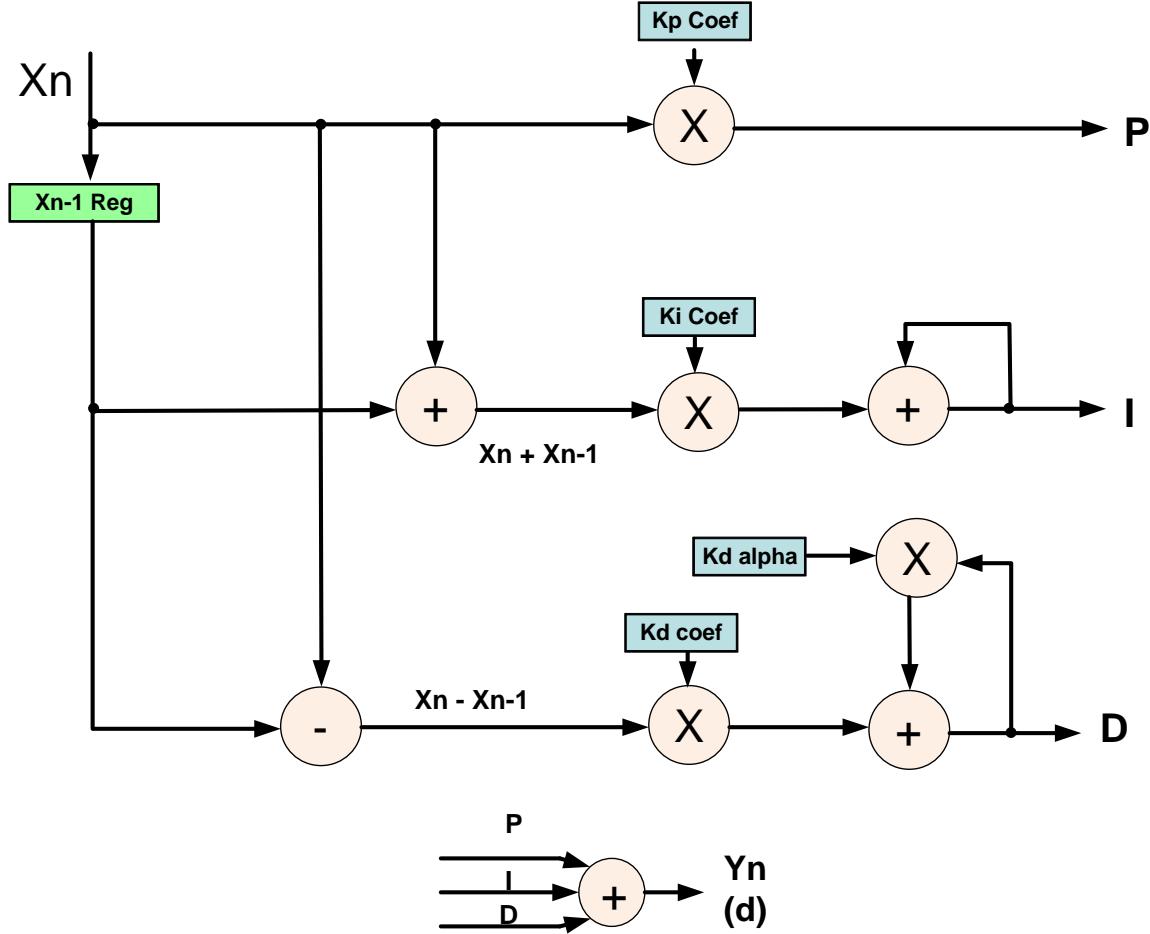


Fig. 6. UCD3138 PID structure

The mathematic equation of this compensator is shown in (1). Now the goal is to find the appropriate K_P , K_I , K_D and α such that current loop has sufficient bandwidth, phase margin and gain margin.

$$G(z) = K_P + K_I \frac{(z+1)}{(z-1)} + K_D \frac{z-1}{z-\alpha} \quad (1)$$

3 Tuning a PFC Current Loop

3.1 Get initial compensator coefficients

The example used here is a 360W single phase PFC controlled by a UCD3138. The test conditions are: $V_{in} = 110V$, $V_{out} = 390V$, Load = 150W. This results in the PFC operating in CCM mode. Let's assume there is no

compensator to start with (e.g. K_p , K_i , K_D and α are all 0). Obviously there is no PWM output; the resulting current waveform is shown in Fig. 7

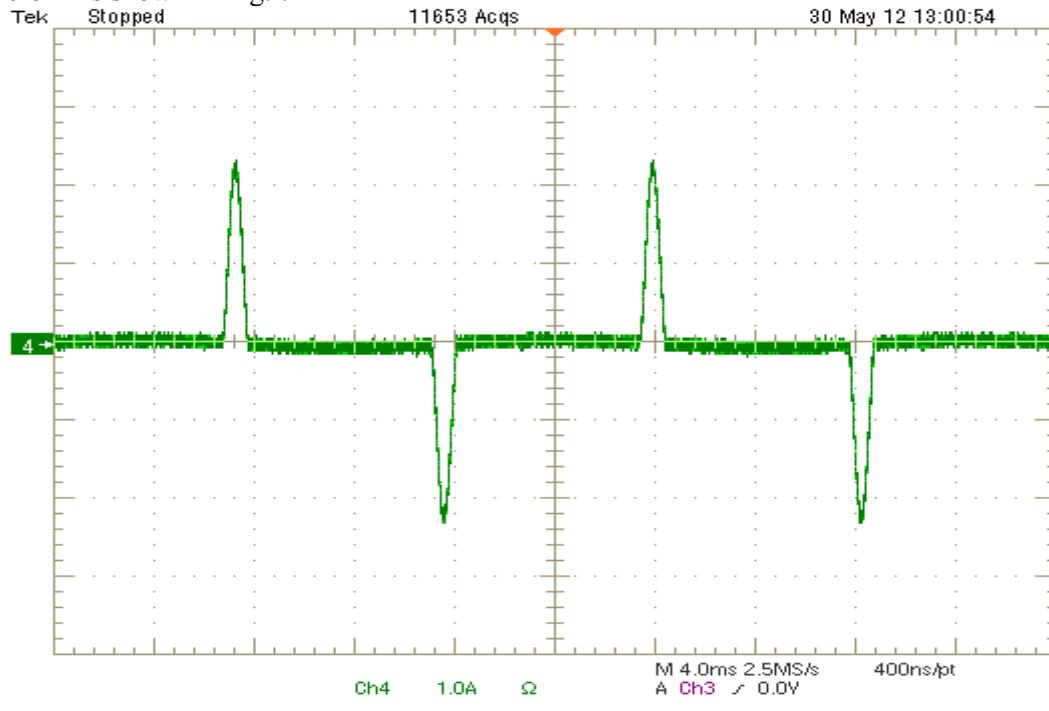


Fig. 7. Current waveform with no compensator

Now we need to find an initial compensator so that the current loop can be closed with stable output, then we will tune from there. Open “Fusion Digital Power Designer”, type in all the power stage parameters in “Design” tab. The GUI will generate the power stage bode plot based on these parameters.

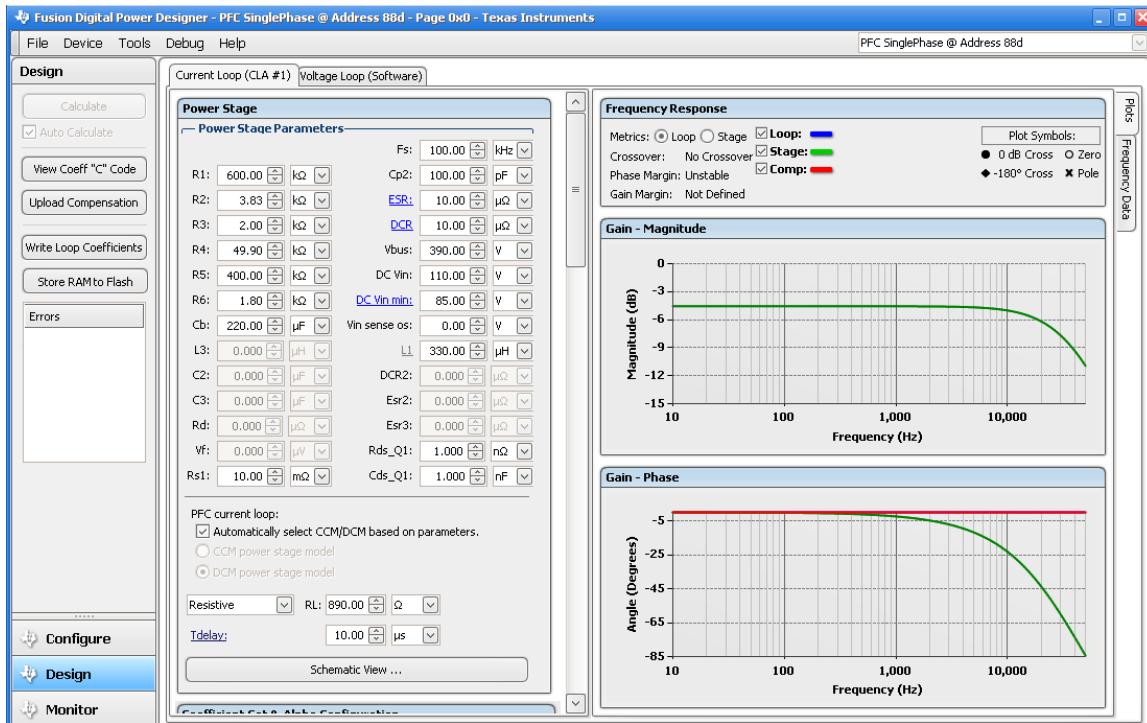


Fig. 8. Enter PFC power stage parameters

Now in the same “Design” tab, enter the initial PID control parameters, the GUI will show the loop bode plot based on these parameters and power stage. It will also show the bandwidth, phase margin and gain margin. As mentioned earlier, it is difficult to get an accurate PFC power stage model because the power stage parameters getting from datasheet are usually not accurate enough. This means that the bode plot displayed in the GUI may not represent the real system. However, our goal is just to get a stable compensator, therefore the plot does not have to be very accurate, it just need to tell us a rough idea how the control loop will be. To make sure the loop is stable, the bandwidth should be low and the phase margin should be high. As shown in this example, after entering these parameters:

$$K_p = 50, K_i = 10, K_d = 0, \alpha = 0$$

The GUI shows the loop bandwidth is 179Hz, and phase margin is about 90 °, as shown in Fig. 9. The control loop should be stable with these parameters. Click “Write Loop coefficients” and these PID coefficients will be downloaded to the controller and the current loop will start to use this compensator to control the current.

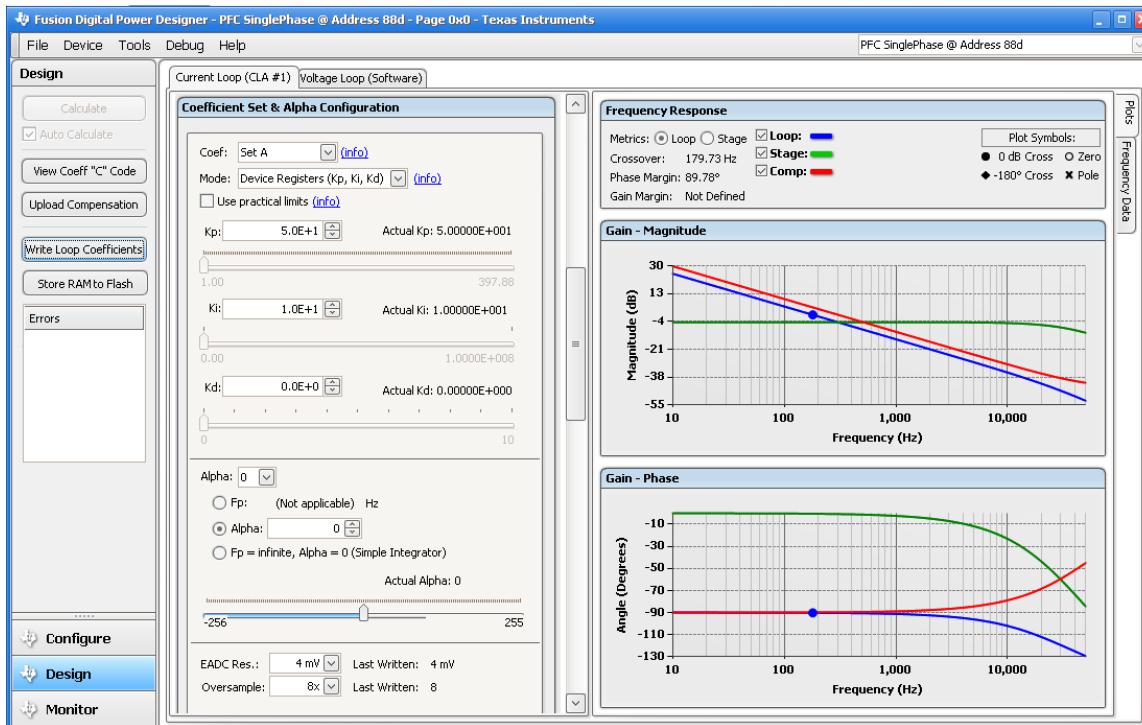


Fig. 9. Enter initial PID coefficients

The current waveform with these initial coefficients is shown in Fig. 10. It is stable as expected, however, the THD is only 10.15% and PF is 0.99. Next, we will fine tune the loop to achieve better performance.

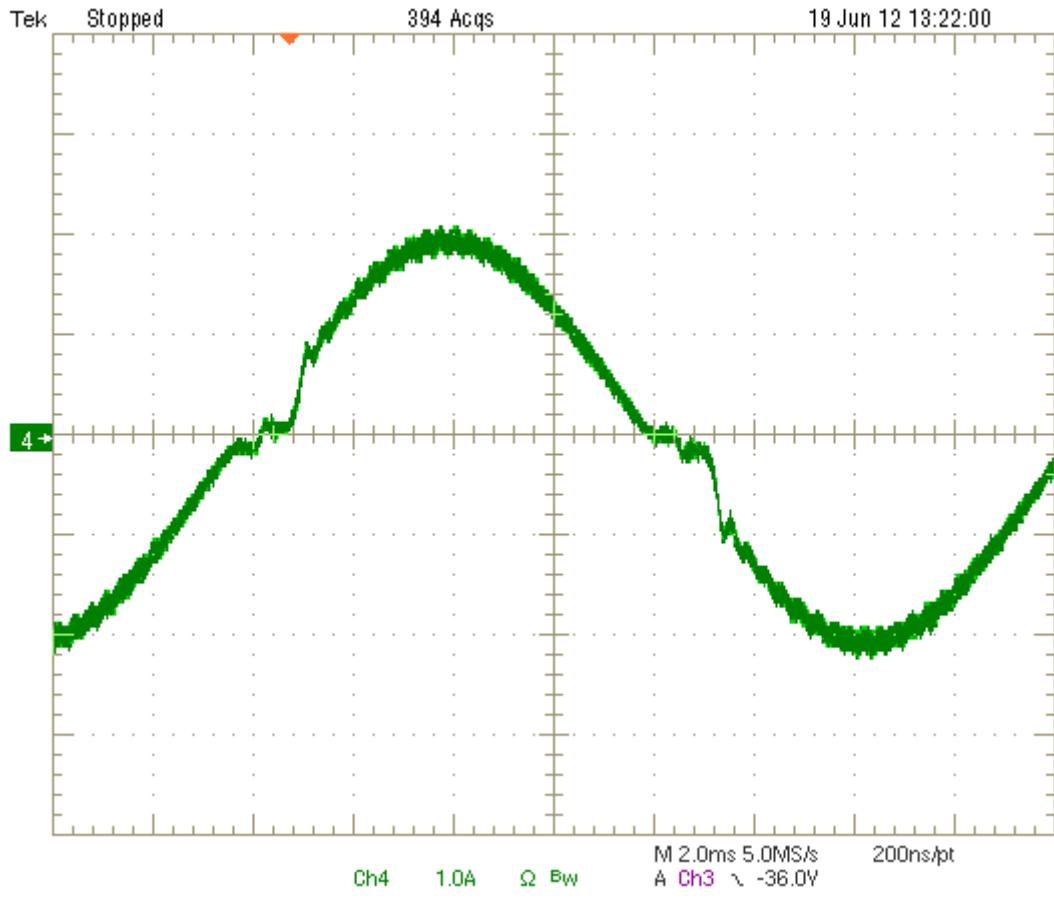


Fig. 10. Current waveform with initial coefficients

3.2 Tuning 1-pole 1-zero compensator

The waveform shown in Fig. 10 is a sine wave with some significant distortion. Furthermore, there is some high frequency ripple at the peak area. Generally, bandwidth affects the waveform shape and phase margin determines how smooth the waveform will be. The waveform in Fig 10 indicates that both bandwidth and phase margin are too low. We need to tune the poles/zeros to get appropriate bandwidth and phase margin. But before that, we need to know what the current gain, poles and zeros are.

Note if the current ripple on the top of the AC line current has uneven amplitude and irregular frequencies, it could be caused by a dirty current feedback signal. The current sensing noise should be minimized prior to attempting to fine tune the loop.

In the “Fusion Digital Power Designer”, change the coefficients mode from “Device registers (K_p , K_i , K_d)” to “Real Zeros (K , $Fz1$, $Fz2$)”, the GUI will change the initial coefficients from the PID format to a pole/zero format, as shown in Fig. 11:

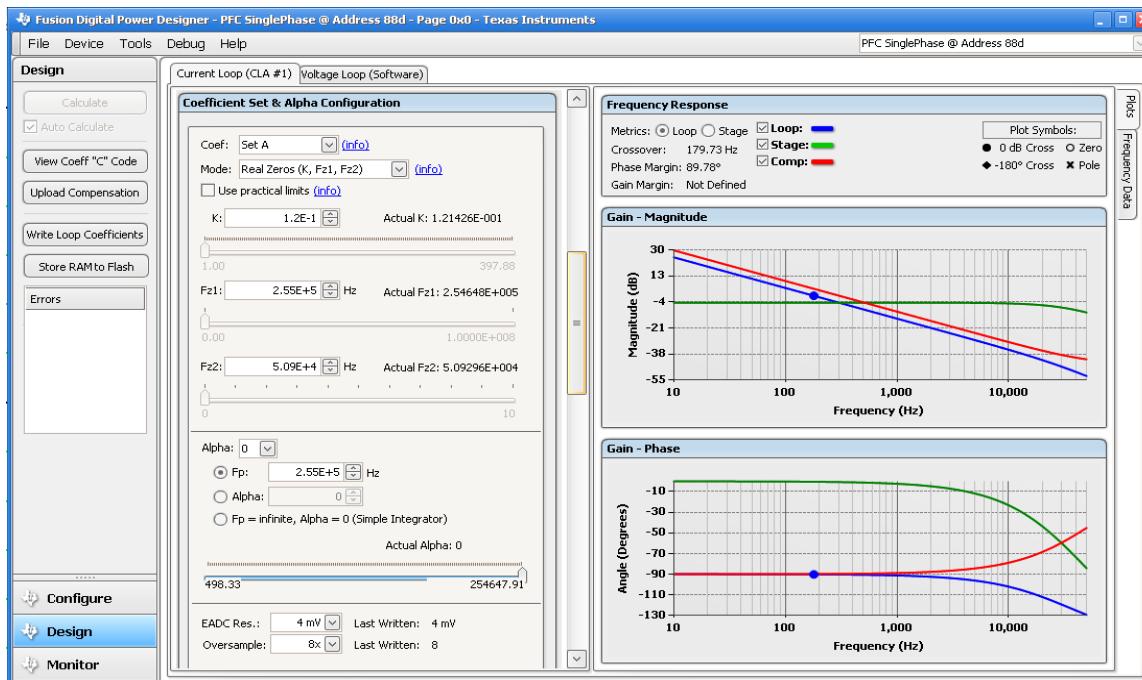


Fig. 11. Initial coefficients in pole/zero format

$$K = 0.12, Fz1 = 255\text{KHz}, Fz2 = 50.9\text{KHz}, Fp = 255\text{KHz}$$

This is the compensator we are currently using. It is a pure PI controller, the first zero and pole are far away and cancel each other; they have no effect on the current loop performance. Now we need to tune the gain K and second zero Fz2 so that the loop has good bandwidth, phase margin and gain margin.

Now use Venable to measure the bode plot with these initial coefficients:

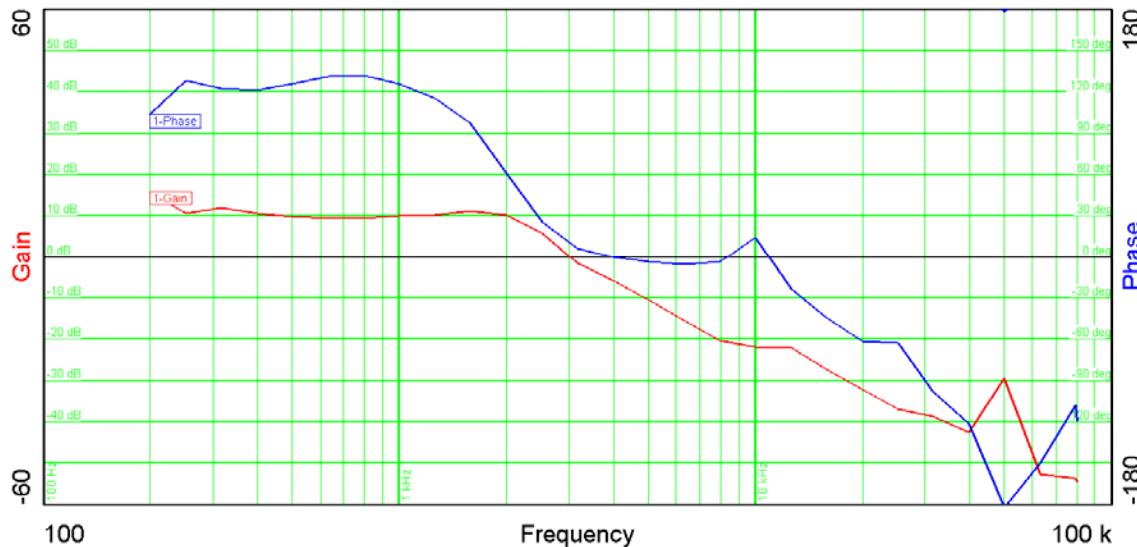


Fig. 12. Bode plot with initial coefficients

From the Bode plot in Fig. 12, the bandwidth is only 3KHz, and the phase margin is only about 13° . That explains why the current waveform has distortion and also the high frequency ripple. To have good current loop performance, the bandwidth needs to be around 8KHz, and phase margin needs to be $> 40^\circ$. Let's increase the phase margin first. In the GUI, move Fz2 to 5KHz, then click “Write Loop coefficients”, the new coefficients with Fz2 = 5KHz is now taking over the control. Use Venable to measure the Bode plot again. Fig. 13 is the bode plot after moving Fz2 to 5KHz:

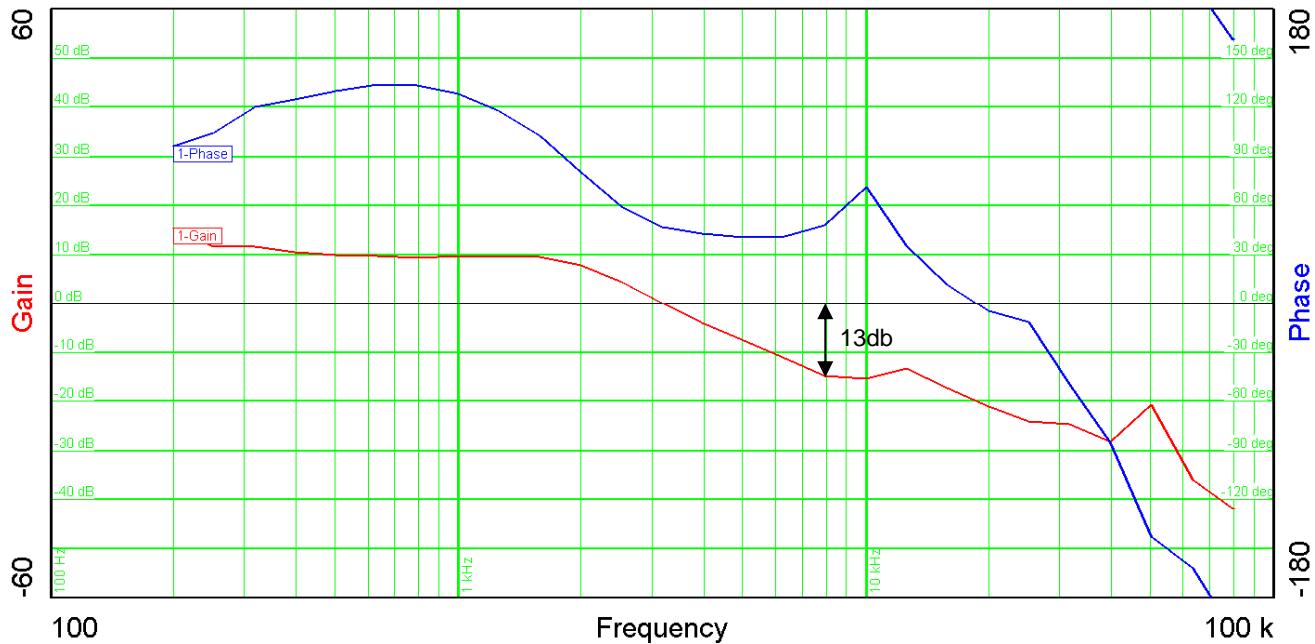


Fig. 13. Bode plot after moving zero

It can be seen that now the phase margin is increased to about 45 degree, the loop should be stable with this phase margin. It can also be seen that the gain is about -13db at 8KHz. To have a bandwidth of 8KHz, the gain needs to be increased by about 13dB. Therefore, the new gain will be:

$$K = 0.12 * 13\text{dB} = 0.53$$

Now in the GUI increase K to 0.53. Download these new coefficients, and measure the bode plot again, as shown in Fig. 14:

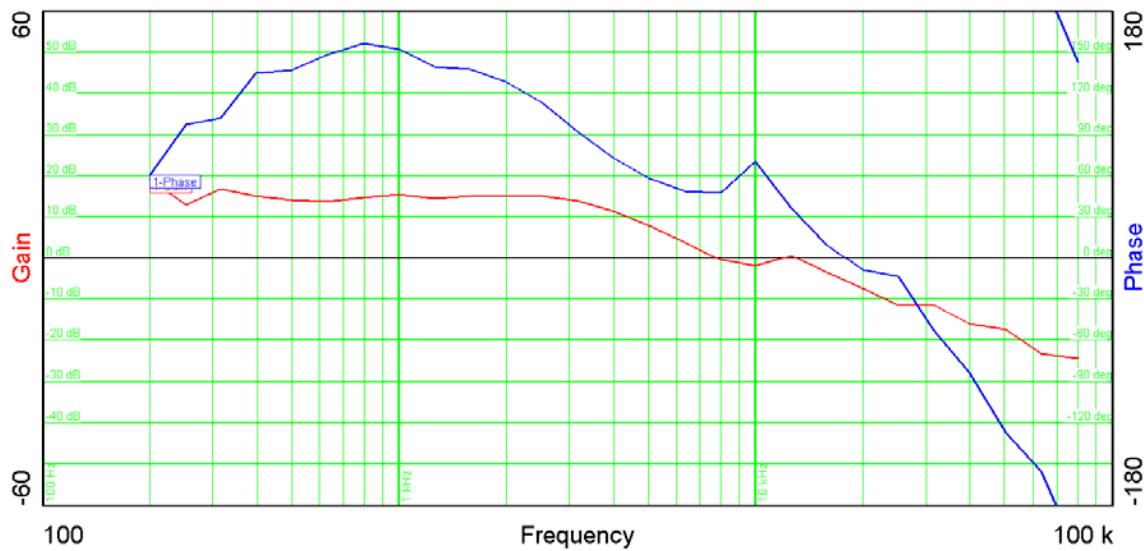


Fig. 14. Bode plot after increasing gain

Now bandwidth is about 8KHz, and phase margin is about 45 degree, both of them meet our requirements. With these new coefficients, the current waveform gets much better, as shown in Fig. 15. THD is reduced from 10.15% to 7.45%, PF is increased from 0.99 to 1. Furthermore, the previous observed high frequency ripple goes away.

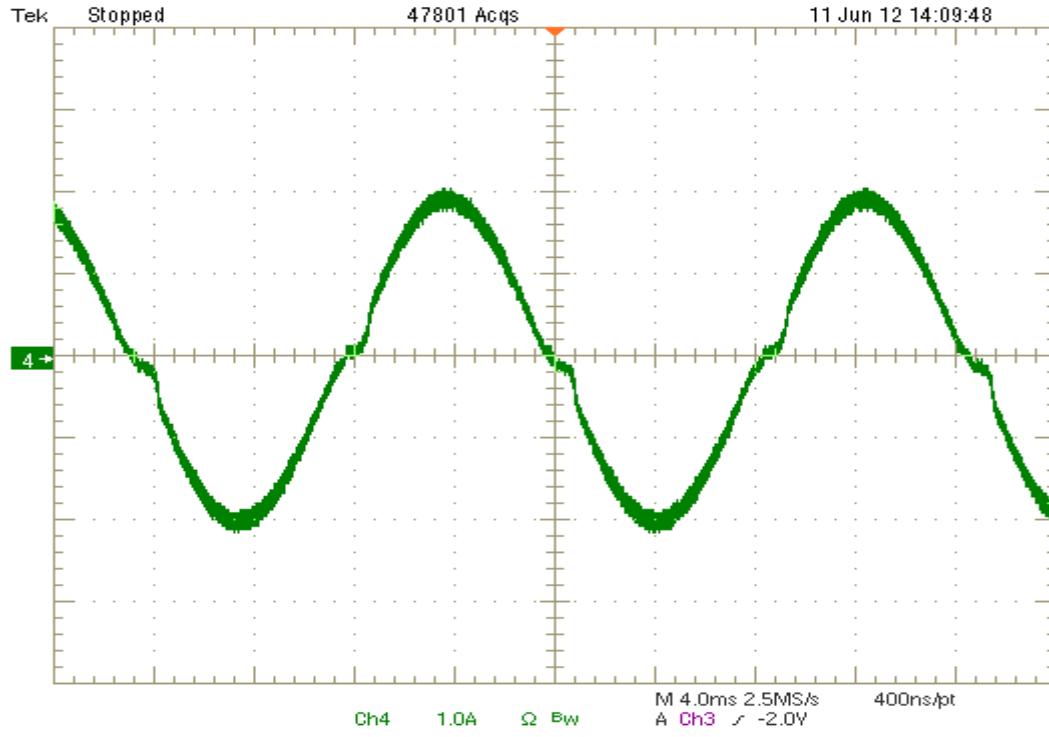


Fig. 15. Current waveform with new coefficients

Fig. 16 shows the new coefficients after these tuning. The coefficients are in pole/zero format:

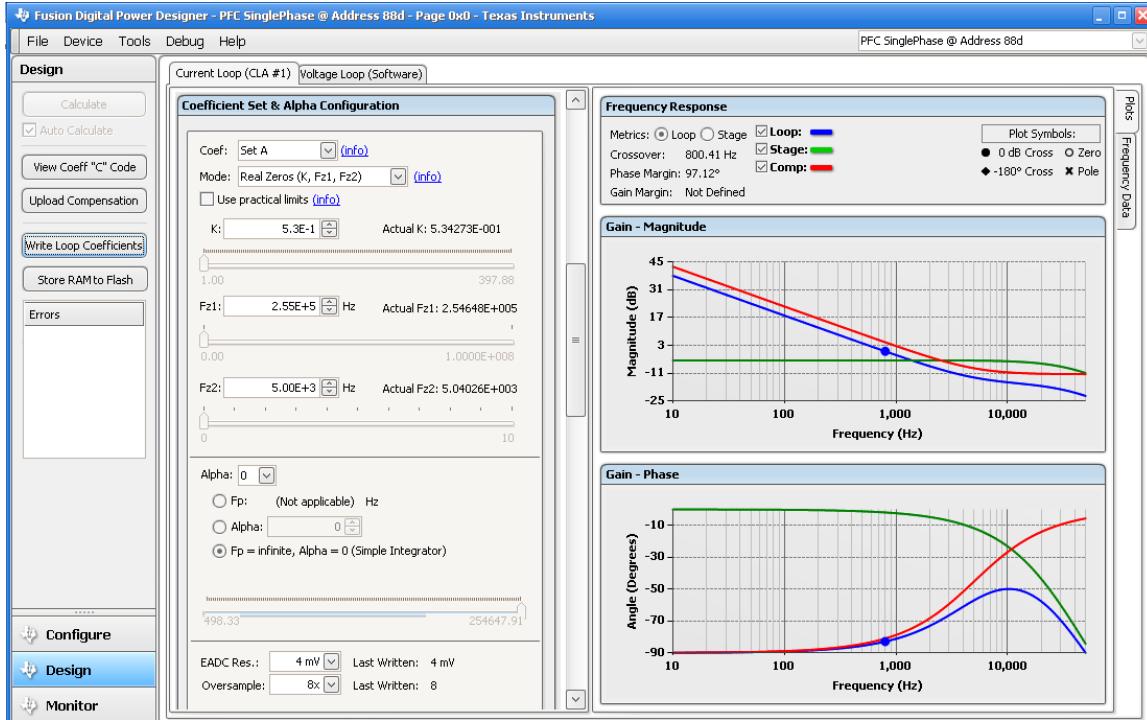


Fig. 16. New coefficients in pole/zero format

These new coefficients have good performance, we want to keep them and put them in firmware, however, the control loop registers inside UCD3138 only takes PID, not pole/zero. In “Fusion Digital Power Designer”, change the coefficients mode from “Real Zeros (K, Fz1, Fz2)” to “Device registers (kp, ki, kd)”, the GUI will change the coefficients from pole/zero format to PID format, as shown in Fig. 17:

$$K_p = 2223, K_I = 44, K_D = 0, \alpha = 0$$

Now we can put these values in the firmware, the PID coefficient tuning is done for low line.

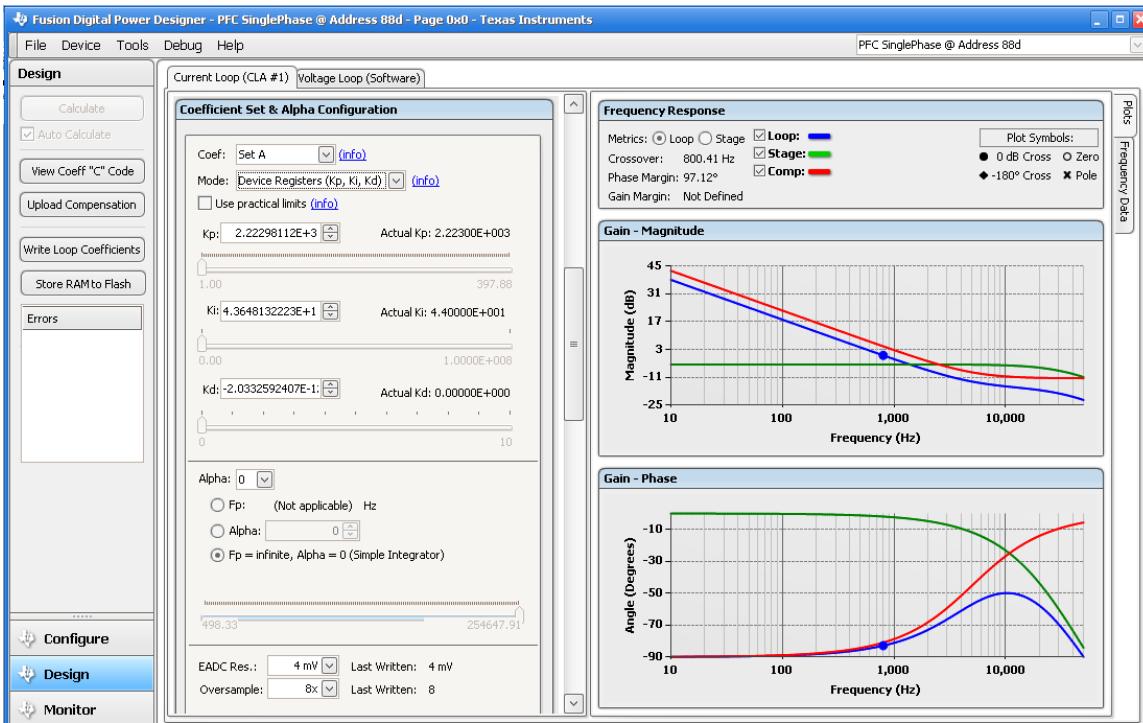


Fig. 17. New coefficients in PID format

3.3 Tuning 2-pole 2-zero compensator

The final compensator used above is a pure PI compensator with only 1-pole and 1-zero, this is normally good enough for the PFC current loop, since the PFC current loop is normally a first order system. In some application, 1-pole and 1-zero may not be able to meet the requirement, then the second pole and zero can be used. The tuning procedure for the second pole/zero is similar as above. For example, if we want to further increase the phase margin while still keeping the bandwidth at 8 kHz, based on the bode plot of Fig. 13, move Fz1 to 4 kHz to further increase the phase margin, then move Fp to 10 kHz so that the loop gain will have a rapid decrease after crossover frequency. Measure the bode plot with these new 2-pole and 2-zero compensator, then tune the gain to get 8KHz bandwidth based on the bode plot. In this example, the new 2-pole 2-zero compensator is tuned as:

$$K = 0.32, Fz1 = 4 \text{ kHz}, Fz2 = 5 \text{ kHz}, Fp = 10 \text{ kHz}$$

The bode plot with this 2-pole 2-zero compensator is shown in Fig. 18:

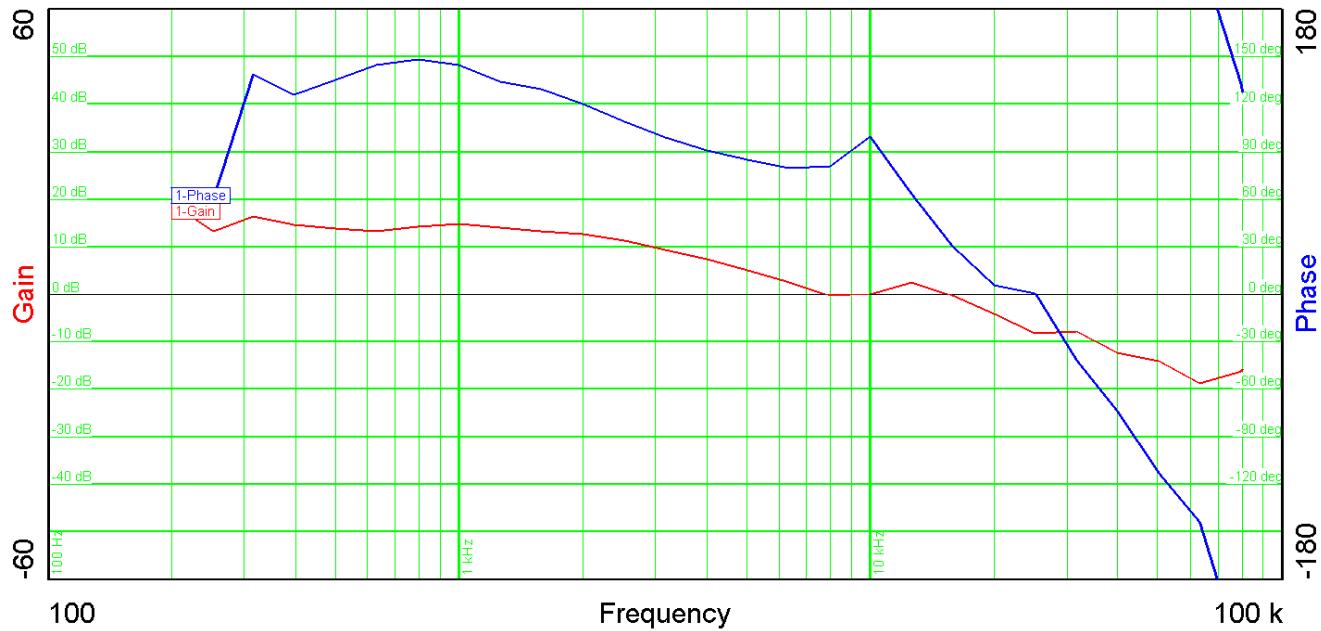


Fig. 18. Bode plot with 2-pole 2-zero compensator

With this 2-pole 2-zero compensator, the phase margin is further increased to about 80° , while bandwidth is still kept at 8 kHz. The PFC operating in this condition will be very stable with good waveform.

4 Adding Current Reference Offset

Fig. 15 shows a flat area at zero-crossing. This is because when the PFC enters DCM, the boost inductor current starts to decrease when the MOSFET is turned off. The current will not stop decreasing when it reaches zero. Rather, it will continue to go to negative and an oscillation between the inductor and the total parasitic capacitance at the switching node occurs. The negative current will not show up at the output of the current amplifier. Therefore, the amplifier output does not represent the total inductor current. This is illustrated in Fig. 19. The dashed line is the real inductor current, but only the positive part (the solid line) gets measured. Furthermore, some current amplifiers, especially the low cost ones, usually are not able to pull its output down to zero volts at zero input. It may still have a small positive output at zero input. Therefore, the measured average current is bigger than the real inductor average current. This inaccurate feedback signal will cause input current distortion at the AC voltage zero-crossings and deteriorate the THD.

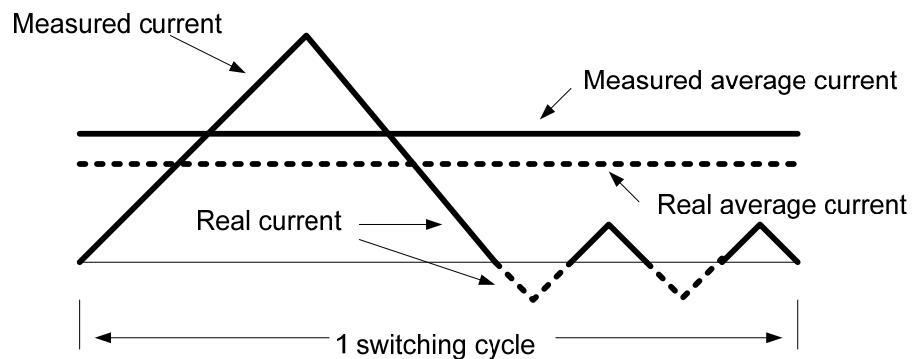


Fig. 19. Current measurement error due to negative current

To deal with this measurement issue, a simple way is to add a DC offset on its calculated current reference to compensate the current measurement error. This can be done by just adding a few lines of code in the firmware. Fig. 20 shows the waveform after adding a small current reference offset. The flat spot at the zero-crossing goes away, and THD is reduced to from 7.45% to 2.47%.

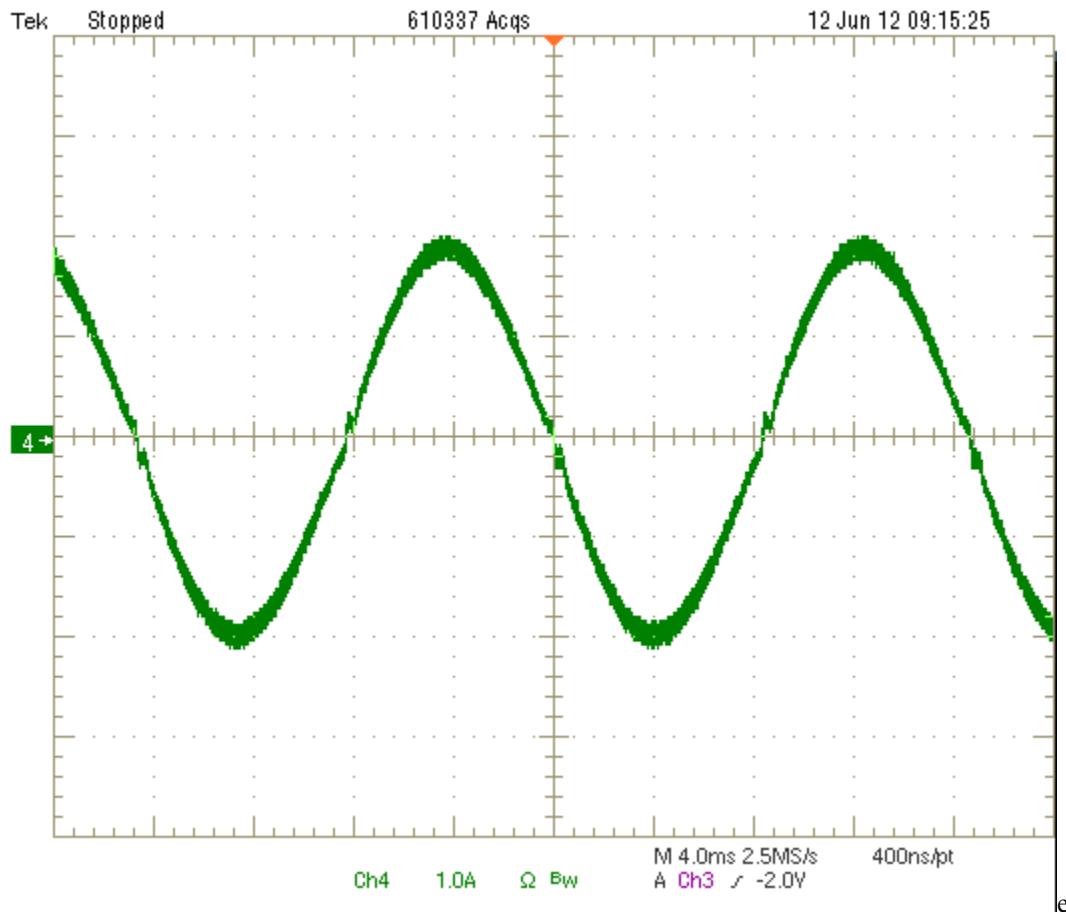


Fig. 20. Current waveform after adding current reference offset

The above analysis applies not only to current shunt sensed PFC, but to current transformer (CT) sensed PFC as well.

Please note that when the load is reduced to zero, the current feedback signal is almost zero, and this DC offset will cause the control loop to continue generating PWM pulses, thus the PFC output voltage will rise up and eventually trigger over voltage protection (OVP). To prevent this, the firmware needs to clear this DC offset at no load.

5 Dynamic Loop Compensation

So far we have tuned a very good current loop compensator for low line. However, the PFC electrical characteristics may vary a lot at different input voltages and load. Proper loop compensation at low-line may not work well at high-line, and the bandwidth of a well tuned compensator at CCM may be reduced too much when operating at DCM. It is desirable that the loop compensation be dynamically adjusted based on the input voltage or load.

The UCD3138 has several sets of coefficient registers. It can store up to 7 sets of different PID coefficients. With this flexibility, we can store several different coefficient sets in firmware. For example, use two different coefficients, one is optimized for low line and the other is optimized for high line. The coefficients will be dynamically swapped based on the input voltage. The loop bandwidth, phase margin and gain margin can therefore be optimized at both low line and high line. The low line coefficients determined previously can be used as the starting point for high line tuning. Repeat procedure in section 3.2 to fine tune the coefficients for high line.

Similarly, we can use different coefficients for different loads. For example, use a higher gain for DCM mode to compensate the reduced bandwidth.

6 Oversampling

Using a current shunt to sense a boost inductor current is very common in PFC design. An operational amplifier is used to amplify the current signal to a level suitable for the PFC control circuit. However, this current signal conditioning circuit does not provide sufficient attenuation to the input current ripple. The current ripple still appears at the output of the amplifier. Therefore, if this signal is sampled only once in each switching period, there is no perfect location where the signal represents the average current all the time. Hence, with a single sample, it is very difficult to achieve good THD.

In UCD3138, in addition to the normal single sample per period, it can also do 2X, 4X, 8X oversampling. An 8X oversampling mechanism is shown in Figure 21. With this oversampling capability, the current signal can be sampled and the converted data be loaded to the digital compensator eight times each switching cycle. It effectively averages the current ripple out such that the measured current signal gets closer to the average current value. Also, the controller becomes less sensitive to noise.

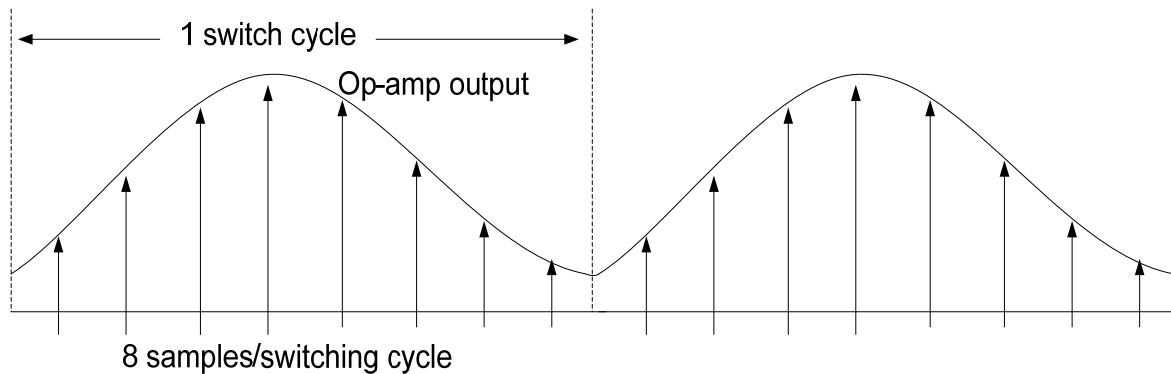


Fig. 21. 8X oversampling

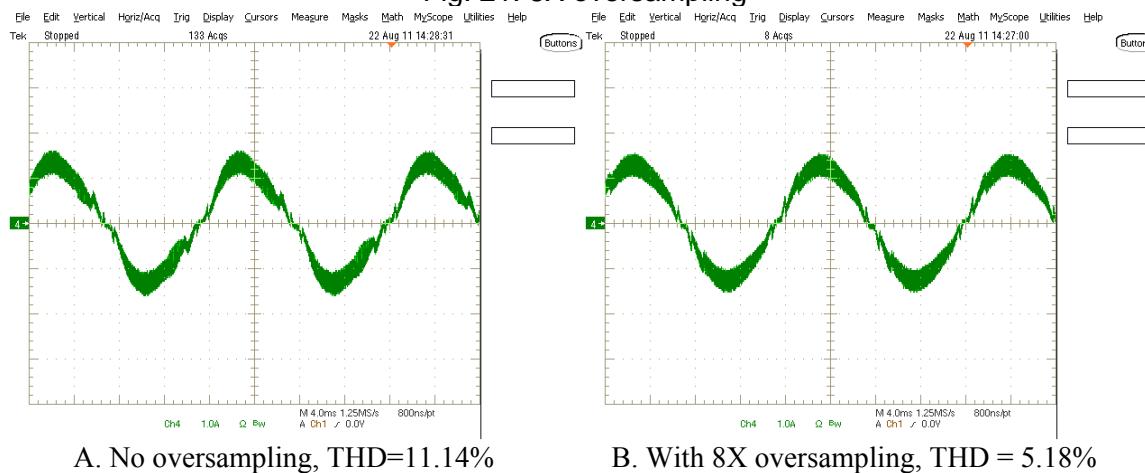


Fig. 22. Oversampling test

An oversampling test result on a 360W single phase PFC is shown in Fig. 22. With all the same operation conditions, the THD is reduced from 11.14 percent to 5.18 percent by just enabling 8X oversampling.

7 Current Distortion Reduction at DCM Mode

As mentioned before, in DCM, once the boost inductor current declines to zero, the boost inductor resonates with the PFC MOSFET's parasitic capacitance. The resonant current can be big enough to distort the PFC current significantly. Depending on the MOSFET's turn-on time, the resonant current contributes to average current in a different way in each switching cycle. In other words, the resonant current adds to the switching current in one switching cycle, but in the next switching cycle, the current is subtracted from the switching current, which causes large current steps, as shown in Fig. 23. Since this effect occurs at much higher frequency than a PFC's current loop bandwidth, the current loop cannot regulate the boost inductor current fast enough to compensate the abrupt current disturbance.

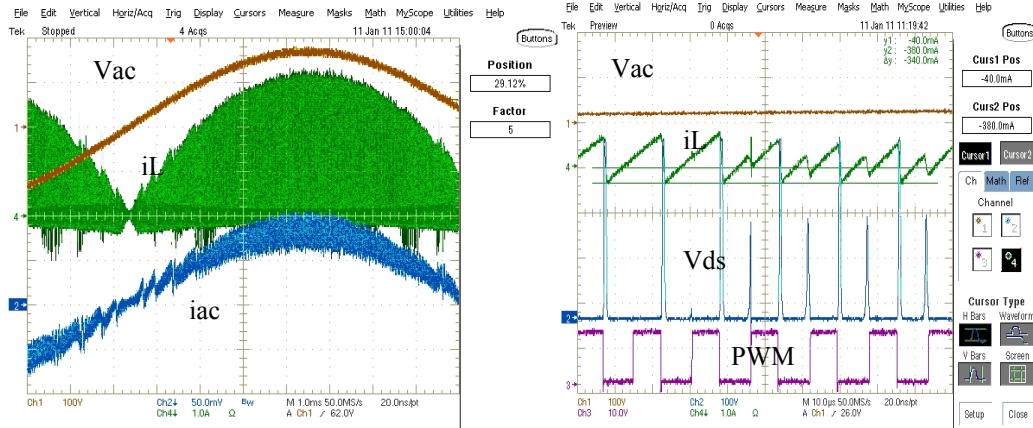


Fig. 23. Current oscillation in DCM

A new control method developed by TI [2] can force the MOSFET to turn on at the point when the oscillating current first time rising back from negative value to zero. Since the MOSFET always turns on at the same zero current position, the issue described above is solved, and the current distortion is greatly reduced. Also, because of zero voltage switching (ZVS) and zero current switching (ZCS), the efficiency is also improved.

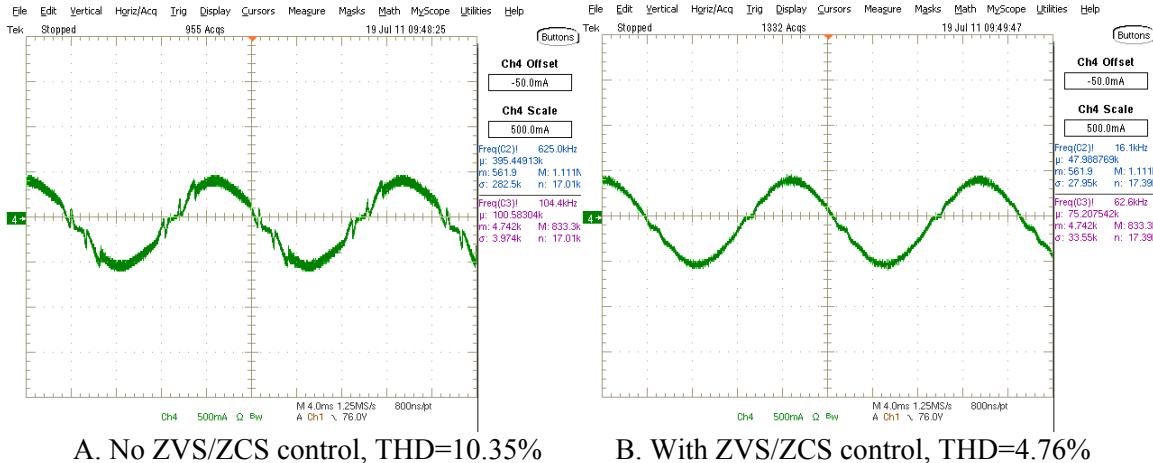


Fig. 24. ZVS/ZCS control test result

Fig. 24 is a comparison test without and with this new ZVS/ZCS control algorithm on a 360W single phase PFC. With all the same operation conditions, the THD is reduced from 10.35% to 4.76% by applying this new control algorithm.

8 Adding Sample Trigger Offset

For a PFC with CT current sensing, since only the inductor rising current (when MOSFET is turned on) is measured, the current needs to be sampled at a specific position; for example, the middle of the PWM pulse, so that this instantaneous current can be translated into an average current by a specified mathematical equation. However, due to the gate driver circuit and power stage delay, the real inductor current will delayed a certain time, compared with the related PWM pulse. The actual mid-point of the MOSFET on-time is a little bit later

than the mid-point of the PWM pulse. To compensate this delay, a sample trigger offset needs to be added, as shown in Fig. 25.

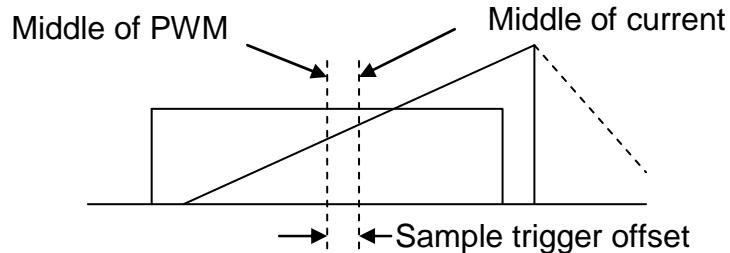
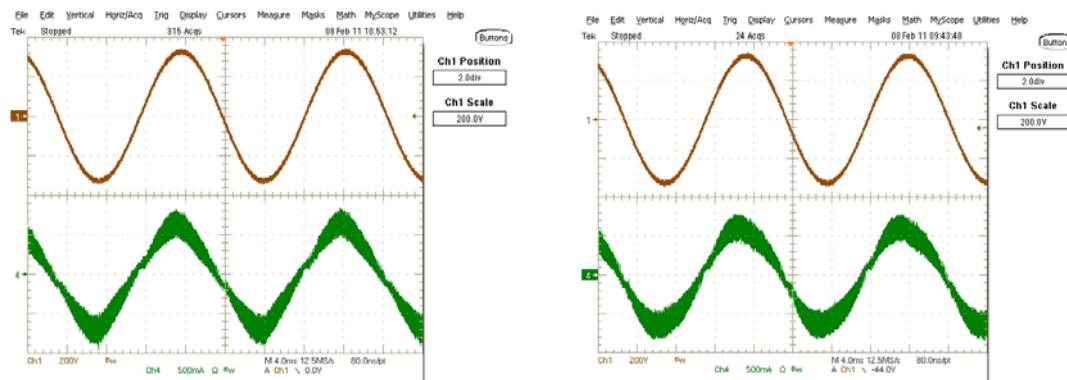


Fig. 25. Current signal delay and sample trigger offset



A. No sample trigger offset, THD = 7.85%

B. With sample trigger offset by 512ns, THD = 5.86%

Fig. 26. Adding sample trigger offset to reduce THD

Fig. 26 is a test result with this sample trigger offset on a 360W bridgeless PFC test board. The test shows that with all the same operating conditions, the THD is reduced from 7.85% to 5.86% by adding a 512ns sample trigger offset.

9 Harmonic Injection

For a high end PFC design, it not only requires the THD not exceeding a certain percentage with a specific load, but also requires each of the individual harmonics not exceeding a specific limit, as defined in IEC 61000-3-2. Sometimes a new PFC design can pass the THD test, but failed with individual harmonics distortion test. How to reduce a specific order of harmonic distortion is a big challenge in PFC design.

A harmonics injection method is developed such that the harmonics with high magnitudes will be suppressed actively [3].

10 EMI Filter X-CAP Reactive Current Compensation

A typical FPC converter has an electromagnetic interference (EMI) filter at the input end, the X-Cap of the EMI filter will cause the AC input current leading AC voltage, as shown in Figure 27. Although the PFC current control loop force the inductor current I_L to follow V_{AC} , the reactive current of X-Cap I_C leads V_{AC} by 90 degree,

which causes the total current \bar{I}_{AC} leads \bar{V}_{AC} . This results a poor PF. This situation gets worse at light-load and high-line. The PF will be difficult to meet a rigorous specification.

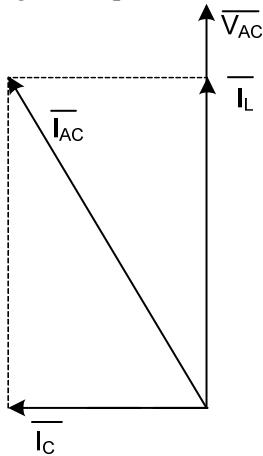


Figure 27, X-Cap reactive current cause AC current leading AC voltage

A novel X-Cap reactive current compensation method is developed and a high PF can be achieved [4].

11 Reduce the Voltage Loop Effect

Although with a much lower bandwidth, the voltage loop will still affect THD more or less. To eliminate the effects of voltage loop as much as possible, it is recommend to:

- 1, use small control gain
- 2, add a digital filter for the sensed Vout and, use the filtered Vout signal for the voltage loop control.

These will put the voltage loop at a very low bandwidth. To meet the transient response requirement, a nonlinear control is necessary. When Vout deviates from the setpoint too much:

- 1, switch to larger gain
- 2, use the instantaneous Vout signal for voltage loop control

Reference

- [1]UCD3138 datasheet
- [2]slua644, TI application note
- [3]TI application note: A Harmonic Injection Method to Reduce PFC Harmonics and Improve THD
- [4]TI application note: A Novel EMI Filter X-CAP Reactive Current Compensation Method to Increase PF

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