Application Report
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Layout Guidelines for Wireless Power Receiver

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ABSTRACT

Printed-circuit board (PCB) layout becomes more complex as device pin density increases, power demand gets higher, and the system board size decreases. A successful wireless power receiver board must effectively integrate all devices and other elements of the system while staying within the recommended thermal budget, avoiding system noise problems, minimizing cross talking between traces, and creating the smallest size solution possible. This application note provides layout guidelines on the third generation wireless power receiver design that includes the bq51221, bq51020, and bq51021 devices.

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1 Traces

Most applications of wireless power receivers are on portable devices. The size and weight of these products is critical. With dramatic increase on component count, the PCB space quickly becomes limited. Designers must decide on board dimensions, component placements, layer counts, and traces routing effectively to meet these challenging requirements.

In wireless receiver layout design, component placement and traces are important. This section provides a description of different traces in wireless power receivers. There are three types of traces: signal and sensing, noisy, and power traces.

1.1 Signal and Sensing Traces

Signal and sensing pins are responsible for sensing and receiving signals. These traces carry small signals to the device, such as measuring the temperature of the battery through TS pin, receiving the power measurement for FOD detection, control signals from the EN1 and EN2 pins, I2C communication such as SCL and SDA, and so forth.

Signal and sensing traces are the most sensitive to noise; the sensing signal amplitudes are usually measured in mV, which is comparable to the noise amplitude of power traces. Make sure that noisy and power traces are not interfering with signal and sensing traces.

High dv/dt voltage change on one conductor will couple currents to another through the parasitic capacitance. To reduce the noise coupling from the noisy traces, it is necessary to keep the noisy switching paths far from the sensitive small signal traces. If possible, route the noisy and sensitive traces on different layers, with an internal ground layer in between for noise shielding. The following is a list of signal and sensing pins of the bq51221 and bq5102x device family:

- **ILIM:** Charge current / overcurrent level programming pin. Any noise will affect the current limit accuracy or even can cause fluctuation in the output voltage.
- **AD and AD_EN:** Adapter sensing and AD _EN pins.
- **TS/CTRL:** Temperature sense. Temperature thresholds accuracy will not be possible with noisy trace.
- **FOD:** Inputs that are used for scaling the Received Power Message. Choose resistor to ground based on FOD Calibration procedure. If noise is interfering with this trace, the FOD calibration will be harder and certification of wpc1.1 will be a challenge.
- **TMEM:** This pin allows the capacitor to be connected so energy from Transmitter Ping can be stored to retain memory of state. This is important for detection of the right mode in the bq51221 device.
- **SDA and SCL:** These pins are used for I2C communication. The data and clock are high frequency and very sensitive impedance tracking and noise. Make sure these traces are as short as possible. Also, a 200-Ω resistor in series is always a good practice.
- **LPRB1 and LPRB2:** These pins are open drain – will be active to help drive RECT voltage high at light load.
- **VOREG and VIREG:** Output voltage regulation setting and input voltage feedback. These are feedback pins, any noise is seen directly at the output.
- **TERM:** Sets termination current as a percentage of ILIM. Especially at low power applications, any noise is amplified and affects the termination threshold and accuracy.
- **$\overline{\text{WPG}}$:** Open Drain output that allows the user to sense when power is transferred to load.
- **CM_ILIM:** Enables or disables Communication Current Limit. Pull high to disable COMM ILIM. Pull low to enable COMM ILIM.
- **$\overline{\text{PD\_DET}}$:** Open drain output that allows the user to sense when receiver is on transmitter.
- **COMM1 and COMM2:** Open-drain output used to communicate with primary by varying reflected impedance. Isolating this from noisy traces is a must. The noise can affect communication and can cause malfunction of the whole system. This trace also can cause noise to other traces during communication.

1.2 Noisy Traces

AC1, AC2, BOOT1, BOOT2, COMM1, and COMM2 are the main source of noise in the board. These traces should be shielded from other components in the board. It is usually preferred to have a ground copper area placed underneath these traces to provide additional shielding. Also, make sure they do not interfere with the signal and sensing traces.

1.3 Power Traces

The power traces includes the components that conduct high current such as AC1, AC2, OUT, PGND return, CLAMP1, and CLAMP2. In general, they should be placed first and sized properly. Then, small signal paths are subsequently placed in specific spot in the layout. The large current traces should be short and wide to minimize PCB inductance, resistance and voltage drop. This is especially critical for the traces with high dv/dt pulsating current flow.

2 Layout Recommendations for Receiver Design

2.1 Primary Concerns on PCB Layout

The primary concerns when laying a custom receiver PCB are:

- AC1 and AC2 trace resistance and width
- OUT trace resistance
- GND connection, thermal dissipation
- COMM1 and 2, CLAMP1 and 2, BOOT1 and 2 caps connections
- Isolation of sensitive traces from noisy traces
- Copper weight (> 2 oz)
- Number of layers (higher is better)

2.2 Step-by-Step PCB Layout Guidelines:

- **First step:** The first step in the layout design of the bq51x2x receiver is to put power traces first:
  - AC and OUT width design should be enough to create low trace resistor
  - The length between the IC pin the OUT connector should be as short as possible
  - The traces from the input/output connector to the input/output of the bq51x2x pin should be as wide and short as possible to minimize the impedance in the line (see Figure 1)
  - PGND should be designed to help thermal dissipation
  - The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components, see Figure 1)
  - The dissipation of heat path is important. Adding internal ground layers increases the thermal performance as shown in Figure 1. The layers can be connected to each other with multiple vias to help heat dissipation.
  - For high-current applications, the balls for the power paths should be connected to as much copper in the board as possible. This allows better thermal performance because the board conducts heat away from the IC (see Figure 1).

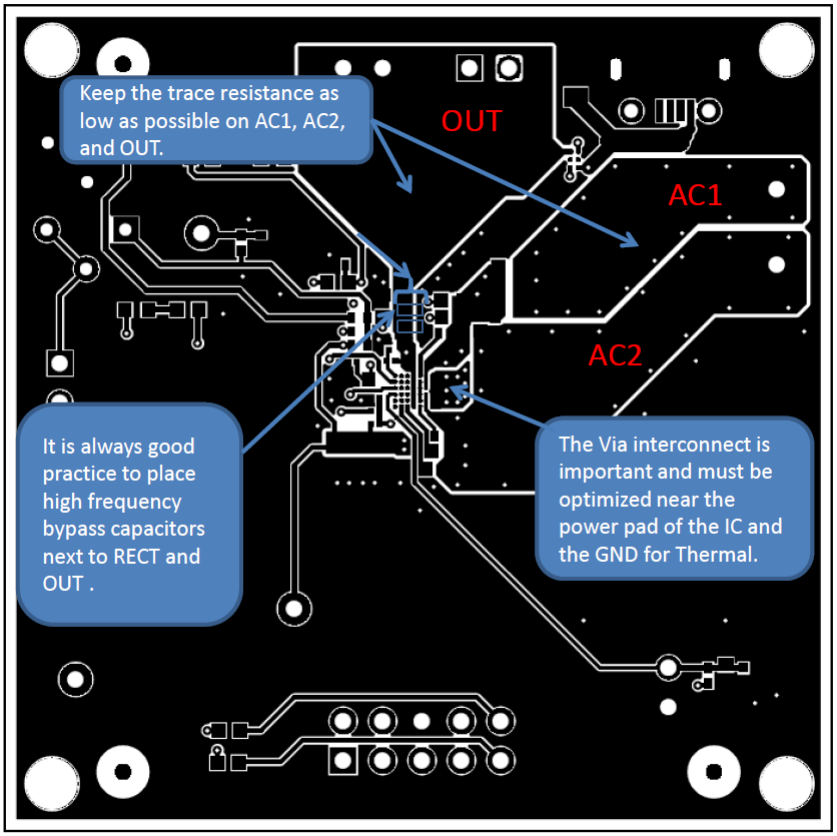

Figure 1. bq51x2x Power Traces

- **Second Step:** The second step is connecting sensitive trace:
  - Connect the output caps as close as possible to the IC pin (see Figure 2)
  - Connect the Rect caps as close as possible to the IC pins
  - It is a good practice to use small signal (0.1 µF) caps on Rect and OUT traces
  - The Via interconnect is important and must be optimized near the power pad of the IC and the GND
  - All sensitive components such as C_COMM1 and 2, C_BOOT1 and 2, C_CLAMP1 and 2, R_ILIM, R_Term, R_FOD, ROS, VOREG, and VIREG divider should be connected as close as possible to the IC and far from the noisy and power traces. For reference, see Figure 2.

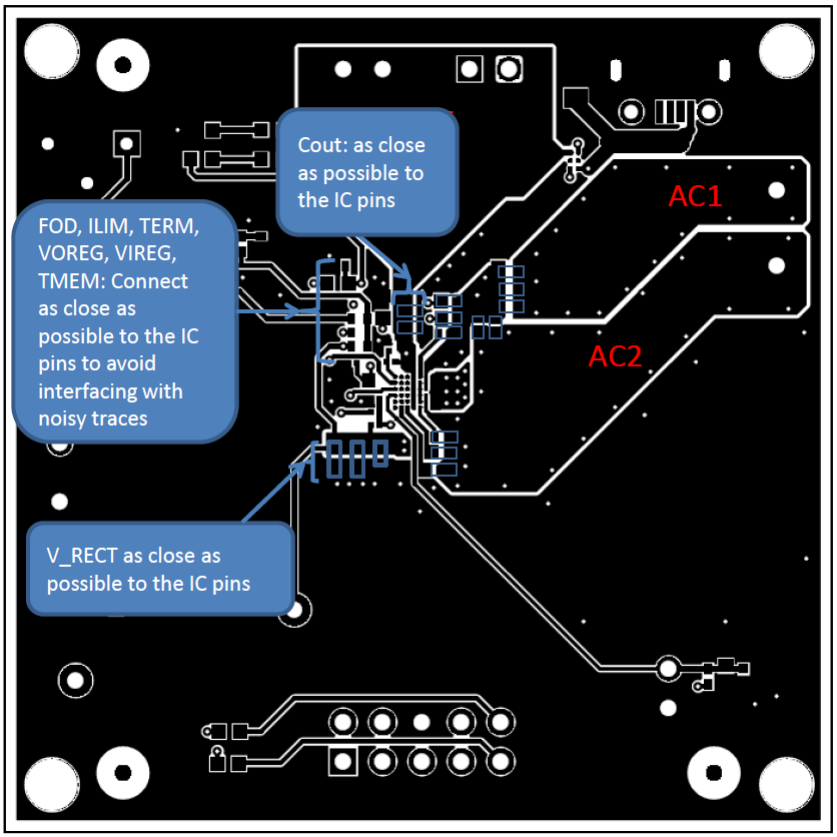

Figure 2. bq51x2x Sensitive Traces

- **Third Step:**
  - BOOT, COMM, and CLAMP caps are noisy and should be isolated from other traces
  - The best practice is to connect them as close as possible to the IC pin to avoid having long traces that may increase the possibility of spreading the noise all over the board
  - Putting a ground trace between noisy trace and sensitive trace is one way to isolate them from each other. The ground should help absorb the noise.
  - Separation between Analog ground and power ground is a good practice. Analog ground is connecting all the sensing and signal trace. Power ground is used for power traces.
  - Copper weight is important for thermal performance of the board. TI recommends using copper weight more than 2 oz.
  - The number of layers also helps in power dissipation and provides more flexibility to place the part and put a good layout

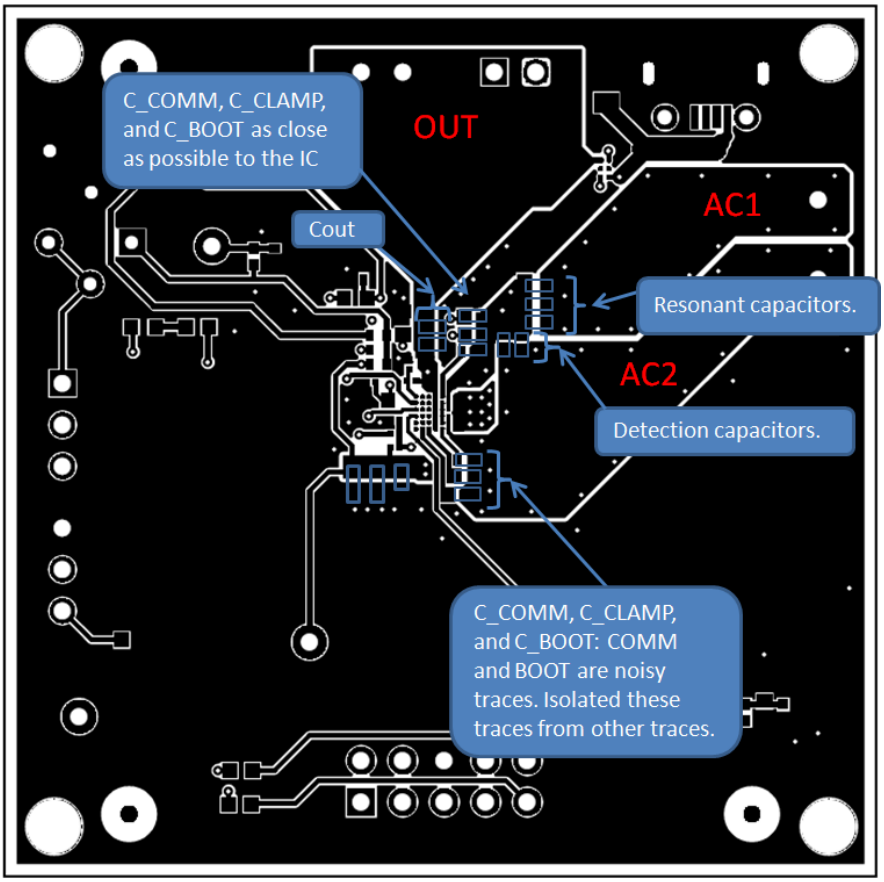

Figure 3. bq51x2x Noisy Traces

2.3 Current Rating Example

For a 1-A fast charge current application, the current rating for each net is as follows:

- AC1 = AC2 = 1.2 A
- BOOT1 = BOOT2 = 10 mA
- RECT = 100 mA
- OUT = return GND=1.2 A
- COMM1 = COMM2 = 300 mA
- CLAMP1 = CLAMP2 = TMEM = 500 mA
- ILIM = VTSB = VIREG = VOREG = 10 mA
- AD = AD_EN = TS-CTRL = EN1 = EN2 = SDA = SCL = TERM = FOD = CM_ILIM = 1 mA
- WPG = PD_DET=20 mA

2.4 EVM Layout Example

Figure 4 through Figure 8 illustrate an example EVM layout.

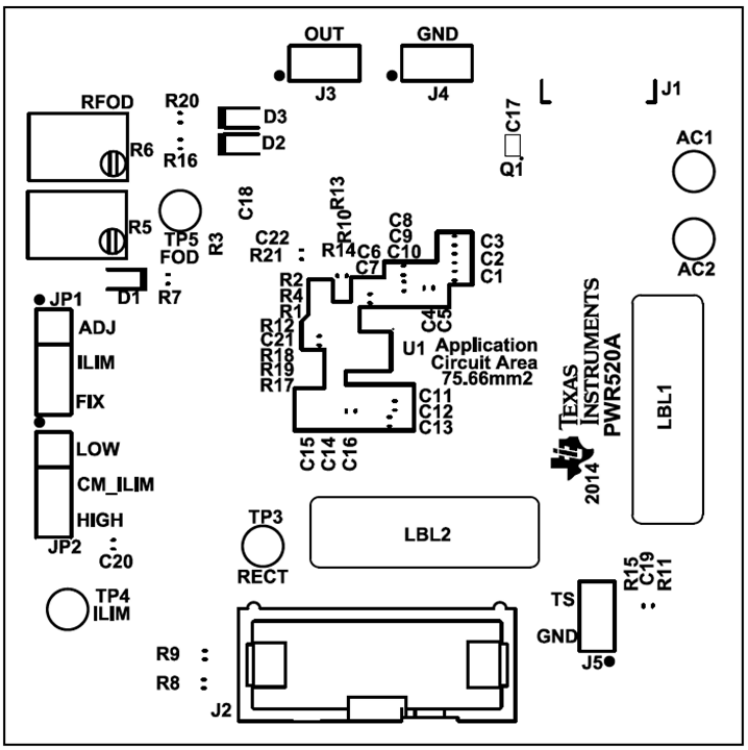

Figure 4. bq51221EVM-520 Top Assembly

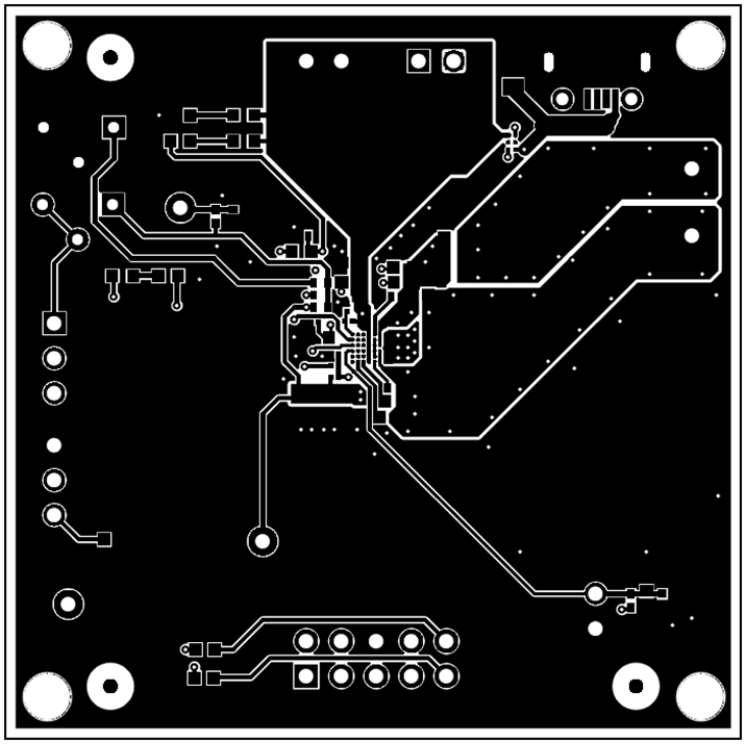

Figure 5. bq51221EVM-520 Layer 1

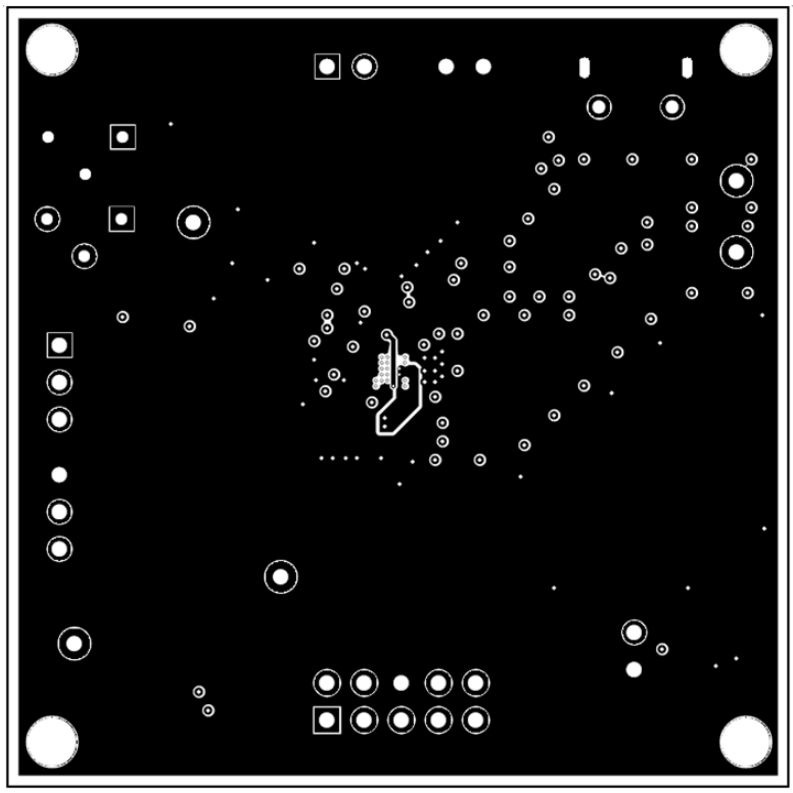

Figure 6. bq51221EVM-520 Layer 2

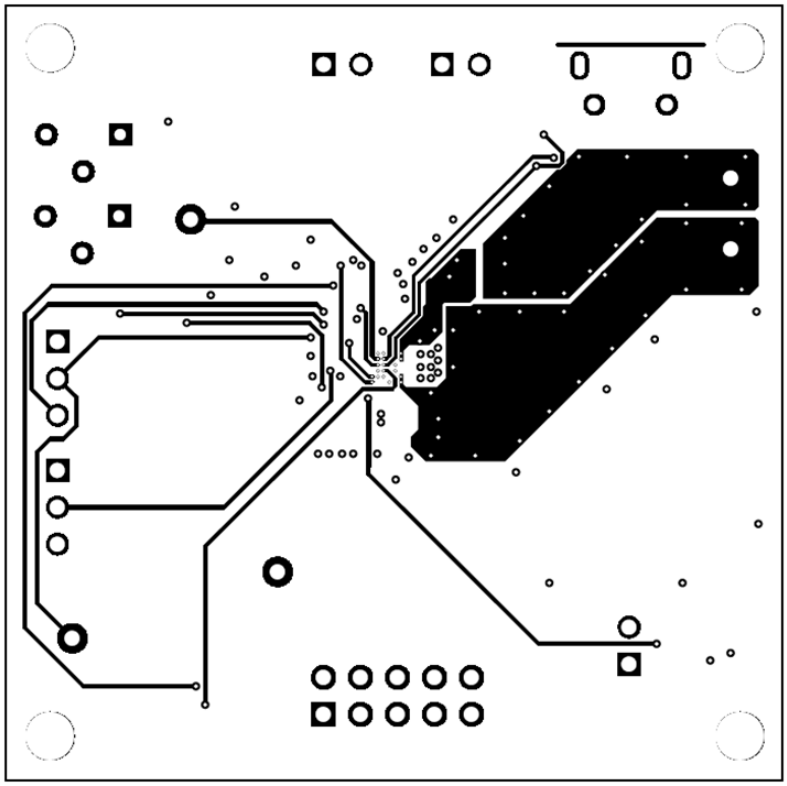

Figure 7. bq51221EVM-520 Layer 3

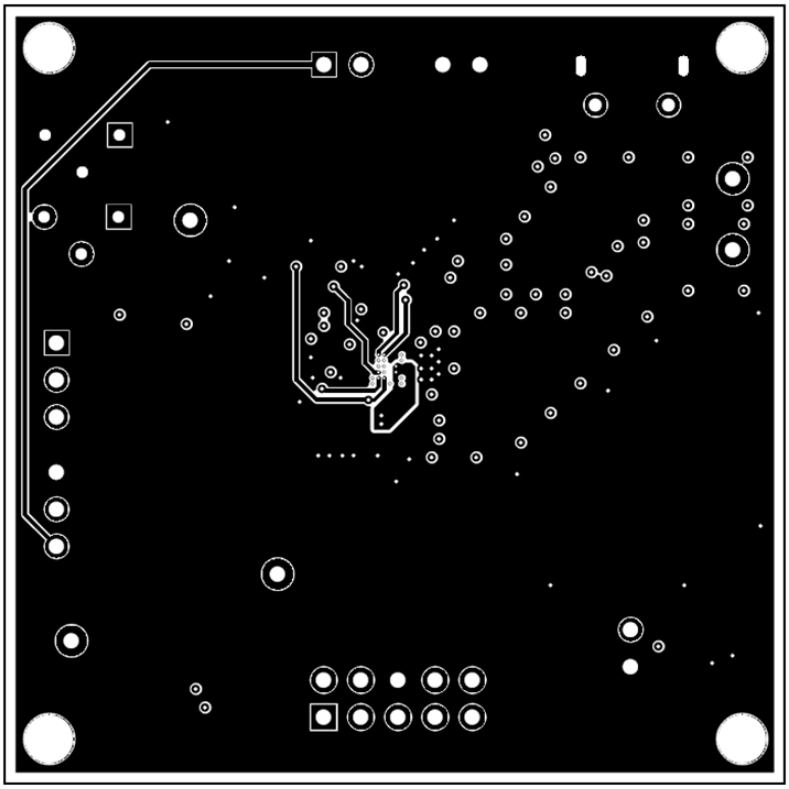

Figure 8. bq51221EVM-520 Layer 4

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