bq76PL455A-Q1 Design Recommendations

ABSTRACT

The bq76PL455A-Q1 is a 16-cell battery monitoring and protector device, for automotive and industrial applications. This document provides design considerations and a checklist for using the bq76PL455A-Q1 in a battery system. For best performance, use the design recommendations in this application report. This document provides some of the specific recommendations which must be implemented for a successful battery system using the bq76PL455A-Q1.

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1 NPN LDO Supply

The bq76PL455A-Q1 is powered from the same cells it monitors. The bq76PL455A-Q1 generates the additional VP and VDIG supplies used in operation from this input.

VP1 is the input for the external LDO supply for the bq76PL455A-Q1. Figure 1 shows the typical circuit.

Select the NPN Transistor based on the following criteria:
1. **Collector-Emitter Breakdown Voltage** ($BV_{CEO}$) > 100 V (or the module voltage, plus any derating)
2. DC gain ($\beta$, or approximately equal to $h_{fe}$ (AC gain)) > 100 at the expected load current
3. Collector-based capacitance < 35 pF at typical base-voltage range
4. Power handling > 500 mW (this assumes a 1-kΩ resistance in series with the collector)
5. Current handling > 100 mA

The series resistors R163 and R164 in Figure 1 serve several purposes:
1. Limit the current in the event of a fault
2. Shift some constant power dissipation in the regulator away from the transistor onto the resistor
3. Combine with the input capacitor on the transistor collector to serve as a filter

To calculate the required resistance, use:
\[
R_{\text{MAX}} = \frac{(V_{\text{MODULE(min)}}) - (V_{\text{P MAX}} + V_{\text{CE(SAT)}}))}{31\, \text{mA} + I_{\text{LOAD}}}
\]

where
- \(V_{\text{CE(SAT)}} = V_{\text{CE}} \text{ min at } V_{\text{BE(on)}}\) from transistor datasheet
- 31 mA is the bq79PL455A maximum inrush current at startup
- \(I_{\text{LOAD}}\) is the expected current for any non-bq76PL455A external loads applied to the VP pin

1. The R78 and R80 series resistors in the VDIG and VIO supplies, respectively, isolate large load capacitance from the voltage regulator to help with loop stability.
2. Connect a filter on the VP supply (R23 and C36) for stability. Use \(R23 = 390 \, \Omega\) and \(C36 = 4.7 \, \mu\text{F}\).

**Design Considerations**

1. Select R163 and R164 from the \(R_{\text{MAX}}\) formula. \(R_{\text{MAX}}\) is calculated based on the minimum module voltage but should consider the thermal heat of resistors with the maximum module voltages. The resistor can be in series and parallel to spread out the heat, if board space permits.
2. A capacitance of 1 \(\mu\text{F}\) is recommend for C40 but it can be up to 2.2 \(\mu\text{F}\), if \(R_{\text{MAX}}\) is reduced to 200 \(\Omega\). It is a good practice to have 2 capacitors in series, in case one capacitor gets shorted. There could be hundreds of mA depending on the number of cell counts if C40 is damaged and shorted to GND.
3. The Q17 transistor must meet bq76PL455A-Q1 requirements
4. The VP filter is critical, TI recommends using \(R23 = 390 \, \Omega\) and \(C36 = 4.7 \, \mu\text{F}\)
5. A 1-\(\Omega\) resistance of R78 and R80 series resistors in the VDIG and VIO (respectively) supplies is a must have for isolating large load capacitance from the voltage regulator to help with loop stability

2 **TOP and VSENSE16**

To ensure that the voltage between Top and VSENSE16 do not violate the absolute maximum rating and operating condition during hot-plug, connect the VSENSE16 input or highest sense input to the TOP pin.

**Design Considerations**

1. Top input must include a low-pass filter with 100 \(\Omega\) and 0.1 \(\mu\text{F}\). R1 should be in the range of 100 \(\Omega\) to a maximum of 300 \(\Omega\) to avoid voltage stress during hot-plug.
2. Back-to-back diode D1 and D2 should be able to withstand the continual current in the event of an open wire on VSENSE16 and also to withstand inrush currents during the hot plug. Use a diode that has a higher Vf, not a Schottky diode which has low Vf. The 1N4148W is used on the reference design.
3. Connect a TVS diode, Z1, to TOP to clamp the voltage below 88 V and prevent an overvoltage condition on TOP during hot-plug and other transient event
4. Connect VSENSE pins to VSENSE16 as Figure 3 shows
3 VREF and V5VAO

VREF output filter pin. Decouple with parallel 0.1-µF and 1.8-µF (25 V+) capacitors to the ground plane. Locate decoupling capacitors as close to the pin as possible. To maintain measurement fidelity, do not place external loads on this pin.

V5VAO is connected to an internal 5-V always-on supply. Decouple with a 4.7-µF capacitor connected to the ground plane. Place the decoupling capacitor as close to pin as possible. Do not use this pin to supply external circuitry.

Design Considerations
1. Both VREF and V5VAO are used for very sensitive internal circuits and should not be used to supply external circuits.
2. Decouple a 4.7-µF capacitor on the V5VAO pin to the ground plane. Put the capacitor as close to pin as possible.
3. A good temperature coefficient for VREF is needed.
   1. All capacitors are X7R or better
2. Must be up to, but not exceed 2 µF
3. The best option is 1.8 µF + 0.1 µF, but 1.8-µF capacitors are only available from a few vendors

![Figure 4. Connecting VREF and V5VAO](image)

4. CHM, CHP, and VM

VM is an internal –5-V charge pump output. It requires an external flying capacitor connected between the CHP and CHM pins plus a storage capacitor on the VM pin to generate a rail of –5 V for internal use. The charge pump (VM) is always on in IDLE and off in SHUTDOWN. VM requires the oscillator to be running and stable and does not start until the other supplies are above their POR thresholds. The VM charge pump will start ramping at the start of the WAKEUP tone on COMH.

**Design Considerations**
1. Connect a 22-nF flying capacitor between CHP and CHM
2. Decouple with 4.7-µF and 0.1-µF capacitors to VM pin and locate them as close to VM pin as possible.

![Figure 5. Connecting VM, CHP and CHM](image)

5. AGND and VSENSE0

To ensure that the voltage between VSENSE0 and AGND1 does not violate the absolute maximum and recommended operating conditions during hot-plug or other unusual conditions, connect the VSENSE0 input to the AGND1 pin using two back-to-back signal diodes. Select diodes with a high enough current rating to withstand the continuous currents during a wire disconnect and the inrush currents during hot plug. Use diodes that have a higher Vf, such as an ultra-fast or fast diode. Low Vf diodes, such as Schottkey diodes, must not be used because noise on AGND may couple onto the VSENSE0 input. Additionally, connect a 1-µF capacitor between VSENSE0 and AGND1. **Figure 6** illustrates the correct VSENSE0-to-AGND1 connection.

**Design Considerations**
1. Connect back-to-back diodes between AGND to VSENSE0. The 1N4148W is used on the reference design.

2. Connect a 1-µF capacitor between VSENSE0 and AGND.

Figure 6. Connecting AGND and VSENSE0

6 **VSENSE to VSENSE Connections**

To ensure that the voltage between the VSENSE_ inputs (VSENSE0 to VSENSE1, VSENSE1 to VSENSE2, and so forth) does not violate the absolute maximum rating and recommended operating condition during hot-plug or other unusual conditions, Zener diodes must be connected between the VSENSE input pins, as close as possible to the inputs. One Zener diode across every input is advised. The Zener diodes provide overvoltage protection and a path for inrush current during a hotplug event. **Figure 7** illustrates the correct VSENSE-to-VSENSE connection.
Figure 7. bq76PL455A-Q1 Front-End Circuit
Selecting Zener diode for VSENSE(Z15, Z16):

1. The bq76PL455 inputs are protected from input voltage transients greater than 5.5 V. Any transients greater than 5.5 V must be clamped to less than 6.5 V for an accumulative time duration not to exceed 0.1% of the device 10-year lifetime.

2. The Zener diode maximum reverse current ($i_z$) at normal battery-cell voltage levels are as low as possible to keep the quiescent system-current draw low. Additionally, any leakage through the Zener diode affects the total channel accuracy measurements as it adds to the voltage drop across the filter resistor.

3. The Zener must be capable of withstanding instantaneous or continuous currents that the bq76PL455A-Q1 experiences during fault events. These events can include cable connect or disconnect, inrush, or reverse battery voltage. Depending on the fault and the direction of current flow, the maximum power dissipation for the Zener diode must not be exceeded, to stay within maximum operating conditions.

A series resistor and bypass capacitor are required for each of the VSENSE inputs. The series resistor (R69 and R76 in Figure 7) serves four functions:

1. They protect the AFE inputs from in-rush currents during hot plug-in. This requirement limits the input series $R$ to a minimum of 100 $\Omega$. Keep this resistance as low as possible to minimize input voltage offset, which is also subject to drift over temperature. These requirements limit the maximum value to 1 k$\Omega$. Error due to input bias currents on the front end of the AFE, is directly proportional to the value of the resistors. The voltage measurement error can be calculated as:

$$\text{voltage measurement error} = 2 \times R \times I_{\text{SENSE}}$$  \hspace{1cm} (1)

2. The resistor and capacitor (R69 and C16 in Figure 7) provide an RC filter for high-frequency noise on the AFE inputs. The tuning of this filter cutoff is adjustable and depends on the expected frequency of noise in the system. Calculate the cutoff frequency using the following equation:

$$f_c = \frac{1}{2\pi R C_1} \text{Hz}$$  \hspace{1cm} (2)

3. Ensure that the RC-filter components are as close to the device as possible. The capacitor location is extremely important and must be given priority for optimum performance.

4. For applications that require a very low filter cutoff frequency, connect a differential capacitor between the VSENSE lines to provide the bulk of the AFE input filtering. The bias voltage on these differential capacitors are the same (or very close), therefore, anti-aliasing is improved.

**Design Checklist:**

1. Select a Zener diode with the lowest reverse current and that meets the criteria described in this section.

2. R69 and R76 should not exceed 1 k$\Omega$ and the filter should be as close to the device as possible.

### 7 Balancing Circuit

#### Balancing FET

Select the Balance FET (Q15 and Q16) based on the following criteria:

1. The $V_{DS}$ must be selected based on derating requirements determined by the stack voltage.

2. $V_{GS}$ must be as large as possible and preferably have ESD protection from gate to source. This protects the part during hot plug.

3. The $V_{GS}$ threshold is of concern only if the discharge resistors are going to be turned on at low-battery voltages.

The 2V7002K is recommended because of its 60 $V_{DS}$, ±20 $V_{GS}$, and the gate is ESD-protected with an internal Zener diode.

The $R_{DS}$ value is of little consideration with the discharge currents for this application.

The $V_{GS}$ resistors (R70 and R22) ensure that the gate of the FET is turned off and does not float into a linear or on state causing excessive leakage currents on that cell in case of FET failure or PCB open.
A series resistor between the EQ pin and the FET gate limits current going into the FET during hot plug or other transient events.

**Balancing Resistor**

The balancing resistors (R15 and R16) set the required balance current. If used, the resistors in series with the cell connections (top and bottom, in front of the Zener diode) must be included in this calculation. These resistors must be sized appropriately to handle the thermal dissipation of continuous cell balancing.

**Balancing Zener**

The balancing Zener diode is not required if the 60 \( V_{DS} \), ±20 \( V_{GS} \) requirement is satisfied. If the balancing FET does not meet the requirement, then a Zener diode is necessary to protect the device during hot plug.

**Design Checklist:**

1. Select proper FETs for Q15 and Q16.
2. Consider thermal for R16 and R15. They set the balancing current.
3. R70 and R22 are needed to make sure the FET does not float when it is turned OFF.
4. R89 and R88 limit current in hot-plug.

**8 OUT1,2**

OUT pins are the connection between the analog front end (located on the analog die) and the ADC (located on the digital die). A 390-pF capacitor type C0G or NP0 between OUT pins to GND is strongly recommended with ADC settings for best ADC measurements.

![Figure 8. Connecting OUT1 and OUT2](image)

**9 AUX Input Channels**

Typically, 8 AUX ADC inputs are used to monitor externally-supplied temperature sensors and other sensors with an input voltage range of 0 V to 5 V.

For best performance, the AUX inputs require a series of resistor and bypass capacitors for filtering. Recommendation is to connect a 1-kΩ and 1-µF filter as Figure 9 illustrates.

A differential AUX measurement is recommend for extremely noisy environments as shown in Figure 9.

Unused AUX inputs can be allowed to:

1. Float
2. Tie to local GND
3. Pull up to VP/VDIG with a 100-kΩ pullup
There are six GPIO pins available in the bq76PL455A-Q1. Register GPIO_xxx is located at addresses 0x78-7D and controls GPIO behaviors. Each register can be programmed to be an input or output pin. When DEVCONFIG[ADDR_SEL]==0, the device uses the address sampled from GPIO[4:0] to set ADDR. The address is sampled as part of the reset process or by setting DEV_CTRL[AUTO_ADDRESS].

GPIO pins are all programmed as inputs, no pullup or pulldown resistors are enabled, leaving the inputs floating. The pins should not be allowed to remain as floating inputs. The pins should be reprogrammed to become outputs or add a pullup or pulldown if none are provided externally.

Design Checklist:
• GPIO pins are all programmed as inputs, no pullup or pulldown resistors are enabled, leaving the inputs floating. The pins should not be allowed to remain as floating inputs. Reprogram the pins to become outputs or add a pullup or pulldown as shown in Figure 10, if none are provided externally.
11 WAKEUP

The WAKEUP pin must be held in the low state to allow the device to enter and remain in the SHUTDOWN state. If the WAKEUP pin remains in the high state, the device will cycle off and immediately back on. Operation is unpredictable if the WAKEUP pin floats, ensure the WAKEUP pin is kept in a defined state. Setting the WAKEUP pin low does not put the device in the SHUTDOWN mode.

![Diagram of WAKEUP connection](image)

**Figure 11. Connecting WAKEUP**

**Design Considerations**

1. Connect WAKEUP to local GND for all Slave ICs
2. Add 0.1µF capacitor if WAKEUP signal is on cable. Capacitor is to filter out possible transient introduced by the cable.
3. R1 can be as low as 50 Ω, if the WAKEUP signal is less than 4 V
4. R1 can be high as 50 kΩ, if the WAKEUP is higher than 4-V signal. Wakeup is internally connected to V5VAO and it can be as low as 4V in shutdown mode.

12 Single-Ended Communication

Communication with the bq76PL455A-Q1 from a host controller is performed utilizing UART communication protocol. The UART interface requires the following configuration:

1. COMML– is connected by a 100-kΩ pulldown to DGND
2. COMML+ is connected by a 100-kΩ pullup to V5VAO
3. FAULT_N has a 50-kΩ pulldown to make sure faults are generated when VIO is not present. The pulldown on the FAULT_N notifies the host controller in the case of an inadvertent shutdown.
4. TX and RX are pulled-up to VIO through a 100-kΩ resistor. Do not leave TX and RX unconnected. The TX must be pulled high to prevent triggering an invalid communications frame during the idle state when TX is high. When using a serial cable to connect to the host controller, connect the TX pullup on the host side and the RX pullup on the bq76PL455A-Q1 side.
Figure 12. Single-Ended Circuit
Table 1. Single-Ended Communication Check List

<table>
<thead>
<tr>
<th>List</th>
<th>Pin</th>
<th>Single-Ended (Figure 12)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RX</td>
<td>100-kΩ pullup to VIO</td>
</tr>
<tr>
<td>2</td>
<td>TX</td>
<td>100-kΩ pullup to VIO</td>
</tr>
<tr>
<td>3</td>
<td>COMML+</td>
<td>100-kΩ pullup to V5VAO</td>
</tr>
<tr>
<td>4</td>
<td>COMML−</td>
<td>100-kΩ pulldown to GND</td>
</tr>
<tr>
<td>5</td>
<td>COMMH+</td>
<td>Float</td>
</tr>
<tr>
<td>6</td>
<td>COMMH−</td>
<td>Float</td>
</tr>
<tr>
<td>7</td>
<td>FAULTH+</td>
<td>Float</td>
</tr>
<tr>
<td>8</td>
<td>FAULTH−</td>
<td>Float</td>
</tr>
<tr>
<td>9</td>
<td>FAULTL+</td>
<td>Float</td>
</tr>
<tr>
<td>10</td>
<td>FAULTL−</td>
<td>Float</td>
</tr>
<tr>
<td>11</td>
<td>FAULT_N</td>
<td>50 kΩ, pull down to GND and 50Ω series to host</td>
</tr>
<tr>
<td>12</td>
<td>WAKEUP</td>
<td>R1 should be 50 kΩ, if the WAKEUP signal is greater than 4 V (see Figure 11)</td>
</tr>
</tbody>
</table>

13 Stack Daisy-Chain Communication

In the stacked configuration, the main microcontroller first communicates through a bq76PL455A-Q1 device using the UART communications interface, see Figure 13. Communication is then relayed up the chain of connected slave bq76PL455A-Q1 devices using a proprietary differential communications protocol over AC-coupled differential links interconnected by the COMMH± and COMML± pins.

Each device in the daisy chain buffers the signal drive levels. The signal is not re-clocked or filtered; it passes through the device without change and the entire stack sees all data sequencing regardless of the target device. The packet is not validated before being transmitted to the next device in the daisy chain. The uniquely-addressed or group-addressed device acts on the command (that is, begins an ADC conversion of the inputs) as soon as it receives and validates the packet for the correct address, message contents, and CRC.
Figure 13. Simplified Stack Communication
Figure 14. Stack Main (Master) Device
Figure 15. Stack Slave (Middle) Device
Figure 16. Stack Slave (TOP) Device

Many applications require multiple, daisy-chained bq76PL455A-Q1 devices that are separated by cables or located on the same PCB. The cables can introduce additional challenges and additional components are needed for noisy environments. See Figure 17 for different ways of designing differential communication VBUS daisy chains.
Design Checklist:
1. Follow Table 2 for all communication pins.
2. TVS diodes are required for communicating between PCB. Use a TVS diode with the lowest capacitance as shown in Figure 17.

Table 2. Stack and Single-Ended Communication Check List

<table>
<thead>
<tr>
<th>List</th>
<th>Pin</th>
<th>Stack Main (Master) Device (Figure 14)</th>
<th>Stack Slave (Middle) Device (Figure 15)</th>
<th>Stack Slave (TOP) Device (Figure 16)</th>
<th>Single-Ended (Figure 12)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RX</td>
<td>100-kΩ pullup to VIO</td>
<td>100-kΩ pullup to VIO</td>
<td>100-kΩ pullup to VIO</td>
<td>100-kΩ pullup to VIO</td>
</tr>
<tr>
<td>2</td>
<td>TX</td>
<td>100-kΩ pullup to VIO</td>
<td>Float</td>
<td>Float</td>
<td>Float</td>
</tr>
<tr>
<td>3</td>
<td>COMML+</td>
<td>100-kΩ pullup to V5VAO</td>
<td>COMMH+ of lower (main) device</td>
<td>COMMH+ of lower (middle) device</td>
<td>100-kΩ pullup to V5VAO</td>
</tr>
<tr>
<td>4</td>
<td>COMML–</td>
<td>100-kΩ pulldown to GND</td>
<td>COMMH– of lower (main) device</td>
<td>COMMH– of lower (middle) device</td>
<td>100-kΩ pulldown to GND</td>
</tr>
<tr>
<td>5</td>
<td>COMMH+</td>
<td>COMML+ of upper (middle) device</td>
<td>COMML+ of upper (TOP) device</td>
<td>Float</td>
<td>Float</td>
</tr>
<tr>
<td>6</td>
<td>COMML–</td>
<td>COMML– of upper (middle) device</td>
<td>COMML– of upper (TOP) device</td>
<td>Float</td>
<td>Float</td>
</tr>
<tr>
<td>7</td>
<td>FAULTH+</td>
<td>FAULTL+ of upper (middle) device</td>
<td>FAULTL+ of upper (TOP) device</td>
<td>Float</td>
<td>Float</td>
</tr>
<tr>
<td>8</td>
<td>FAULTH–</td>
<td>FAULTL– of upper (middle) device</td>
<td>FAULTL– of upper (TOP) device</td>
<td>Float</td>
<td>Float</td>
</tr>
</tbody>
</table>
Table 2. Stack and Single-Ended Communication Check List (continued)

<table>
<thead>
<tr>
<th>List</th>
<th>Pin</th>
<th>Stack Main (Master) Device (Figure 14)</th>
<th>Stack Slave (Middle) Device (Figure 15)</th>
<th>Stack Slave (TOP) Device (Figure 16)</th>
<th>Single-Ended (Figure 12)</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>FAULTL+</td>
<td>Float</td>
<td>FAULTH+ of lower (main) device</td>
<td>FAULTH + of lower (middle) device</td>
<td>Float</td>
</tr>
<tr>
<td>10</td>
<td>FAULTL-</td>
<td>Float</td>
<td>FAULTH- of lower (main) device</td>
<td>FAULTH– of lower (middle) device</td>
<td>Float</td>
</tr>
<tr>
<td>11</td>
<td>FAULT_N</td>
<td>100 kΩ pulldown to GND</td>
<td>Float</td>
<td>Float</td>
<td>100 kΩ pulldown to GND</td>
</tr>
<tr>
<td>12</td>
<td>WAKEUP</td>
<td>See Figure 11.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

14 Common and Differential Mode Noises

X-Y caps are commonly used and may be required for extremely noisy environments
- Differential mode noise goes out one wire and returns back on another wire. An X capacitor is placed between two lines to suppress the noise.
- Common mode noise goes out from both wires and returns back to the chassis through stray capacitance to ground. A Y capacitor is placed between the chassis as Figure 18 illustrates.

Battery Pack

Design Considerations
- Device placements are important. Daisy-chain cable should not be resting on bus-bar or mental enclosure surface.

Figure 18. XY Caps
15 EMC Susceptibility on Cell Inputs

Additional components are necessary to improve EMC performance of the bq76PL455A-Q1 in automotive applications with electrically noisy environments.

- Use ferrite beads or small inductors in series with the cell inputs between the cell output and the series resistor to the VSENSE input. The bead and small capacitor must be located near each other.
- Add a 0.0033-µF capacitor from each cell input to the battery pack (BAT0 in Figure 19). Adjust the value of capacitance to satisfy the PCB layout and field conditions for the application.

BAT0S is the sense point to the negative terminal of CELL1. BAT0 is the power plane for the negative terminal of the cell stack.

Figure 19. EMC Filter
16 Layout Consideration

Since the bq76PL455A-Q1 measures small changes in voltage, care must be taken in the layout of signals to and from the device to avoid coupling noise onto sensitive inputs. The layout of ground and power connections, as well as communication signals should also be made carefully.

16.1 Layout Examples

To ensure the best possible accuracy performance, TI recommends following some basic layout guidelines for the bq76PL455A-Q1 to provide the best EMI and BCI performance. The isolation caps must be placed close to the edge of the board. The Common Mode Chokes must be close to the daisy-chain cable connector to provide a high-impedance path to common-mode noise as it enters the board. Place the series resistors and TVS diodes next to the bq76PL455A-Q1.

For detailed layout guidelines, see the bq76PL455A-Q1 datasheet (SLUSCB8).

An unbroken ground plane layer as part of a four or more layer board is recommended, with all AGND, DGND, and CGND connections made directly to the plane. The common GND planes are star connected directly to BAT0. There should also be a keep-out area on the plane area adjacent to the isolation capacitors, if daisy-chain communication is implemented. The following is a list of grounds:

- AGND1 – power section (noisy GND)
- AGND2 – GND for front-end output
- AGND3 – GND for ADC input
- DGND1, DGND2, DGND3 – digital GND
- CGND – communications digital GND

![Figure 20. Simplified Layout Guideline](image_url)
17 FAQ

17.1 Hot-Plug

The bq76PL455A-Q1 is designed for robust hot-plug performance. Component placement is critical for robust hot plugs.

1. Add a Zener diode between all VSENSE pins, as close as possible to input pins (see Figure 2).
2. Connect VSENSE16 input and any unused VSENSE pins to TOP using back-to-back diodes (see Figure 2).
3. Add a TVS diode on VSENSE16 to local ground to clamp the voltage to below 88 V and prevent an overvoltage and other transient events (see Figure 2).
4. Connect two back-to-back diodes between VSENSE0 and AGND as Figure 6 shows.
5. LPF should be 100 Ω to 1 kΩ and 0.1 µF to 1 µF. Higher resistance is better at limiting inrush current but the resistor value is directly proportional to error due to input bias (see Figure 7).
6. The total resistance of each COMML±, COMMH±, or FAULT_N± lines must be less than 20 Ω (10 Ω on each end of the signal connection between bq76PL455A-Q1 devices). This series resistance is required to limit in-rush current in a hot-plug event.
7. TI recommends connecting cell inputs first and then connecting daisy-chain cables.
8. TI recommends connecting VSENSE 16 to VSENSE 0, if possible.

17.2 Recommended Sample Periods and Setup for Best ADC Measurements

1. Apply 390 pF on OUT12 filter cap (see Figure 8)
2. Set AFE_PCTRL = 1. ADC power up will be 100 µs.
3. Set ADC_PERIOD_VOL = 60 µs. ADC sample period to 60 µs.
4. Set CMD_OVS_GPER = 12.6 µs. ADC sample period for oversamples.
5. Select CMD_OVS_CYCLE. Staying on a cell channel to oversample.
6. Set ADC_PERIOD_AUX = 12.6 µs. AUX ADC sample period
7. Set CMD_OVSMP for 8× oversampling for cells and Aux.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2016) to A Revision

- Changed the description of FAULT_N From: “Float” To: “50 kΩ, pull down to GND and 50Ω series to host” in Table 1 . 13
- Changed the Stack Main description of COMML+ From: “Float” To: “100-kΩ pullup to V5VAO” in Table 2 ................. 18
- Changed the Stack Main description of COMML– From: “Float” To: “100-kΩ pulldown to GND” in Table 2 ................. 18
STANDARD TERMS FOR EVALUATION MODULES

1. Delivery: TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User’s acceptance of the EVM is expressly subject to the following terms.

1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software.

1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 Limited Warranty and Related Remedies/Disclaimers:

2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects within ten (10) business days after the defect has been detected.

2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.
FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lds/ti_ja/general/eStore/notice_01.page

3.3.2 Notice for Users of EVMs Considered “Radio Frequency Products” in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan.
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.
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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿6丁目24番1号
西新宿三井ビル

3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lnds/ti_ja/general/eStore/notice_02.page
電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lnds/ti_ja/general/eStore/notice_02.page

3.4 European Union
3.4.1 For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):
This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 EVM Use Restrictions and Warnings:
4.1 EVMs are not for use in functional safety and/or safety critical evaluations, including but not limited to evaluations of life support applications.
4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
4.3 Safety-Related Warnings and Restrictions:
4.3.1 User shall operate the EVM within TI’s recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User’s handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. Accuracy of Information: To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
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6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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8.2 **Specific Limitations.** IN NO EVENT SHALL TI’S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMNITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. **Return Policy:** Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

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