ABSTRACT
The UCC24630/636 synchronous rectifier controllers are high-performance controllers and drivers for N-channel MOSFET power devices used for secondary-side synchronous rectification. The data sheets of the UCC24630 and UCC24636 devices show them in ground-referenced configurations only, apparently limiting the use cases of the devices. However, these devices can also be configured to be used in non-ground-referenced situations and where the output voltage is higher than the $V_{CC(MAX)}$ limit of the device. This guide will demonstrate implementations for high-side and low-side synchronous rectifiers different from those in the data sheets.

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1 Purpose of the Synchronous Rectifier

The synchronous rectifier (SR) MOSFET replaces the diode as the output rectifier, thereby drastically reducing the conduction losses. The UCC23630/636 use Volt-second balancing rather than \( V_{DS} \)-sensing to control the SR MOSFET in CCM and DCM Flyback converters, respectively. This control method allows the use of MOSFETs with very low \( R_{DS(on)} \) which minimizes conduction loses.

2 When to Use Which Controller

Use the UCC24630 for Continuous Conduction Mode (CCM) Flyback SR applications that operate at a fixed or slowly-varying frequency. The UCC24630 can also work in Discontinuous Conduction Mode (DCM), but the CCM-specific features may prove to be an unnecessary burden on DCM-only operation. The UCC24636 is an SR device for DCM and Quasi-Resonant (QR) Flyback converters, and is not suitable for use in CCM applications.

While the CCM-specific features have been removed, the UCC24636 accommodates for the need of widely-varying switching frequency. Both devices can be used in either high-side or low-side applications.

Typically low-side SR is simplest and easiest to design, whereas high-side SR requires some design adjustments and extra circuitry. Despite the complexity, high-side SR is often preferred due to its better EMI performance.

NOTE: This configuration guide should not be used in place of the data sheet, but in conjunction with it for SR design.

3 Comparison Table

<table>
<thead>
<tr>
<th>CONFIGURATION</th>
<th>PROS</th>
<th>CONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-Side SR</td>
<td>• GND-referenced MOSFET drive and direct power from ( V_{OUT} ), for ( V_{OUT} &lt; V_{CMAX} )</td>
<td>• Capacitance of drain node may increase possibility of higher EMI</td>
</tr>
<tr>
<td></td>
<td>• Fewest amount of parts</td>
<td>• &quot;Quiet&quot; side of transformer winding is ( V_{OUT} ) with (small) ripple voltage</td>
</tr>
<tr>
<td></td>
<td>• No need for bias winding on transformer</td>
<td>• Needs bias winding on transformer</td>
</tr>
<tr>
<td></td>
<td><strong>High-Side with Bias Winding</strong></td>
<td>• VSC is indirect reflection of ( V_{OUT} ), changes slowed by ( C_{VDD} )</td>
</tr>
<tr>
<td></td>
<td>• Allows heatsinking of MOSFET drain to &quot;quiet&quot; ( V_{OUT} ) or GND nodes</td>
<td>• Entire SR control rides on switched voltage at high ( dv/dt )</td>
</tr>
<tr>
<td></td>
<td>• &quot;Quiet&quot; side of transformer winding is GND</td>
<td>• Entire SR control rides on switched voltage at high ( dv/dt )</td>
</tr>
<tr>
<td></td>
<td>• Non-ultrafast diode ( D_b ) helps ( V_{BIAS} ) track ( V_{OUT} ) better</td>
<td>• VSC is fixed to maximum expected ( V_{OUT} ), no changes in ( V_{OUT} ) are detected</td>
</tr>
<tr>
<td></td>
<td><strong>High Side without Bias Winding</strong></td>
<td>• SR on-time is shorter than desired when ( V_{OUT} ) is low</td>
</tr>
<tr>
<td></td>
<td>• Allows heatsinking of MOSFET drain to &quot;quiet&quot; ( V_{OUT} ) or GND nodes</td>
<td>• Entire SR control rides on switched voltage at high ( dv/dt )</td>
</tr>
<tr>
<td></td>
<td>• &quot;Quiet&quot; side of transformer is GND</td>
<td>• May need LDO at ( R_b )</td>
</tr>
<tr>
<td></td>
<td>• No need for bias winding on transformer</td>
<td>• Large amount of parts</td>
</tr>
</tbody>
</table>

Figure 1, Figure 2, and Figure 3 show typical SR implantations using the UCC24630. The same configurations apply when using the UCC24636.
4  **UCC24630/636 Used in Low-side SR**

The simplest low-side implementation for both devices is under the condition that $V_{\text{OUT(max)}} < V_{\text{DD_ABS_MAX}}$.

![Figure 1. Low-Side SR Configuration](image)

Setting $R_{\text{VPC1}}$ and $R_{\text{VSC1}}$ is done so using the following equations:

$$R_{\text{VPC1}} = \left[ \frac{V_{\text{BULK(min)}}}{N_{\text{PS}}} + \frac{V_{\text{OUT(min)}}}{V_{\text{VPCEN(max)} \times 1.1}} \right] - 1 \quad R_{\text{VSC1}} = \left[ \frac{R_{\text{VPC1}}}{R_{\text{VSC2}}} + 1 \right] \frac{\text{Ratio}_{\text{VPC\_VSC}} \times 1.1}{1} - 1$$

where

- $V_{\text{BULK(min)}}$ is the converter minimum bulk capacitor voltage
- $V_{\text{OUT(min)}}$ is the minimum converter output operating voltage
- $N_{\text{PS}}$ is the transformer primary to secondary turns ratio
- $V_{\text{VPCEN(max)}} = 0.45 \text{ V}$; synchronous rectifier enable voltage

The values for $R_{\text{VPC2}}$ and $R_{\text{VSC2}}$ are suggested to be set as $R_{\text{VPC2}}$ to 10 kΩ and $R_{\text{VSC2}}$ to 47 kΩ to balance a trade-off between speed and stand-by power. Other values may be chosen at the designer's discretion.

A more in-depth guide to selecting $R_{\text{VPC2}}$ and $R_{\text{VSC2}}$ resistors can be found in section 8.3.2 in the **UCC24636 datasheet**.
The following configurations sections show the UCC24630/636 used in configurations not shown in the datasheet and how to accommodate component values in design. The terms highlighted in red are modifications to the standard TI low-side SR equations.

In the configuration of Figure 2, the bias winding provides power to the device floating on the secondary switching node. Here, $V_{\text{BIAS}}$ tracks $V_{\text{OUT}}$ through $N_{\text{BS}}$ and can be used as a source for the VSC-divider input.

![Figure 2. High-Side SR Configuration with Bias Winding](image)

Setting $R_{\text{VPC1}}$ and $R_{\text{VSC1}}$ is done so using the following equations:

\[
R_{\text{VPC1}} = \left[ \frac{V_{\text{BULK}}(\text{min}) + V_{\text{OUT}}(\text{min})}{V_{\text{VPCEN}}(\text{max}) \times 1.1} \right] - 1 \quad \text{and} \quad R_{\text{VSC1}} = \left[ \frac{N_{\text{BS}} \left( \frac{R_{\text{VPC1}}}{R_{\text{VPC2}}} + 1 \right)}{k_{\text{VS}}} \frac{\text{Ratio}_{\text{VPC,VSC}}}{1.1} \times 1.1 \right] - 1
\]

(3) \hspace{1cm} (4)

Where

- $N_{\text{BS}} = \frac{N_{\text{B}}}{N_{\text{S}}}$
- $N_{\text{BS}} < \frac{V_{\text{DDA_MAX}}}{V_{\text{OUT}(\text{max})}}$
- $k_{\text{VS}} = \frac{N_{\text{BS}} V_{\text{OUT}(\text{min})}}{N_{\text{BS}} V_{\text{OUT}(\text{min})} - V_{\text{DB}}}$

Be aware that $V_{\text{OUT}(\text{min})}$ and $V_{\text{OUT}(\text{max})}$ are different values used in different places.

The values for $R_{\text{VPC2}}$ and $R_{\text{VSC2}}$ are suggested to be set as $R_{\text{VPC2}}$ to 10 kΩ and $R_{\text{VSC2}}$ to 47 kΩ to balance a trade-off between speed and stand-by power. Other values may be chosen at the designer's discretion.

A more in-depth guide to selecting $R_{\text{VPC2}}$ and $R_{\text{VSC2}}$ resistors can be found in section 8.3.2 in the UCC24636 datasheet.
6 UCC24630/636 Used in High-Side SR without Bias Winding

This configuration does not use a bias winding to power the controller. Here, $V_{BIAS}$ is not able to track $V_{OUT}$, so $D_Z$ must be used as a fixed source for the VSC-divider input. SR on-time is shorter than expected when $V_{OUT}$ is low. A 5.1-V low current Zener diode such as the NXP PLVA6xxA series diodes is a good place to start with to avoid higher current losses as well as variations in operation due to temperature coefficients.

Setting $R_{VPC1}$ and $R_{VSC1}$ is done so using the following equations:

$$R_{VPC1} = \left( \frac{V_{BULK \text{ (min)}}}{N_{PS}} + \frac{V_{OUT \text{ (min)}}}{V_{PCEN \text{ (max)}}} \times 1.1 \right) - 1$$  \hspace{1cm} (8)

$$R_{VSC1} = \left( \frac{R_{VPC1} + 1}{k_{VZ} \times \text{Ratio}_{VPC_{VSC}}} \times 1.1 \right) - 1$$  \hspace{1cm} (9)

where

- $V_{DB}$ is the voltage drop of diode $D_b$
- $V_{BULK_{\text{max}}}$ is the converter maximum primary bulk capacitor voltage

and

$$\frac{V_{BULK_{\text{max}}}}{N_{PS}} + \frac{V_{OUT_{\text{max}}}}{V_{DB} < V_{DD_{ABS_{\text{max}}}}$$

$$k_{VZ} = \frac{V_{DZ}}{V_{OUT_{\text{max}}}}$$

where

- $V_{DZ}$ is the voltage of Zener diode $D_Z$

Choose $V_{DZ}$ to keep losses in $R_z$ and $R_b$ low.

NOTE: An LDO may be required in place of $R_b$ to keep VDD within its allowable range.

The values for $R_{VPC2}$ and $R_{VSC2}$ are suggested to be set to $R_{VPC2}$ to 10 kΩ and $R_{VSC2}$ to 47 kΩ to balance a trade-off between speed and stand-by power. Other values may be chosen at the designer's discretion.

A more in-depth guide to selecting $R_{VPC2}$ and $R_{VSC2}$ resistors can be found in section 8.3.2 in the UCC24636 datasheet.
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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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