

# DDR $V_{TT}$ Power Solutions: A Competitive Analysis

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## ABSTRACT

This application report describes the series stub termination logic (SSTL) and tracking termination voltage ( $V_{TT}$ ) in DDR applications. It analyzes and compares the power loss and voltage deviation of passive and active  $V_{TT}$  terminations, and highlights the advantages of active termination.

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## 1 Introduction

Double data rate (DDR) memory is the most popular type of dynamic RAM (DRAM). Computer, laptop, servers, and other electronic devices use DDR memory.

DDR memory power requires two power rails:  $V_{DDQ}$  (drain-to-drain core voltage) and  $V_{TT}$ . Typically the switching power supply provides power to the  $V_{DDQ}$  rail because of the high current requirement. Depending on the current requirement, the  $V_{TT}$  rail can be powered by either passive termination or by active termination. This application report explains how  $V_{DDQ}$  and  $V_{TT}$  provide power for DDR memory. It analyzes and compares the power loss and voltage deviation of two types of  $V_{TT}$  terminations, summarizes the advantages of active termination. This application report also describes some  $V_{TT}$  power solutions offered by Texas Instruments.

## 2 Series Stub Termination Logic (SSTL) Used in DDR Design

Figure 1 shows the series stub termination logic (SSTL) used in DDR design. It uses one series resistor ( $R_S$ ) connected from the output buffer (driver) to the memory (receiver) and one termination resistor ( $R_T$ ) connected to the termination rail ( $V_{TT}$ ). The typical  $V_{TT}$  voltage and  $V_{REF}$  are equal to  $V_{DDQ}/2$ .

When the output buffer is in a high state, the Q1 switch is on and Q2 switch is off. Also, the current flows from  $V_{DDQ}$  to  $V_{TT}$  through resistors  $R_S$  and  $R_T$ . Because the  $V_{TT}$  termination then sinks the current, the receiver input voltage ( $V_{IN}$ ) is higher than  $V_{REF}$ . When the output buffer is in a low state, Q1 is off and Q2 is on, the current flows from  $V_{TT}$  to ground thru  $R_T$  and  $R_S$ ,  $V_{TT}$  termination sources current, consequently  $V_{IN}$  is lower than  $V_{REF}$ .

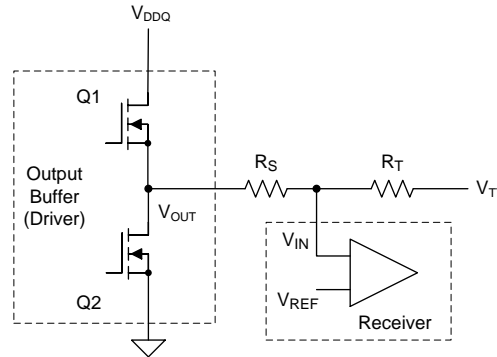


Figure 1. Series Stub Termination Logic (SSTL)

To avoid a data read/write error, the value of  $V_{IN}$  must be within the specification window. For example for SSTL\_18 (DDR2),  $V_{IN}$  must be higher than  $V_{REF} + 125\text{ mV}$  in order for receiver to interpret the high bit signal correctly.  $V_{IN}$  must be lower than  $(V_{REF} - 125\text{ mV})$  in order for the receiver to interpret the low bit signal correctly. If the value of  $V_{IN}$  is outside of the specification window, a data read/write error may occur.

Table 1. DC Input Logic Levels of SSTL\_18

SYMBOL	PARAMETER	MIN	MAX
$V_{IH(dc)}$	dc input logic high	$V_{REF} + 125\text{ mV}$	$V_{DDQ} + 300\text{ mV}$
$V_{IL(dc)}$	dc input logic low	$-300\text{ mV}$	$V_{REF} - 125\text{ mV}$

## 3 Power Dissipation of Passive Termination

The simplified circuit shown in Figure 2 illustrates a high bit line of SSTL\_18 (DDR2) with passive termination. The simplified circuit shown in Figure 3 illustrates a low bit line with passive  $V_{TT}$  termination. In these examples,  $V_{DDQ}$  voltage is 1.8 V and  $V_{REF}$  is 0.9 V. The on-resistance  $R_{ON}$  of Q1 and Q2 and its typical value  $20\ \Omega$  is used in the following calculation. The typical values of  $R_S$  and  $R_T$  are  $20\ \Omega$  and  $25\ \Omega$ , respectively. Two resistors ( $R_P$ ) with the same value act as passive termination.

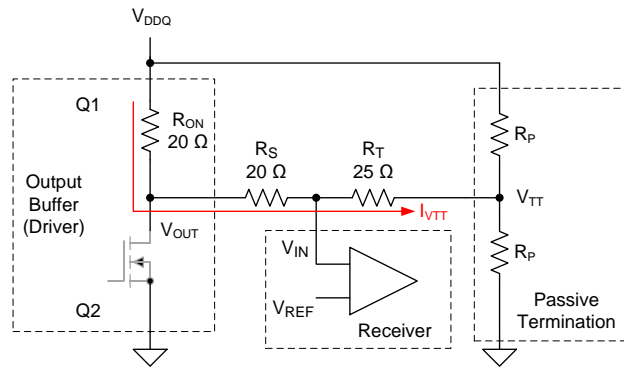


Figure 2. High Bit Line With Passive Termination

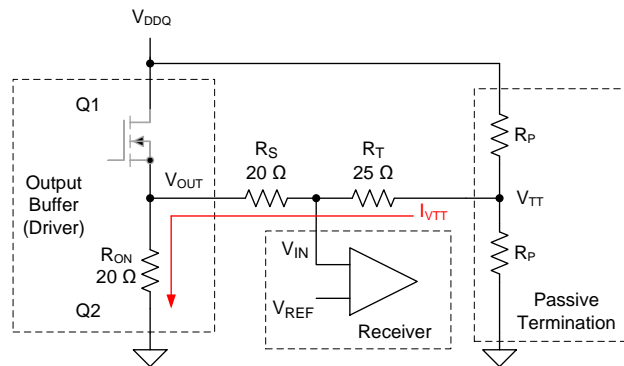


Figure 3. Low Bit Line With Passive Termination

In DDR memory, multiple bit lines share one  $V_{TT}$  voltage. The output buffer is either in a high state for the high bit or in a low state for the low bit. If the number of high bit lines and low bit lines is exactly equal, the  $V_{TT}$  sink current (current goes into termination) from high bit lines is equal to the source current (current goes out of termination) from low bit lines. As a result, the net  $V_{TT}$  current is zero. In this example, the  $V_{TT}$  voltage is exactly  $V_{DDQ}/2$ .

If the number of high bit lines and low bit lines are not equal (which is the typical case in the application) the  $V_{TT}$  voltage does not equal  $V_{DDQ}/2$ . The net  $V_{TT}$  current and the  $R_P$  resistor value determines the actual  $V_{TT}$  voltage.

Assuming the number of low bit lines is larger than that of high bit lines, the net  $V_{TT}$  current goes out of termination and  $V_{TT}$  voltage is lower than  $V_{DDQ}/2$ . Based on calculation, to make  $V_{IN}$  at high bit line higher than logic high threshold ( $V_{REF} + 125 \text{ mV} = 1.025 \text{ V}$ ),  $V_{TT}$  voltage must be higher than  $0.54 \text{ V}$ .

For a DDR2 memory application with 32 data lines and 10 address lines, there are total 42 lines. Assuming  $V_{TT}$  termination sources current and the  $V_{TT}$  voltage is  $0.54 \text{ V}$ , use [Table 2](#) to determine the required  $R_P$  resistor value and the total power loss on two resistors. As calculated, if all lines are low bit, this application requires two  $2.07\text{-}\Omega$  resistors. These resistors yield a total power loss of  $0.91 \text{ W}$ . In order to make the  $V_{TT}$  voltage higher than  $0.54 \text{ V}$  (for the purpose of increasing the margin), the  $R_P$  resistor value must be smaller and the power loss on two resistors increases.

**Table 2. Power Loss of Passive Termination**

BIT LINE QUANTITY		$I_{V_{TT}}$ (A)	$R_p$ ( $\Omega$ )	$P_{Loss}$ (W)
HIGH	LOW			
0	42	0.35	2.07	0.91
1	41	0.32	2.24	0.84
2	40	0.29	2.46	0.77
3	39	0.27	2.71	0.69
4	38	0.24	3.03	0.62
5	37	0.21	3.43	0.55
6	36	0.18	3.95	0.48
7	35	0.15	4.65	0.40
8	34	0.13	5.67	0.33
9	33	0.10	7.25	0.26
10	32	0.07	10.06	0.19
11	31	0.04	16.40	0.11
12	30	0.02	44.44	0.04

#### 4 Passive Termination vs. Active Termination

Compared to passive termination operation, active termination operation offers a smaller amount of  $V_{TT}$  voltage deviation and lower power loss. Using the TPS51200 device as an example, the voltage deviation is below 25 mV when the  $V_{TT}$  current is 2 A.

[Table 3](#) compares passive termination and active terminations in DDR2 applications. In this table, two 2- $\Omega$  resistors act as passive termination. The TPS51200 device is used as active termination. Because the  $V_{TT}$  voltage with active termination is very close to 0.9 V, use 0.9 V to calculate across the current range. This table lists the  $V_{TT}$  voltage deviation and power loss of two types of terminations at different  $V_{TT}$  current conditions.

As the calculations listed in [Table 3](#) shows, the  $V_{TT}$  voltage during passive termination operation drops significantly when the current increases. When the current level is 0.35 A, the  $V_{TT}$  voltage drops from 0.9 V to 0.55 V. If the current is higher than 0.35 A,  $V_{TT}$  voltage drops below 0.54 V, and the  $V_{IN}$  voltage in a high-bit line no longer remains within the specification window. As a result of this change, a read/write error may occur.

**Table 3. Comparison Between Passive Termination and Active Termination**

$V_{TT}$ Source Current (A)	PASSIVE TERMINATION		ACTIVE TERMINATION	
	$V_{TT}$ (V)	$P_{Loss}$ (W)	$V_{TT}$ (V)	$P_{Loss}$ (W)
0.00	0.90	0.81	0.9	0
0.05	0.85	0.81	0.9	0.045
0.10	0.80	0.82	0.9	0.09
0.15	0.75	0.83	0.9	0.135
0.20	0.70	0.85	0.9	0.18
0.25	0.65	0.87	0.9	0.225
0.30	0.60	0.90	0.9	0.27
0.35	0.55	0.93	0.9	0.315

In addition to the smaller voltage deviation, the power loss during active termination operation is much lower than that during passive termination operation. When  $V_{TT}$  current is 0 A, the power loss during active termination operation is nearly 0 W, whereas it is 0.81 W during passive termination operation. The effect of this difference is that passive termination consumes much more power than active termination when  $V_{TT}$  current is very small in standby mode. When  $V_{TT}$  current is 0.35 A, the power loss of active termination is 0.315 W. This amount of power loss is only one-third of 0.93-W power loss of passive termination.

Use similar calculations to determine DDR3, DDR3L and DDR4 application comparisons.

## 5 V<sub>TT</sub> Power Solution Offered By TI

Because of the advantages of small voltage deviation and low power loss, most DDR applications now use active V<sub>TT</sub> terminations. [Table 4](#) lists the V<sub>TT</sub> power solutions offered by TI. Both the TPS51206 device and the TPS51200 device are sink/source LDO regulators requiring small output capacitance and minimum external components count. The TPS51206 device supports 2 A and the TPS51200 supports 3 A. The TPS53317A is a 6-A switching regulator which is suitable for high-current applications.

TI also provides V<sub>DDQ</sub> and V<sub>TT</sub> integrated power solutions such as the [TPS51116](#) and [TPS51916](#) devices. See the TI website and device data sheets for more information.

**Table 4. TI V<sub>TT</sub> Power Solutions**

DEVICE	<a href="#">TPS51200, TPS51200-Q1</a>	<a href="#">TPS51206</a>	<a href="#">LP2996</a>	<a href="#">LP2997</a>	<a href="#">LP2998, LP2998-Q1</a>	<a href="#">TPS53317A</a>
MEMORY TYPE	DDR, DDR2, DDR3, DDR3L, LPDDR3, DDR4,	DDR2, DDR3, DDR3L, LPDDR3, DDR4,	DDR, DDR2	DDR2	DDR, DDR2, DDR3, DDR3L	DDR, DDR2, DDR3, DDR3L, LPDDR3, DDR4
I <sub>OUT</sub> (A)	3	2	1.5	0.5	1.5	6
V <sub>IN</sub> (V)	1.1 to 3.5	1 to 3.5	1.8 to 5.5	1.8 to 5.5	1.35 to 5.5	0.9 to 6

## 6 Summary

In a passive termination application, a low-value resistor helps to reduce V<sub>TT</sub> voltage deviation and helps avoid read/write error, but results in high power loss. A high-value resistor helps to reduce power loss but it increases the chance of bit errors.

Compared to passive termination, the active termination solution brings much lower power loss and smaller V<sub>TT</sub> voltage deviation, hence, improves data read/write accuracy and integrity.

Because an application typically converts V<sub>TT</sub> power from V<sub>DDQ</sub> power, the active V<sub>TT</sub> termination demands a lower amount of current from the V<sub>DDQ</sub> rail. Therefore, the V<sub>DDQ</sub> current rating can be reduced when the application uses active termination.

## 7 References

1. Jim Aliberti, "[How To Match The DDR Memory Power Solution To The Application](#)," Texas Instruments, 2013
2. Peter James Miller, "[Powering DDR Memory and SSTL](#)," Texas Instruments, 2011
3. JEDEC Standard, JESD8-15A
4. [TPS51200 datasheet](#)

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