Application Report

SLUA920B–October 2018–Revised October 2019

UCC28056x, Using Auxiliary Winding Voltage for Driving ZCD/CS Pin

Sonal Singh

ABSTRACT

This application report provides an alternate approach to sensing the zero crossing detection aimed for customers who prefer using an auxiliary winding. The advantage of using the aux winding approach is that UCC28056x application designs are more robust and have better immunity to interference from adjacent nodes. UCC28056x is a single-phase PFC boost stage working on an innovative mode method, operating in transition mode (TM) during full load, and transitioning to discontinuous conduction mode (DCM) during reduced load. This application report provides a comparative analysis of the current method of biasing the ZCD/CS pin voltage across the MOSFET versus the modified approach of introducing an auxiliary winding as shown on a high level in Figure 1 and Figure 2.

The new variants of the UCC28056x devices help resolve the noise interference in the application designs by introducing a second level of comparators for the ZCD detection. Table 1 shows the feature description of the UCC28056x devices. Refer to the *UCC28056 6-Pin High Performance CRM/DCM PFC Controller Data Sheet* for a full feature comparison.

Table 1. Feature Description

FEATURE	UCC28056	UCC28056A	UCC28056B	UCC28056C
ZCD improvements	No	Yes	Yes	Yes

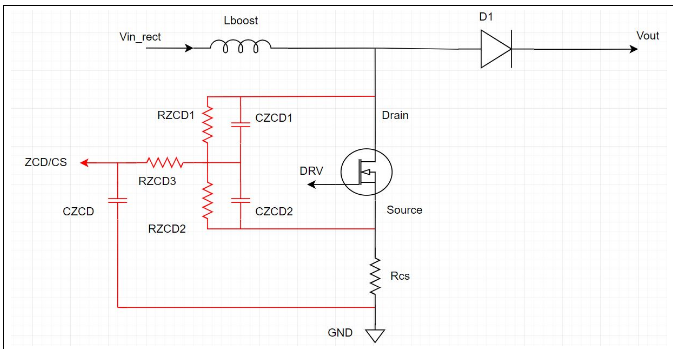

Figure 1. Direct Drain Approach

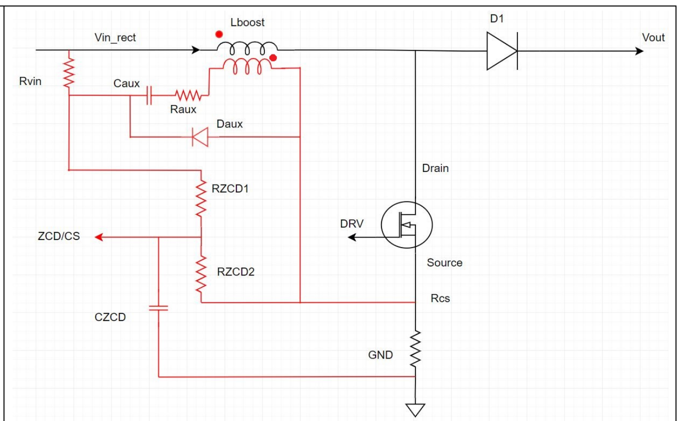

Figure 2. Aux Winding Approach

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1 Introduction

UCC28056x has a ZCD/CS pin which combines the functionality of current sense and the zero crossing detection into a single pin. This application report talks in depth about the more conventional method of ZCD sensing by using a separate winding. This approach is easier to implement and the signal has more immunity to the surrounding interference because the signal is not sensed across the MOSFET.

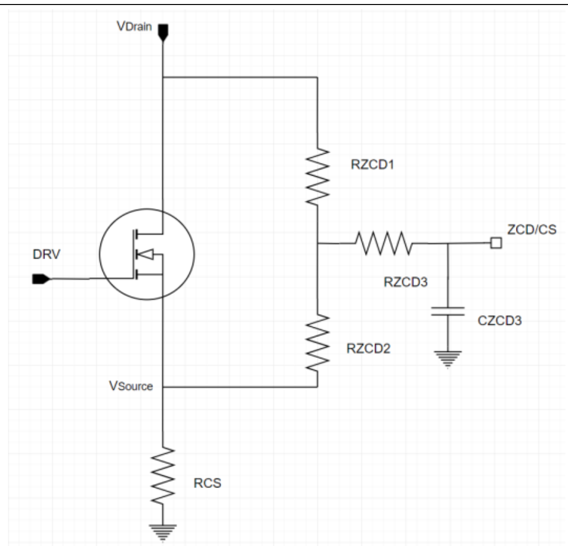

Figure 3. Direct Drain Approach without Aux Winding

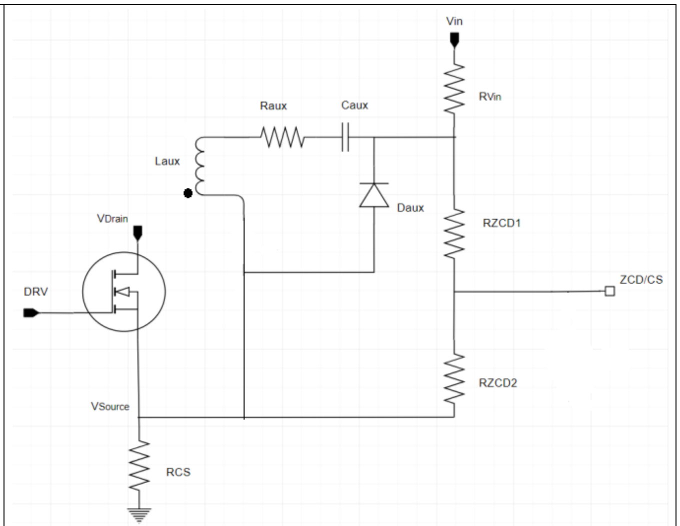

Figure 4. Aux Winding Approach

The approach shown in Figure 4 can be used to replace Figure 3 in order to avoid any sensitivity at the ZCD/CS pin. When the controller is not switching, the voltage across the auxiliary winding is zero, so only the pullup resistor contributes to the standby power. The impedance of the ZCD divider is high and placing it close to the ZCD/CS pin of the controller makes the signal more immune to the disturbances by the capacitive coupling from the nearby switching nodes. Although the direct drain approach eliminates the need of an aux winding, the signal sensing is more complicated and prone to increased noise susceptibility. By using an aux winding approach across the inductor, these issues can be mitigated.

2 Advantages of Using the AUX Winding Approach

This section highlights the advantages of using the proposed auxiliary winding approach.

- All the nodes are low impedance nodes and are relatively insensitive to layout, except the ZCD/CS pin.
- Only small, low-voltage resistors are required at the ZCD/CS pin, therefore, the pin has a smaller parasitic capacitance to surrounding switched nodes.
- High voltage cap is not required.
- Lower cost

3 Calculations for AUX Winding

This section contains the calculations for the component values for this approach mentioned in Figure 4.

3.1 ZCD Divider

The resistor divider for ZCD/CS pin can be calculated as:

$$Vaux \times \frac{RZCD2}{RZCD2 + RZCD1} = V_{ZCBoRise}$$

where

- Vaux is the voltage across the aux winding, which can be calculated as:

$$Vaux = \frac{Vin_{min}\sqrt{2}}{N_{PA}} \tag{2}$$

- Npa is the primary to aux turn ratio; Npa equals 10.4 for the modified EVM.

$$Vaux = \frac{85\sqrt{2}}{10.4} = 11.5V \tag{3}$$

- RZCD2 = 20 kΩ and $V_{ZCBoRise}$ = 0.3 V from the electrical characteristics table in the data sheet. (3)

If you substitute all the above values to solve for RZCD1 from Equation 1, you get RZCD1 = 750 kΩ.

$V_{ZCBoRise}$ is used to ensure that the attenuation factor of the ZCD and Rvin divider matches the attenuation factor on the original EVM.

3.2 Ratio Check for ZCD Divider

There are a number of internal voltage thresholds driven by the attenuated drain voltage signal supplied to the ZCD/CS pin.

$$K_{ZC} = N_{PA}\left[\frac{RZCD1}{RZCD2} + 1\right] \tag{4}$$

If you substitute the RZCD1 and RZCD2 from Equation 4, you get K_{ZC} = 400.4.

Having this ratio (KZC) the same as the original EVM ensures that the other thresholds like brown-out ($V_{ZCBoRise}$), line feedforward rise and fall ($V_{FFxRise}$, $V_{FFxFall}$), and the second overvoltage protection (V_{OVP2th}) are still at the same levels. There is a limited scope to vary the attenuation ratio because it impacts all of these threshold values.

3.3 R_{vin} Divider

The resistor divider from the rectified voltage line to ensure start-up can be calculated as:

$$V_{in\_min}\sqrt{2} \times \frac{RZCD2}{R_{vin} + RZCD1 + RZCD2} = V_{ZCBoRise} \tag{5}$$

$V_{ZCBoRise}$ is used to ensure that the attenuation factor of the ZCD and Rvin divider matches the attenuation factor on the original EVM.

Substituting the values of RZCD1 and RZCD2 from Equation 5, R_{vin} = 7.2 MΩ.

Two resistors in series valued at 4.7 MΩ and 2.7 MΩ were used on the modified EVM.

3.4 Ratio Check for R_{vin} divider

Check the ratio for the attenuation divider to ensure that it matches to the original EVM. This can be done using Equation 6:

$$K_{ZC\_Rvin} = \left[\frac{R_{vin} + RZCD1}{RZCD2} + 1\right] \tag{6}$$

If you substitute the values in Equation 6, you get:

$$K_{ZC\_Rvin} = 398.5 \tag{7}$$

3.5 Caux

Caux charges up during the TON to V_{caux}, which can be defined from Equation 8:

$$V_{caux} = \frac{N_A}{N_P} \times V_{in} - V_{fd}$$

where

- V_{fd} is the forward diode voltage drop, which is 0.6 V (8)

Ideally the Caux discharge is fast enough to trace the Vaux voltage. The value of the Caux voltage discharge slope when V_{in} is falling is greater than the slope of Vaux. The following time constant can be used to ensure this slope.

$$R_{ZCD} \times C_{aux} = 200\mu sec$$

where

- RZCD is total resistance feeding into the ZCD pin (RZCD = RZCD1 + RZCD2) (9)

$$\left[RZCD1 + RZCD2\right] \times C_{aux} = 200\mu sec \quad (10)$$

If you substitute the value of the selected ZCD divider resistance, you can calculate the value of the auxiliary capacitance as:

$$C_{aux} = 0.25\eta F \quad (11)$$

270 pF of Caux was selected on the modified EVM.

3.6 Raux

The value of Raux and Caux are chosen to ensure that the Caux charging occurs very quickly cycle by cycle. Use Equation 12 to select the time constant during the charging period.

$$Raux \times Caux = 100nsec \quad (12)$$

If you substitute the value of Caux from Equation 12, you get:

$$Raux = 400\Omega \quad (13)$$

390 Ω of Raux was used on the modified EVM.

3.7 Daux

It is recommended to use a diode with small reverse leakage current and forward voltage drop. A small signal diode can be a good choice. A bigger voltage drop is replicated in the VOVP2 threshold as mentioned in Equation 15. It is recommended to use a 1N4148 or a similar diode.

4 Results

The section shows comparative data between the direct drain and the aux winding approach including the waveform and the calculations supporting the difference in the results.

4.1 ZCD/CS Waveform Comparison

Figure 5 and Figure 6 show the ZCD/CS waveform of the original and the modified EVM taken under 90 Vac input at a 100 mA load condition.

Figure 5. ZCD/CS Original EVM Waveform

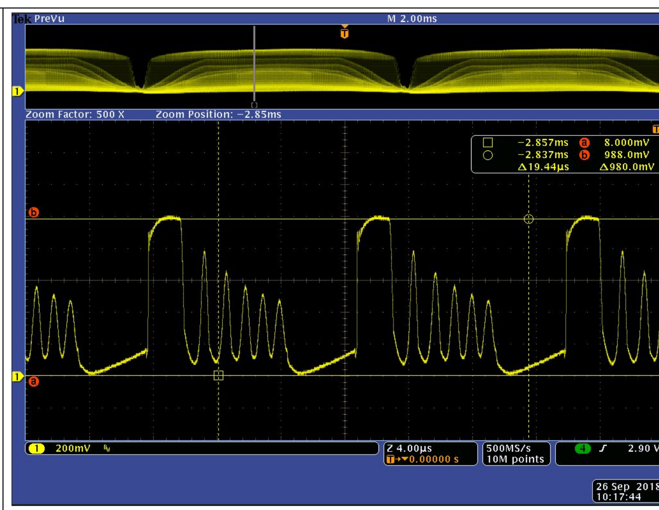

Figure 6. ZCD/CS Modified EVM Waveform

4.2 Brown-in Threshold

Table 2 shows the brown-in threshold levels of the original EVM and the modified EVM. Table 2 shows that the modification does not affect this threshold.

Table 2. Brown-in Threshold Comparison

THRESHOLD LEVELS	ORIGINAL EVM	MODIFIED EVM
BROWN-IN THRESHOLD	84 Vac	83 Vac

4.3 OVP2 Threshold

The UCC28056 has an OVP2 comparator with a fixed internal threshold, Vovp2th, that monitors the ZCD/CS pin voltage during the discharge time. The OVP2 threshold is 1.125 V as specified in the *UCC28056 6-Pin High Performance CRM/DCM PFC Controller Data Sheet*. Remember to factor in the 0.6 V diode drop from Daux.

You can calculate the value of the output voltage at which the OVP2 level would trip from this information. The following equations are working backwards from the ZCD/CS pin.

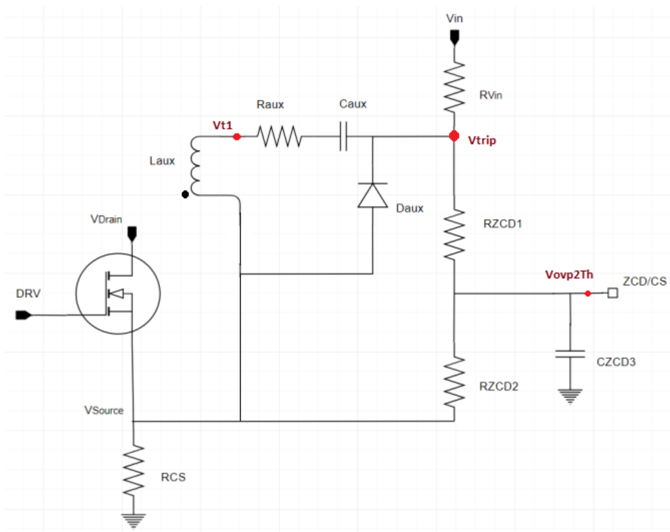

Figure 7. AUX Winding Approach with Reference Voltage Points

$$V_{trip} = \frac{RZCD1 + RZCD2}{RZCD2} \times V_{OVP2Th}$$
$$V_{OVP2T} = 1.125V \;:\; known\;\; from\;\; the\;\; electrical\;\; table$$
$$V_{trip} = \frac{750k\Omega + 20k\Omega}{20k\Omega} \times 1.125V$$
$$V_{trip} = 43.31V \tag{14}$$

Accounting for the diode drop, you can say:

$$V_{t1} = V_{trip} - V_{fd}$$
$$V_{t1} = 43.31V - 0.6V = 42.71V \tag{15}$$

Vt1 in Equation 15 is scaled by the turn ratio of the inductor and reflected at the output during the discharge period when the boost diode is conducting.

$$V_{out} = N_{PA} \times V_{t1}$$
$$V_{out} = 10.4 \times 43.31 = 444.21V \tag{16}$$

Table 3 compares the theoretical Vout value to the original and the modified EVM.

Table 3. Overvoltage Protection Threshold Comparison for the UCC28056

THRESHOLD LEVELS	ORIGINAL EVM	MODIFIED EVM
OVP2_UCC28056	423 V	443 V

Refer to the UCC28056x selection guide for a feature comparison.

4.4 OCP1 Threshold

The OCP1 level is a cycle-by-cycle peak current protection that terminates the Ton duration early if the current sense-to-pin voltage rises above 0.5 V. This is achieved by limiting the peak inductor current, which avoids inductor saturation.

This can be checked by increasing the R_{CS} value:

$$Rcs_{total} = R9 \parallel R10 \parallel R11 \quad (from \quad the \quad original \quad EVM)$$
$$Rcs_{total} = 0.13 \parallel 0.13 \parallel 453k\Omega$$
$$Rcs_{total} = 0.065\Omega \tag{17}$$

The normal switching operation continues and the controller is able to maintain the output regulation at full load condition 423 mA for an R_{cs} value of 65 mΩ. This also ensures the required peak inductor current does not cause the early termination of the TON period.

Changing R_{cs} to 3.54 times the original value causes the TON period to terminate early by a factor calculated by Equation 18.

$$ILoad_{mod} = \frac{423mA}{3.54}$$
$$ILoad_{mod} = 120mA \tag{18}$$

Table 4 shows the OCP1 threshold comparison of the original and the modified EVM. A resistor value of 230 mΩ was selected for the Rcs.

Table 4. Overcurrent Protection Threshold Comparison

THRESHOLD LEVELS	ORIGINAL EVM	MODIFIED EVM
OCP1	140 mA load	130 mA load

4.5 Standby Power Comparison

Equation 19 and Equation 20 show the contribution of the aux winding approach to the total standby power measurements. The electronic load has been disconnected for this test. The average input power is measured across the input and external VCC over a 10 min interval.

$$P_{Stdby} = \frac{{V_{inac}}^2}{R}$$

where

- V_{inac} is the peak of line bulk voltage
- R is the total resistance in the impedance path (19)

$$P_{Stdby} = \frac{(265\sqrt{2})^2}{Rin + RZCD1 + RZCD2}$$
$$P_{Stdby} = \frac{265\sqrt{2}^{\,2}}{7.2M + 750k + 20k}$$
$$P_{Stdby} = 17.6mW \tag{20}$$

Table 5 contains the modified EVM standby power measurements.

Table 5. Total Standby Power

INPUT VOLTAGE (Vrms)	INPUT POWER (mW)	VCC VOLTAGE (V)	VCC CURRENT (µA)	TOTAL STANDBY POWER: MODIFIED EVM (mW)
85	27.36	12.01	102.89	28.596
115	28.44	12.01	102.98	29.677
230	64.7	12.01	103.12	65.938
265	69.52	12.01	103.5	70.763

Figure 8 shows the comparative difference in standby power between the original UCC28056 and the modified EVM UCC28056..

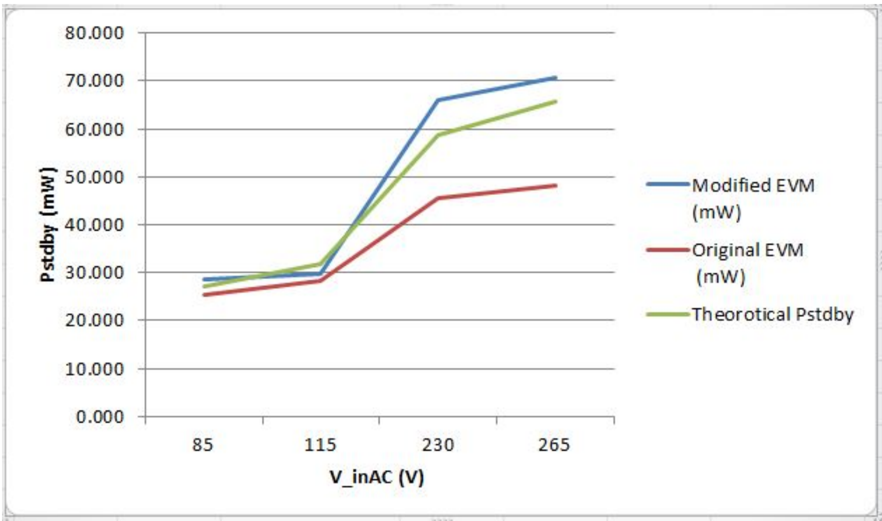

Figure 8. Standby Power Comparison for the UCC28056

4.6 Start-up

Figure 9 through Figure 16 show the output voltage behavior when the line voltage has already been applied and the instant the VCC voltage exceeds the start-up threshold on the EVM with the new approach. CH1 is Vout, CH4 is Vin_AC, and CH3 is Vcc.

Figure 9. 85 V_{inac} at NL

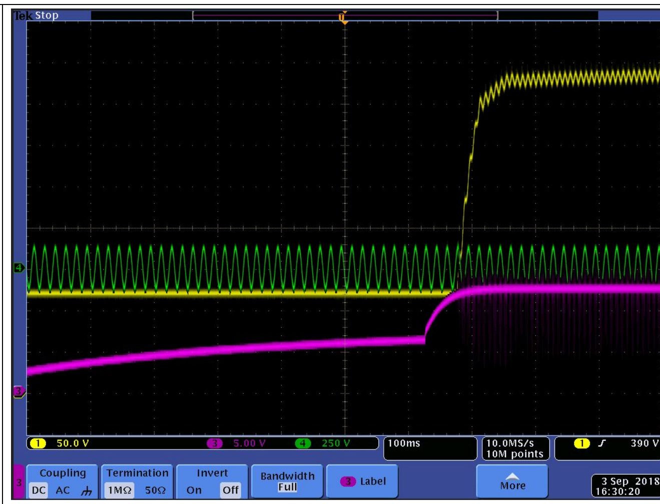

Figure 10. 85 V_{inac} at FL

Figure 11. 115 V_{inac} at NL

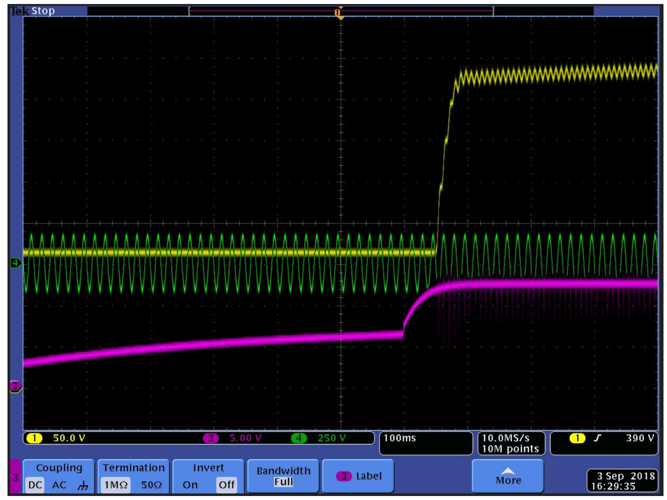

Figure 12. 115 V_{inac} at FL

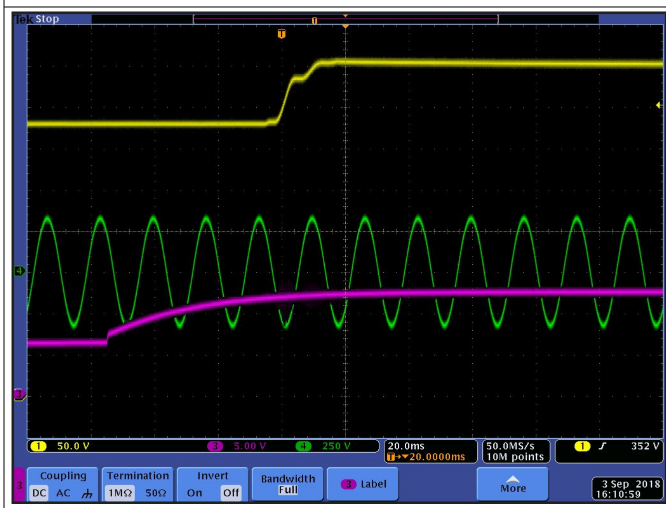

Figure 13. 230 V_{inac} at NL

Figure 14. 230 V_{inac} at FL

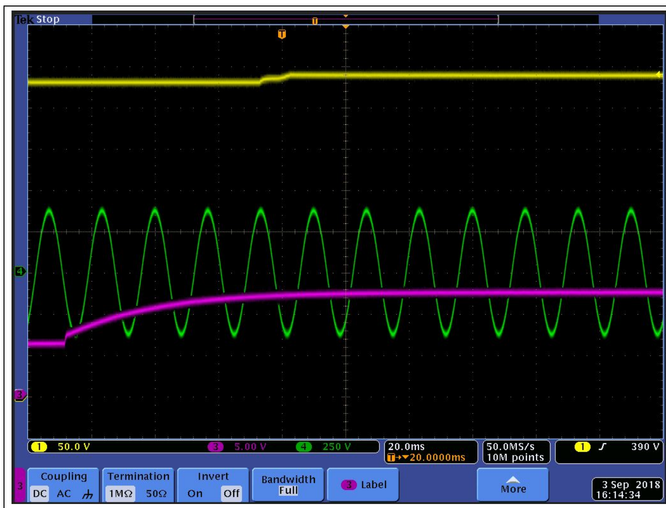

Figure 15. 265 V_{inac} at NL

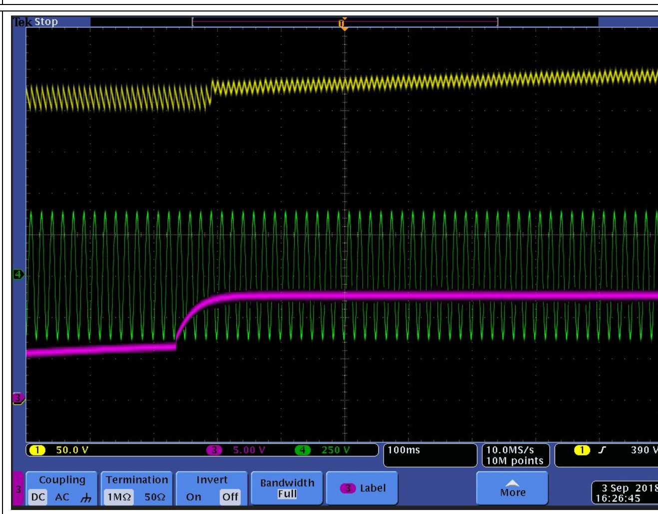

Figure 16. 265 V_{inac} at FL

4.7 Valley Switching

Figure 17 through Figure 20 show drain-to-source voltage of the MOSFET and the valley switching action on the EVM with the modified EVM.

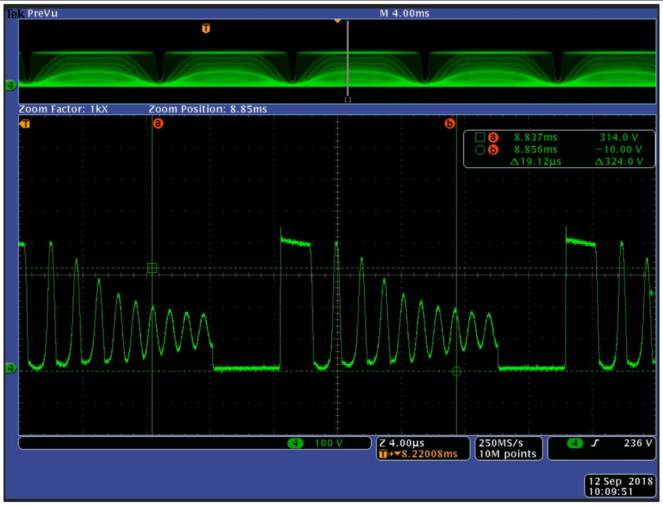

Figure 17. 85 V_{inac} at 60 mA Load

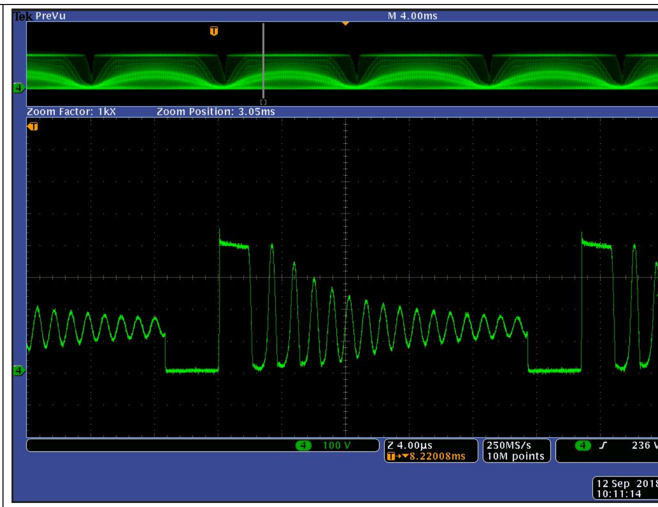

Figure 18. 115 V_{inac} at 60 mA Load

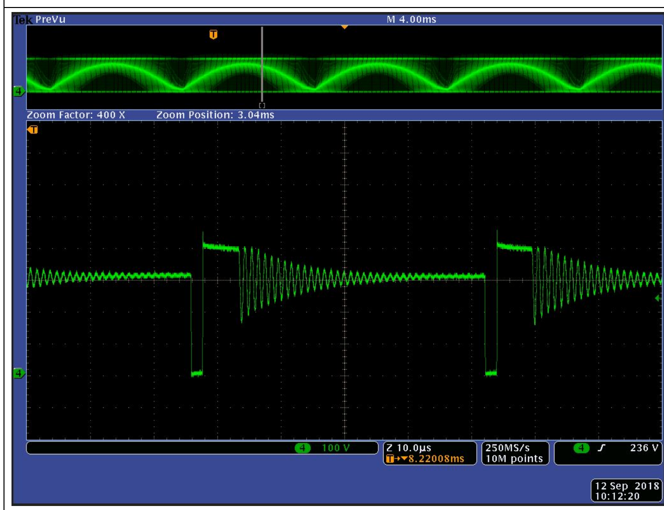

Figure 19. 230 V_{inac} at 100 mA Load

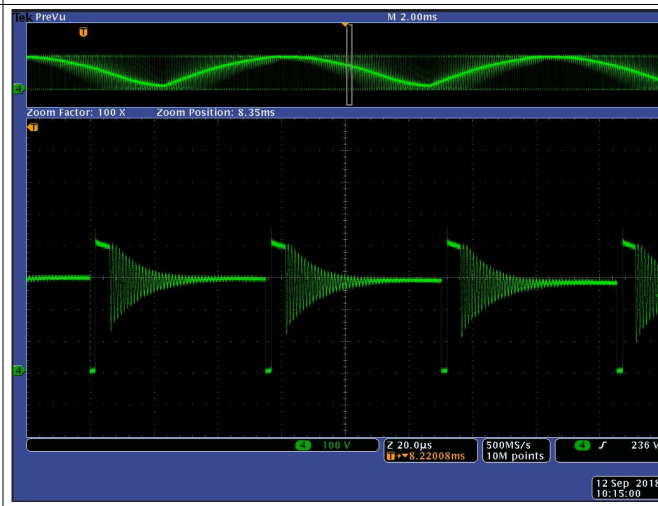

Figure 20. 265 V_{inac} at 100 mA Load

4.8 Transient Response

Figure 21 and Figure 22 show the transient response of the EVM with the aux winding approach where CH1 is Vout and CH4 is Iout.

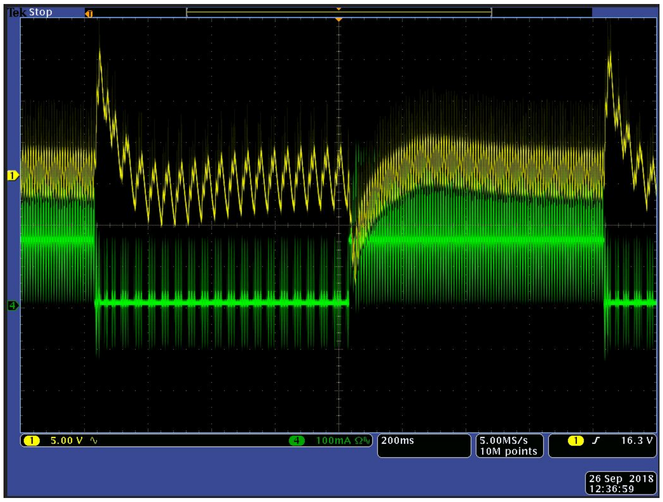

Figure 21. No-Load to 200 mA at 90 Vac

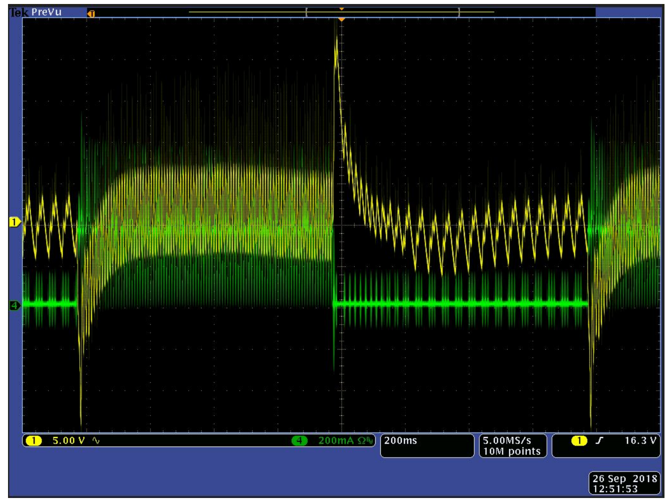

Figure 22. No-Load to 400 mA at 90 Vac

4.9 *Line Voltage and Line Current*

Figure 23 and Figure 24 illustrate the low-line, high-line voltage, and current waveforms where CH4 is V_{inac} and CH2 is I_{inac}.

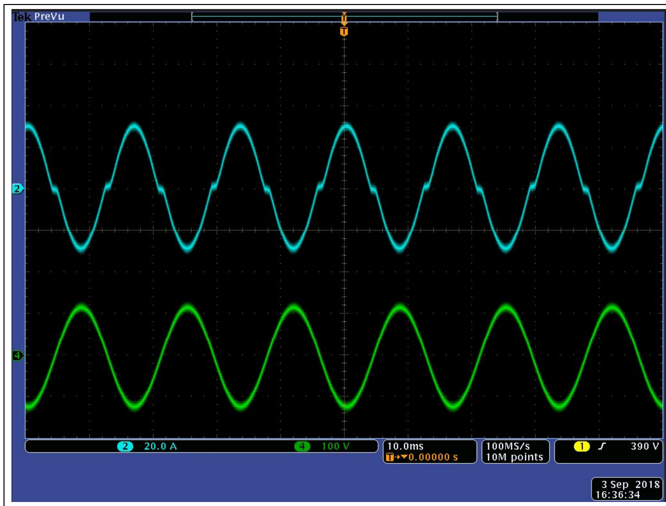

Figure 23. Low-line Voltage and Current Waveforms

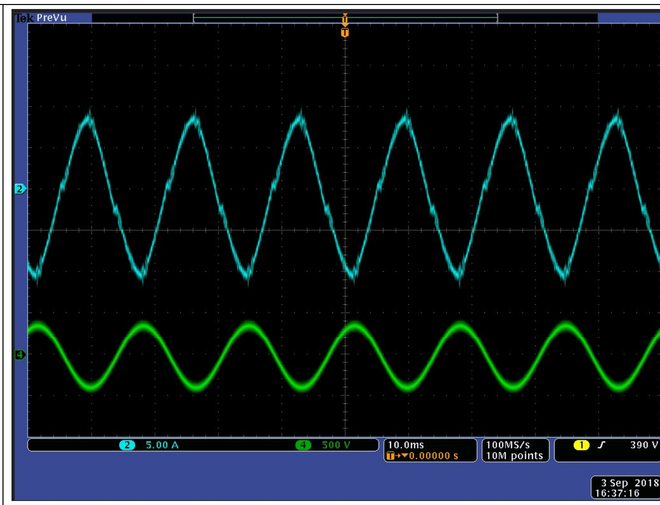

Figure 24. High-line Voltage and Current Waveform

5 Layout Guidelines

The ZCD/CS resistor network is very sensitive to parasitic capacitance. This capacitance can be present between the RZCD1 or RZCD2 resistor nodes and the surrounding high voltage switching nodes. The presence of this parasitic capacitance can cause false fault detection triggering of OCP2 and OVP2, causing the controller to shut down and operate in hiccup mode with an interval of 1 sec when attempting to turn on.

- RZCD2 must be placed as close as possible to the ZCD/CS pin on the controller.
- Rvin and RZCD1 must be placed as close as possible to the RZCD2 resistor.
- PCB traces connecting RZCD1 and Rvin must be kept as short as possible. The width of these traces must be very narrow to allow for the minimum parasitic capacitance.
- The traces connecting the high-valued resistors feeding to the ZCD/CS pin, DRV pin, and Vrect must be at least 1 cm apart to avoid coupling.
- It is important to keep the traces feeding the ZCD/CS pin as far as possible to the high switching traces

(VDrain).

Figure 25 shows an example layout of the modified EVM bottom layer with highlighted circuit.

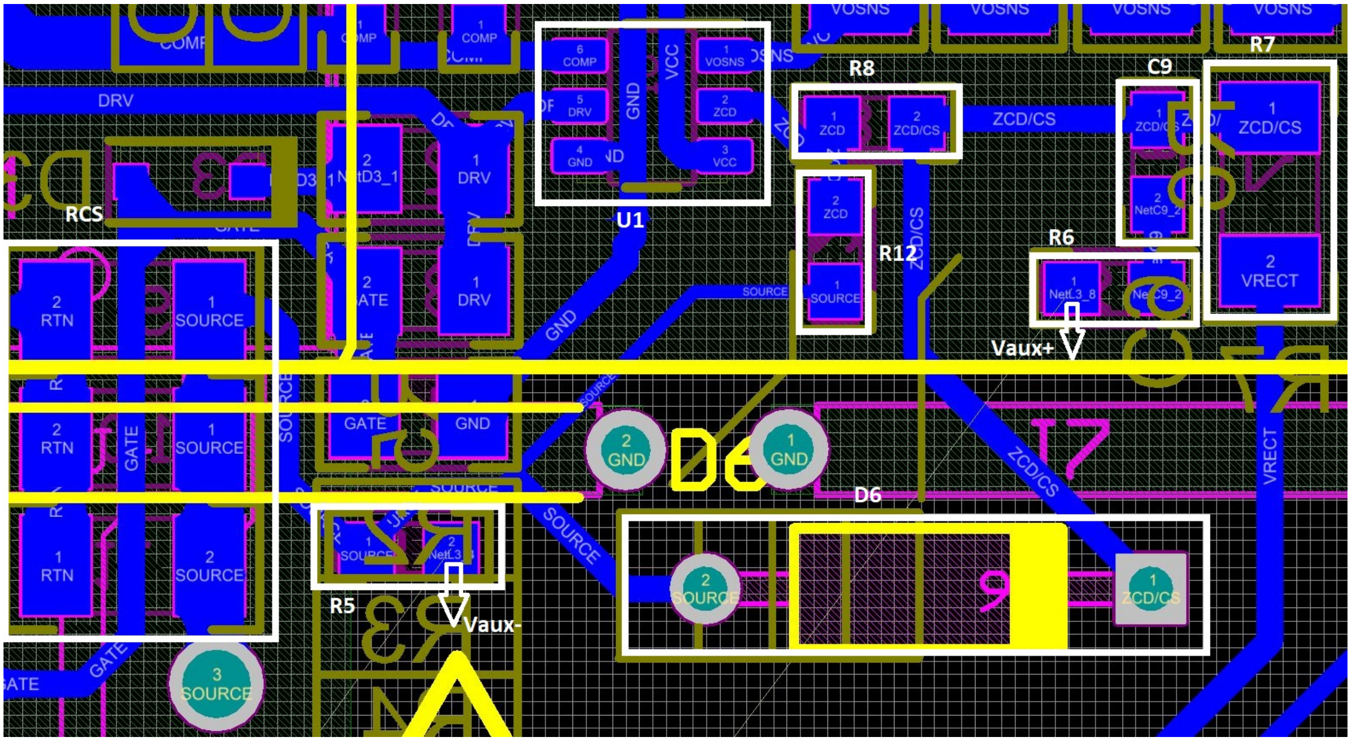

Figure 25. Layout Example; EVM Bottom Layer

See Figure 25 to identify the modified circuit elements. Figure 26 is an updated schematic diagram with the proposed approach.

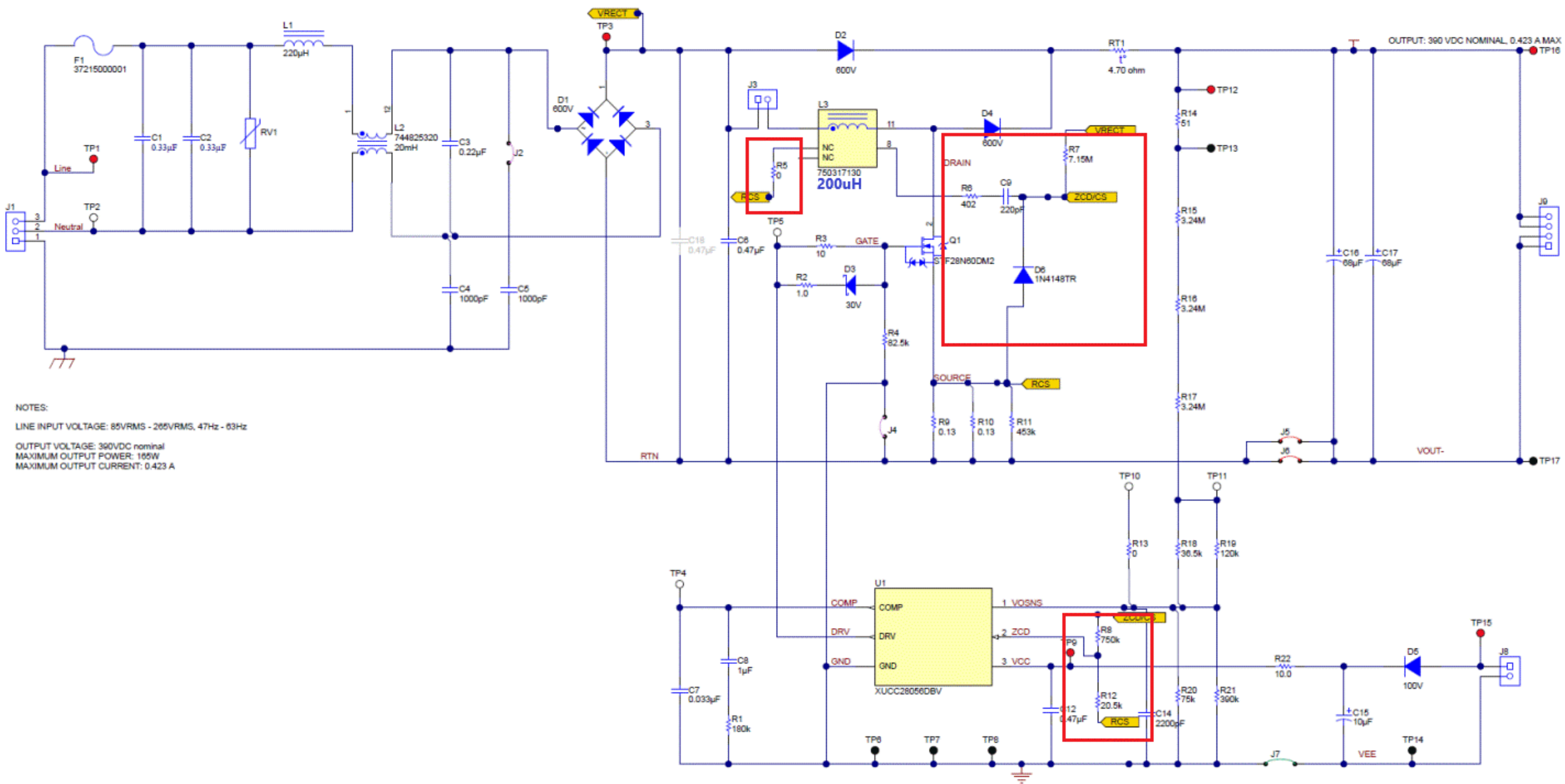

Figure 26. Modified EVM Schematic

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.