Application Report
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HEV/EV Traction Inverter Design Guide Using Isolated IGBT and SiC Gate Drivers

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ABSTRACT

This document describes how to design a HEV/EV traction inverter drive system using the advantages of TI's isolated gate drivers diagnostic and protection features.

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1 Introduction

Intelligent means of vehicle monitoring and protection are necessary due to the full electrification of vehicles and the stringent safety requirements that vehicle manufacturers are held to. The electronics systems and components must remain functional throughout the vehicle's lifetime in order to maintain safe operation. The traction inverter is vital to the drive system and includes protection and monitoring auxiliary circuits to prevent system-level failure modes such as over- and under-torque, unintentional motor commutation, or motor shutdown. This design guide reviews HEV/EV architectures, the failure modes of the traction inverter system, and how the gate driver and surrounding circuits can be used to enhance the reliability of the system. Texas Instruments' UCC217xx-Q1 family of reinforced isolated gate drivers have integrated protection and monitoring features that simplify the design of high-power traction inverter systems. Such features include fast over-current protection or short-circuit protection, isolated temperature and voltage sensing, and under voltage lockout.

2 HEV/EV Overview

This section describes the key components of an HEV/EV automotive powertrain system.

2.1 HEV/EV Architectures

The electrification of vehicles has revolutionized the transportation industry and has resulted in technological advancements in both the automotive and semiconductor industries. Electrified vehicles including both hybrid electric (HEV) and full electric (EV) vehicles consist of various power electronics systems for regulating power from the grid, managing the battery storage element, and ultimately driving the vehicle. Electric motors are used to drive the wheels of the vehicle or to act as a generator to transfer mechanical energy into electric energy to store in the battery. HEVs use a combination of electric motors and generators, used as a low-power starter and alternator or to fully drive the vehicle, along with the internal combustion engine (ICE) typically used as the primary source of the vehicle's motion. The EV, on the other hand, utilizes electric motors as the primary source of vehicle motion as well as for regeneration.

The main HEV architectures are series, parallel and combination of series and parallel, shown in Figure 1. In the series configuration (a), the ICE is indirectly tied to the transmission through the electric motor. The power electronics three-phase drive derives power from the ICE through the generator as well as from the battery. In this architecture, the ICE is optimized for a certain range of speed allowing for minimized size and increased efficiency. This is the simplest HEV architecture with regards to mechanical complexity since there is no coupling of mechanical energy.

The parallel HEV configuration (b) utilizes a combination of the ICE and electric motor mechanically coupled. The electric drive is primarily used as a low-power starter and alternator in this architecture, and is thus lower power. The efficiency of the ICE is lower due to the larger operating range but the size of the electric motor is minimized because it does not need to provide as much power as the ICE.

The series/parallel configuration (c) combines the two previous methods to achieve better efficiency. Mechanical coupling is performed by a planetary gear and the ICE and electric drives combine the traction power. In this case, the electric motor and ICE can be designed to operate within specified output ranges to improve their efficiency.

In each case, the three phase inverter is used to drive the electric motor. The inverter design varies based on the power output requirements which depends on architecture. The proper control of the inverter directly impacts the motor's efficiency and the overall efficiency of the vehicle.

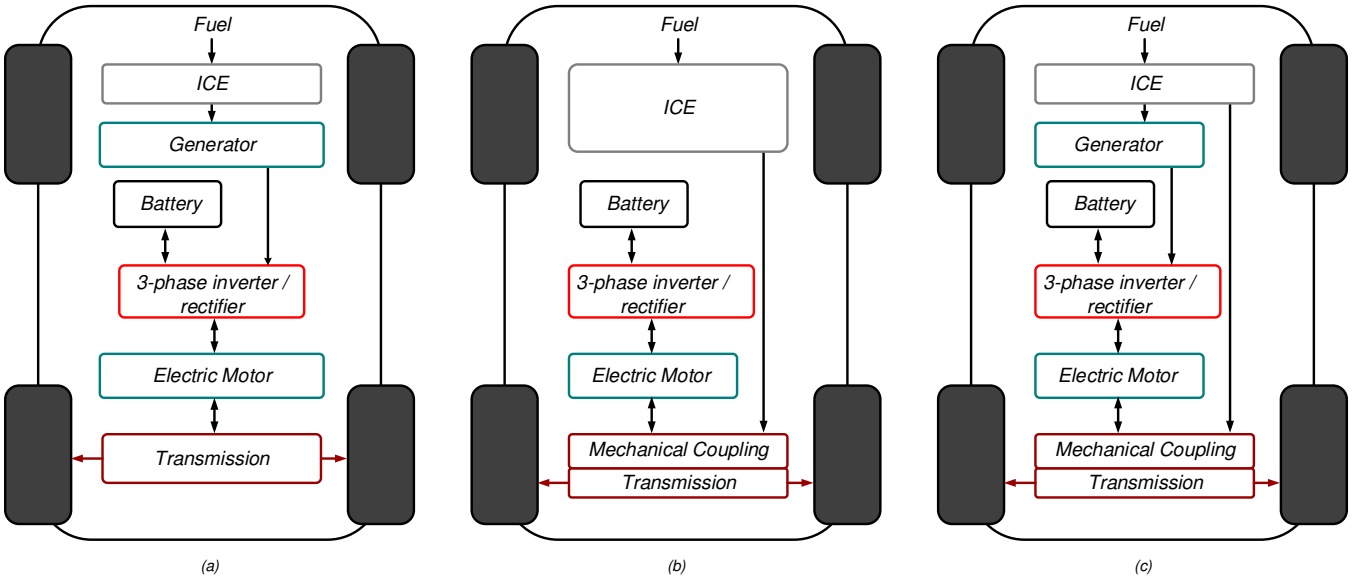

Figure 1. HEV Architectures

The pure electric vehicle, on the other hand, does not have an ICE and relies solely on the energy of the battery. Some different configurations of electric motor is shown in Figure 2. Similar to the HEV, each architecture results in different power requirements for the inverter. The electric motor may be directly tied to the wheel as shown in configurations (a) and (b) or tied to the wheel through a differential as shown in (a) and (c). Direct in-wheel drives has the benefit of simplicity and high efficiency with low maintenance, but must typically be larger in size due to low-speed requirements. The differential drive allows for high power density such that the motor can operate at a high RPM while the differential provides a fixed gear ratio. The drawback is that the mechanical gears require maintenance and has transmission loss.

High-voltage Li-ion batteries are commonly used as the energy storage unit to provide the maximum amount of capacity, minimal weight, and highest efficiency. With current technology, including various battery chemistries and power electronics efficiency, EVs still have limited range compared to HEV and plug-in HEVs. High performance EVs rely on increased power level of the traction inverter, minimization of the electronics' size, and complex controls based on sensed signals.

By increasing the efficiency and robustness of the inverter comes the increase of overall vehicle efficiency. The gate drivers makes an impact by providing the driving force behind each power switch in the inverter, as well as protection and monitoring to reduce the likelihood of failure.

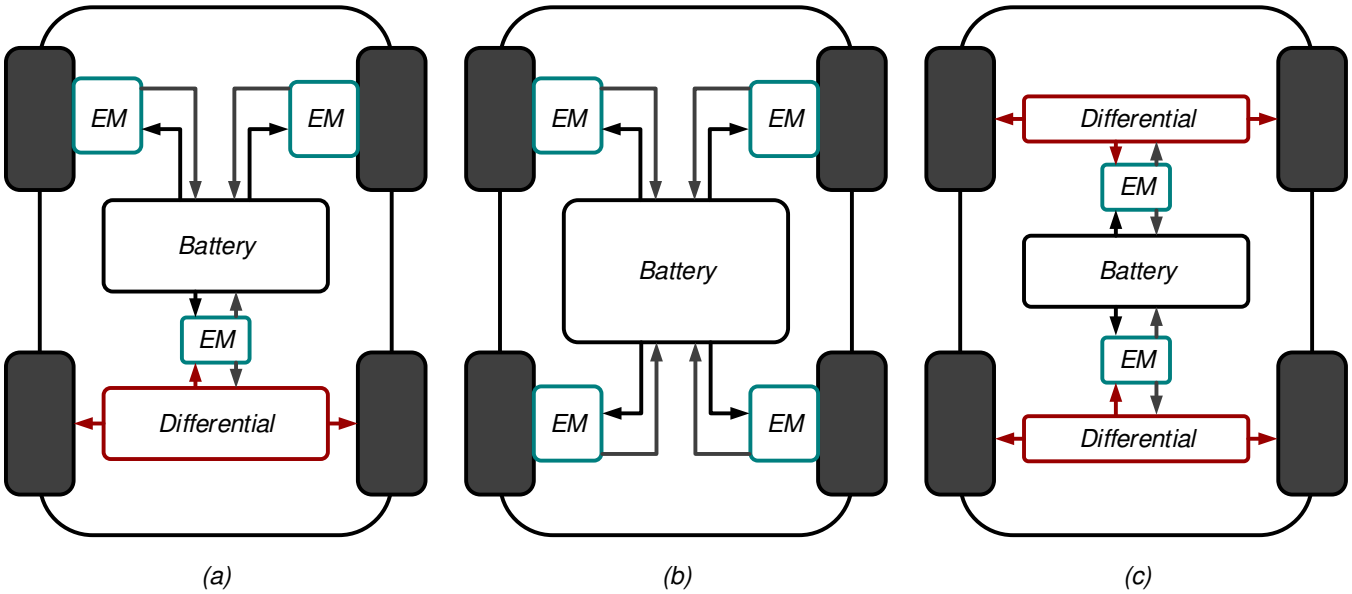

Figure 2. EV Architectures

The key blocks of an EV powertrain system are the electric motor, the traction inverter drive, the DC/DC converter, the Li-ion battery, the AC/DC grid-tied on-board charger (OBC), and controllers (MCU and PMIC), as shown in Figure 3. The traction inverter system, highlighted in red, is described in detail in the following sections. This system alone incorporates many of the protection and monitoring features utilized to achieve high safety levels.

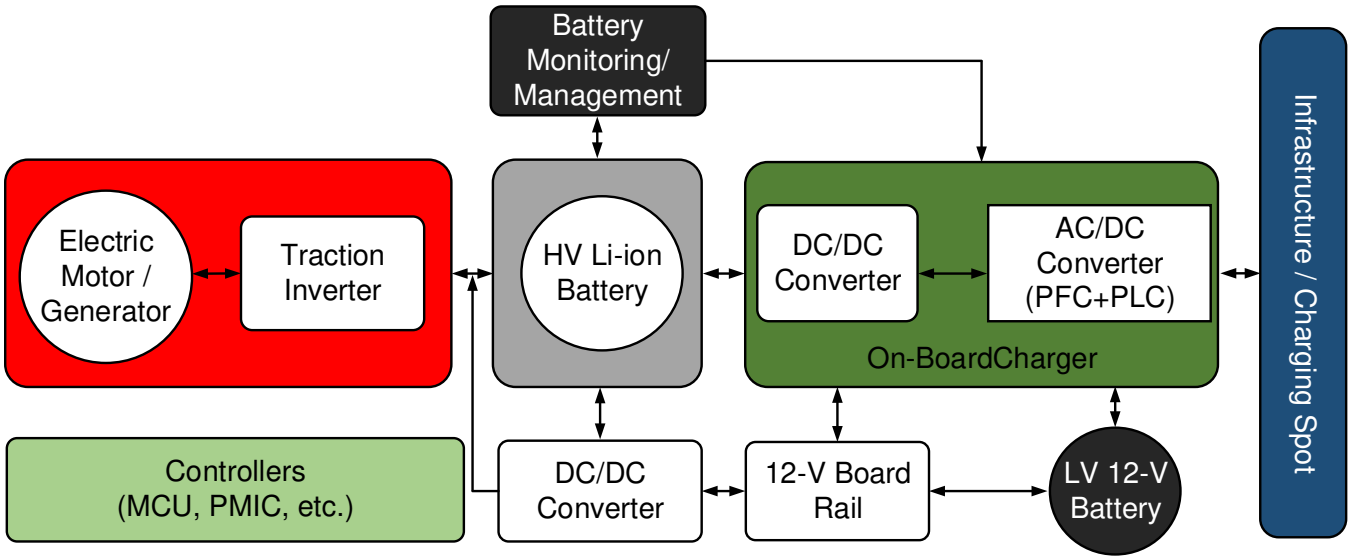

Figure 3. Blocks within an EV System

2.2 HEV/EV Traction Inverter System Architecture

Zooming in to the traction inverter system reveals multiple blocks including the power management IC (PMIC) and the microcontroller (MCU), the high-power IGBT or SiC MOSFET power modules and their temperature sensing elements, the high-voltage (HV) battery, the DC-link capacitor, sensing blocks, various protection and monitoring circuits and signal isolation, shown in Figure 4. The high-power switches are the most critical component in the inverter as they control the flow of current to the motor to generate motion. As such, the switches' are monitored and protected by sensing their temperature, voltage and current throughout their operation. The switches are controlled via the MCU and isolated gate drivers for the high side (HS) and low side (LS) of the inverter leg. The PWM signals are commonly generated using the space vector modulation (SVM) scheme. As the motor operates, the voltage, current and position signals are sensed and fed back to the controller to modify the modulation of the inverter. One such feedback method is field oriented control (FOC), which uses two phases of current and the position to generate the proper vector of modulation. A good modulation scheme, fast feedback and accurately sensed signals are required for efficient motoring.

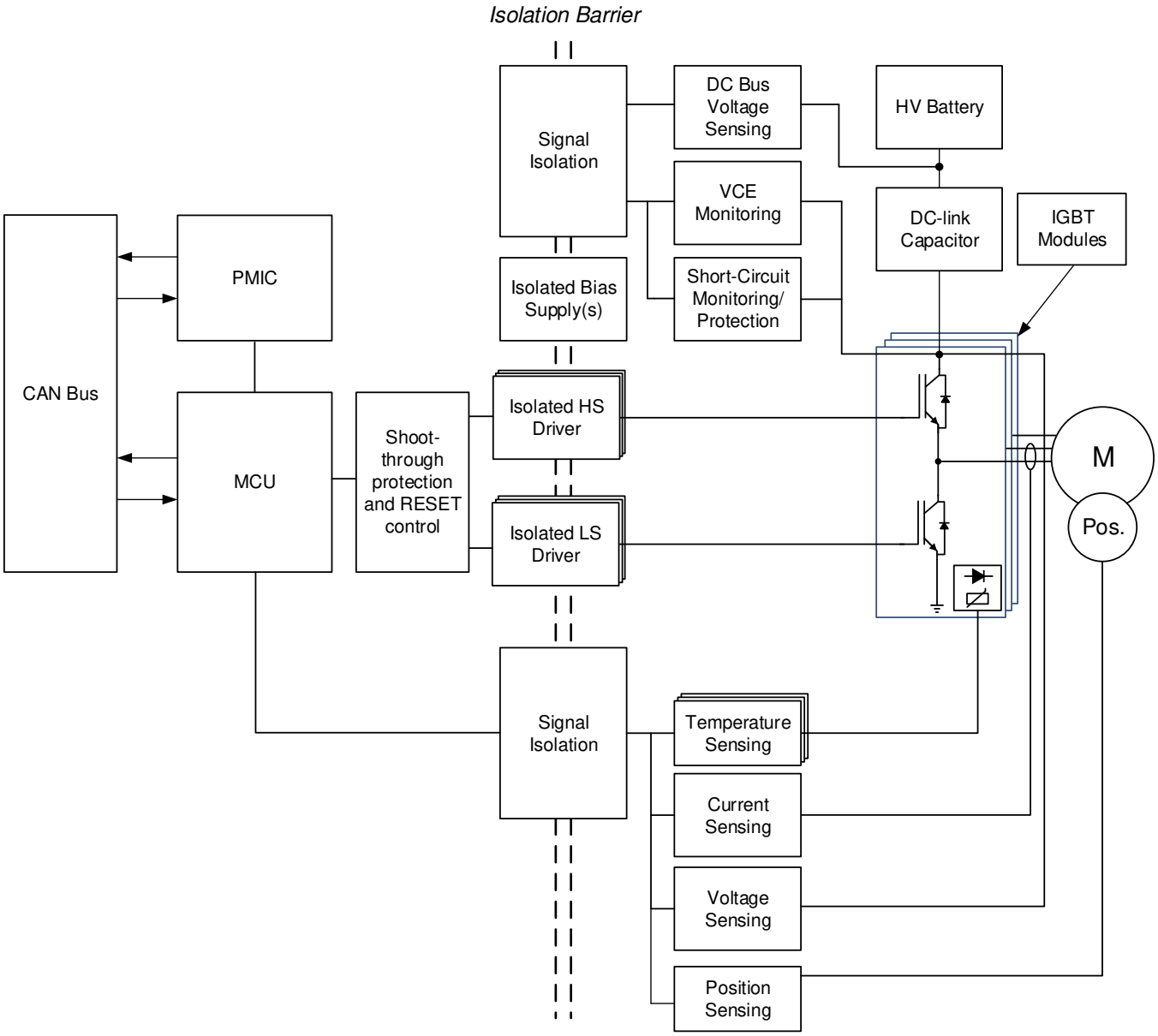

Figure 4. High-Voltage Traction Inverter Block Diagram

A closer look at the inverter, shown in Figure 5, reveals six total semiconductor power switching devices with a gate driver to amplify the PWM signal from the MCU. The three legs of the inverter convert the DC battery voltage into three phases of AC voltage and current to drive the motor. Two current measurements and a position measurement are fed back to the MCU for FOC which utilizes mathematical transformations to generate the proper signals for the six switches to control the output voltages at phases A, B and C.

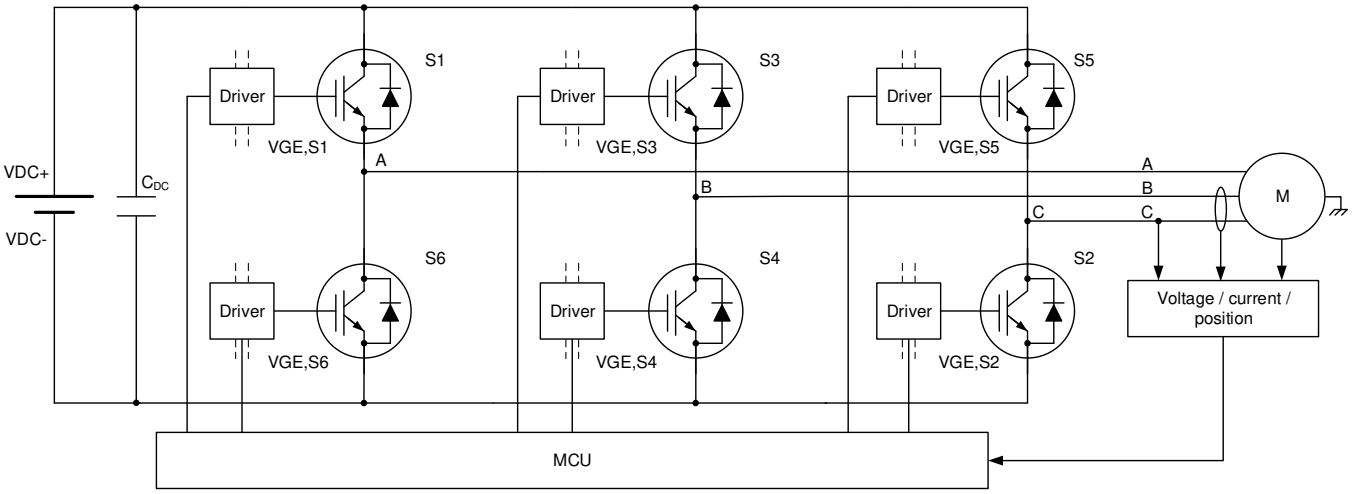

Figure 5. Three-Phase Two-Level Inverter Using IGBTs

In vector modulation, eight total states are available where two are zero vectors and the rest are active vectors used to apply the necessary voltage to the motor to generate the proper amount of torque. Table 1 shows the states where switch pairs S1 and S6, S3 and S4, and S5 and S2 are complementary to one another.

Table 1. Space Vector Modulation States

Vector	S1	S2	S3	S4	S5	S6	VAB	VBC	VCA	Vector Mode
{000}	OFF	ON	OFF	ON	OFF	ON	0	0	0	Zero
{100}	ON	ON	OFF	ON	OFF	OFF	+VDC	0	-VDC	Active
{100}	ON	ON	ON	OFF	OFF	OFF	0	+VDC	-VDC	Active
{010}	OFF	ON	ON	OFF	OFF	ON	-VDC	+VDC	0	Active
{011}	OFF	OFF	ON	OFF	ON	ON	-VDC	0	+VDC	Active
{001}	OFF	OFF	OFF	ON	ON	ON	0	-VDC	+VDC	Active
{101}	ON	OFF	OFF	ON	ON	OFF	+VDC	-VDC	0	Active
{111}	ON	OFF	ON	OFF	ON	OFF	0	0	0	Zero

There are various methods of implementing SVM. Tradeoffs between the SVM methods include reduction of switching losses, bus voltage maximum utilization, reduced harmonic content, while still achieving precise control. One such method is seven segment SVM, which is beneficial to produce a voltage waveform with low harmonics, and thus less distortion when driving the motor. The gating sequence is shown in Figure 6. A single skipped or extra gate signal as a result of an MCU control error or gate driver latched output as a result of a failure could result in inverter output distortion. Overlap of complementary switches in a phase leg could result in shoot through, and must always be avoided. As shown, the commutation of the motor is dependent on very specific gating sequences. Thus, it would be very difficult to unintentionally commutate the motor with a one-off gate driver failure.

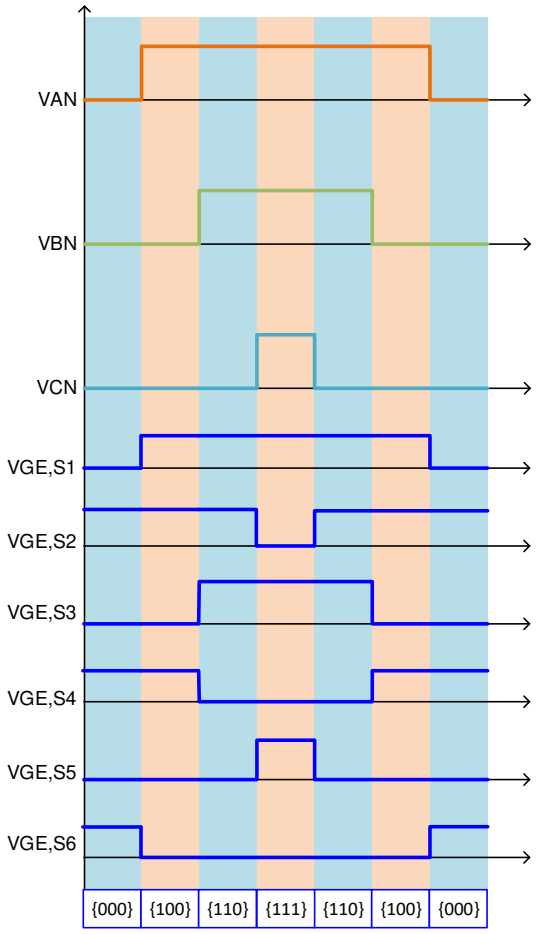

Figure 6. Seven Segment SVM

Aside from an effective gating sequence as generated by the MCU, a smart drive system includes gate drivers with protection and monitoring capabilities to protect the power switch. The following sections discuss the traction inverter system impact due to various failures within the system and how the gate drive and surrounding circuits are used to enhance the reliability of the system.

2.3 HEV/EV Traction Inverter System Performance Impact

The high-voltage traction inverter system is critical to the overall operation and safety of the vehicle. The failure modes must all be considered throughout its design and implementation. Some mechanical or electronics failures that can impact the motor's performance related to the inverter system are shown in Table 2. Those causes such as a motor short or open due to mechanical failure will not be discussed in this application note. Those failures that occur from the vantage point of the power electronics' will be discussed in more detail and the prevention mechanisms are discussed in this section.

Table 2. Traction Inverter System Event Examples

TRACTION INVERTER SYSTEM IMPACT	MECHANICAL CAUSE	ELECTRONICS CAUSE	PREVENTION MECHANISM
Under torque	Coil short or open	IGBT short or open	IGBT protection
		Gate driver damaged	Self-test and diagnostics
		Gate driver output latched	
		Gate driver incorrect logic	
		Isolation Failure	
		MCU failure	MCU watchdog
		PMIC failure	PMIC monitor
		Sensor failure	Redundant sensing
Over torque	N/A	MCU failure	MCU watchdog
		Sensor failure	Redundant sensing
Unintended motor commutation	N/A	MCU failure	MCU watchdog
Unintended motor shutdown / no output	Coil short or open	IGBT short or open	IGBT protection
		DC bus failure	Voltage monitor
		MCU failure	MCU watchdog
		PMIC failure	PMIC monitor

The voltage applied to the three windings of the motor, as previously discussed, determine the speed and torque of the motor. Disturbances can occur due to a variety of events. The power switching devices in the inverter, referred to as the IGBTs from this point on, may become shorted or open due to a mechanical failure, over-heating, etc. The gate driver itself could be a source for failure if it is damaged due to over-temperature or mechanical reasons, has a latched output, receives an incorrect signal from the MCU, or has experienced isolation barrier failure. To cover a variety of potential failures, the gate driver and auxiliary circuits are used to monitor the power switch for short circuit, proper gate voltage and other signals to protect the IGBTs and gate drivers. Additionally, circuitry is included to perform self-tests on critical functions in the case of a latent failure which occurs after a cycle of operation. Aside from the gate driver circuits, the MCU or PMIC should also have redundant monitoring circuits to prevent controller failure or supply failure.

The following section introduces the UCC217xx gate driver family and how it can be implemented in the design of the traction inverter system using its integrated protection and diagnostic functions. The external circuits used to perform self-tests and diagnostics are also described.

3 Design of HEV/EV Traction Inverter Drive Stage

This section will discuss how to design the HEV/EV traction inverter system using UCC217xx devices to provide the protection and diagnostics necessary for reliable operation.

3.1 Introduction to UCC217xx-Q1

The UCC21732-Q1 is a galvanic isolated single channel gate drivers designed for up to 1700V SiC MOSFETs and IGBTs with advanced protection features, best-in-class dynamic performance and robustness. UCC21732-Q1 has up to ±10-A peak source and sink current. The input side is isolated from the output side with SiO2 capacitive isolation technology, supporting up to 1.5-kVRMS working voltage, 12.8-kVPK surge immunity with longer than 40 years Isolation barrier life, as well as providing low part-to-part skew, and >150V/ns common mode noise immunity (CMTI). The UCC217xx-Q1 family of devices include the state-of-art protection features, such as fast overcurrent and short circuit detection, shunt

current sensing support, fault reporting, active miller clamp, input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness. The isolated analog to PWM sensor can be utilized for easier temperature or voltage sensing, further increasing the drivers' versatility and simplifying the system design effort, size and cost. The benefits of these circuits are given below, along with auxiliary circuitry to enhance system-level reliability.

3.2 Designing a Traction Inverter Drive System Using UCC217xx-Q1

The UCC21732-Q1 is shown in Figure 7 along with the various monitoring and protection blocks required in the inverter system. Four categories are used to describe the various blocks: Self-Test, Diagnostics, Protection and Driver Function. Self-Test blocks signify the circuits used to ensure another critical block is functioning properly. The Diagnostic blocks are used to feed back critical information to the MCU to determine monitor the power stage performance and/or behavior. The Protection blocks are used to prevent IGBT failure. Finally the Driver Function blocks include the basic gate driver function.

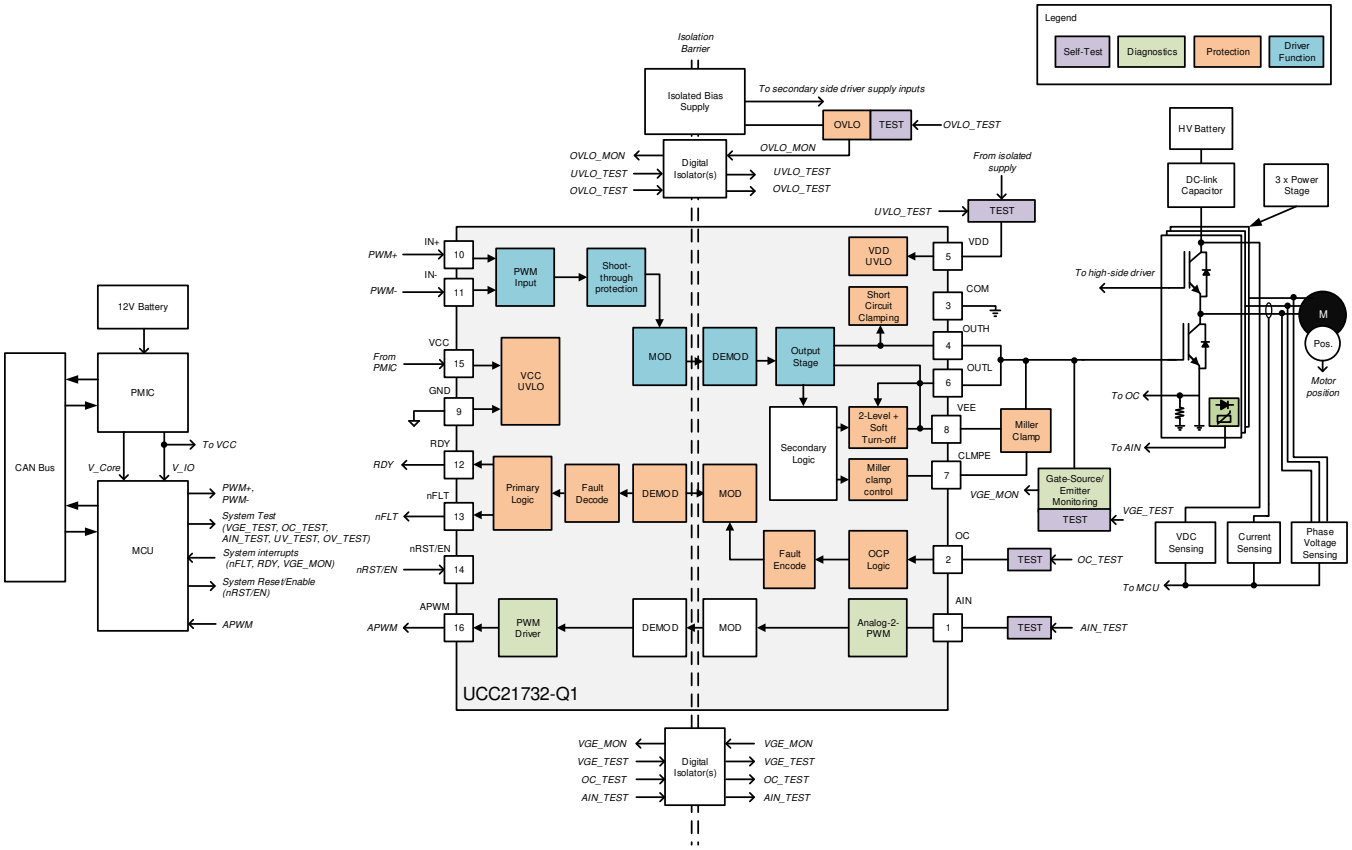

Figure 7. Block Diagram of a Traction Inverter System with UCC217xx-Q1

3.3 Description of Protection Features

This section describes the UCC217xx-Q1 integrated protection and diagnostic features and non-integrated features that are beneficial for reliable traction inverter system operation.

3.4 Protection Features of UCC217xx-Q1

The system impact of various failures are shown as given in Table 2 may be prevented using integrated and auxiliary circuits around the gate driver. Table 3 shows these system impacts and potential failures along with the integrated and auxiliary circuits of the gate driver circuitry that can be used to prevent them.

The potential failure location(s) within the system block are as shown in Figure 8, classified as (F1) PMIC failure, (F2) MCU failure, (F3) Driver failure, or (F4) Motor/Mechanical failure.

Table 3. Protection and Diagnostic Features Using UCC217xx-Q1

System impact	Associated driver and/or inverter failures	Potential failure location(s)	UCC217xx-Q1 integrated features	External circuit features
Torque disturbance	Over or under voltage of driver power supply	F1	UVLO + interrupt signal	OVLO + interrupt signal
Unintended commutation	Gate driver pulse width skew	F2 or F3	Low-delay capacitive isolation barrier and proven process	N/A
Unintended motor shutdown / Torque disturbance	Power switch short circuit	F2 or F4	DESAT/OC detection and interrupt	DESAT (UCC21750) or OC (UCC21732/10) self-test UVLO/OVLO self-test
Unintended motor shutdown / Torque disturbance	Gate shorted to ground or VDD	F2 or F3	N/A	VGE monitoring and compare to PWM with interrupt
Unintended motor shutdown	Power switch shoot-through due to false gate signal or dv/dt-induced current	F2	Anti-shoot-through logic and Miller clamp (internal or external	N/A
Torque disturbance	Power switch over-voltage	F2	Two-level turn-off and/or soft turn-off	VCE/VDS monitoring
Torque disturbance	Power switch over-temperature	F1, F2, or F4	Integrated isolated sensing with integrated bias current	N/A
Torque disturbance	Power switch gate oxide breakdown	F2 or F4	Short circuit clamping to VDD	N/A
Torque disturbance	Power switch false turn-on when input power is floating	F1 or F2	Active pulldown	N/A
Torque disturbance / Unintended motor shutdown	Power system DC bus over/under voltage	F1 or F4	Integrated isolated sensing	N/A

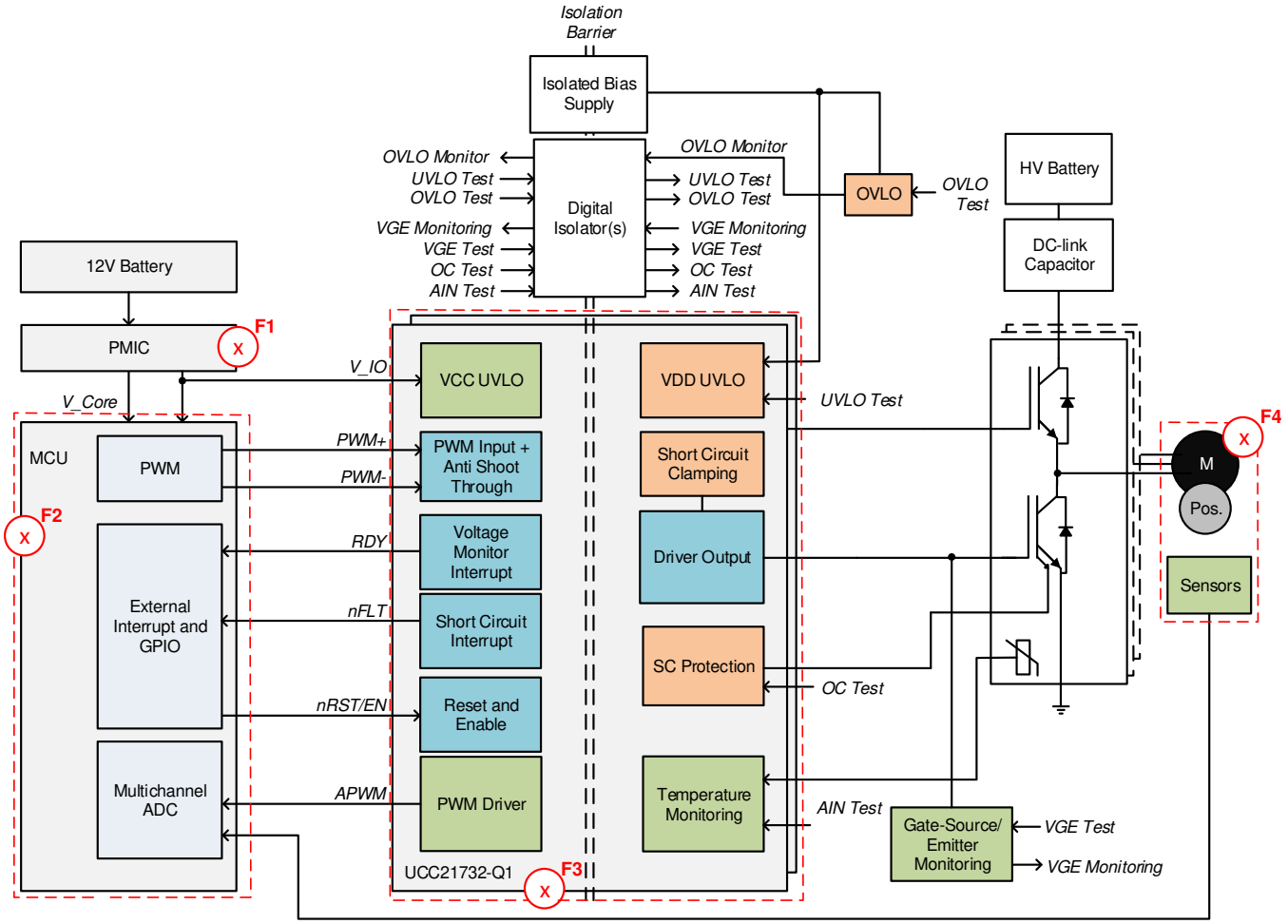

Figure 8. Possible Traction Inverter System-Level Failures and Prevention Circuits Using UCC21732-Q1

3.5 UCC217xx-Q1 Protection and Monitoring Features Descriptions

This section describes the implementation of monitoring and protection circuits using UCC217xx-Q1.

3.5.1 Primary and Secondary Side UVLO and OVLO

Under and over-voltage lockout (UVLO and OVLO) are used to protect the driver IC as well as monitor the voltage used to drive the power switch on the secondary side. UVLO is integrated into UCC217xx-Q1 for both the primary and secondary side supplies, VCC and VDD respectively. These are used to protect the system in case of bias supply failures. The output is pulled low if VCC or VDD drops below the UVLO threshold. Additionally, if there is a UVLO fault, the RDY pin will go HIGH. For VCC the threshold is 2.7 V with a 0.2 V band of hysteresis. The VDD UVLO threshold is 12 V, referenced to COM, with 0.8 V hysteresis. Aside from bias failures, the VDD-side UVLO is beneficial to protect the power switch. Based on the I-V characteristics of high-power IGBTs and SiC MOSFETs, if the device is driven at 12 V the conduction losses are smaller and early saturation of the device can be prevented. In this way, UVLO can be useful to prevent damaging the FET due to a drop in supply voltage.

Overvoltage lockout (OVLO) is also implemented to protect the power switch from being driven with too high of a voltage, outside of the device ratings, which could cause gate oxide breakdown or reduced lifetime. The driver IC should not be supplied with a voltage beyond the maximum ratings, as it may result in driver failure and uncertain driver output state. OLVO is implemented using external circuitry to protect the driver and power device from bias supply failure on the secondary side supply, VDD. VDD is divided down and compared to a fixed voltage reference generated by a Zener diode. When the divided voltage drops below the Zener voltage, the comparator output will switch and will be sent across the isolation barrier to the MCU.

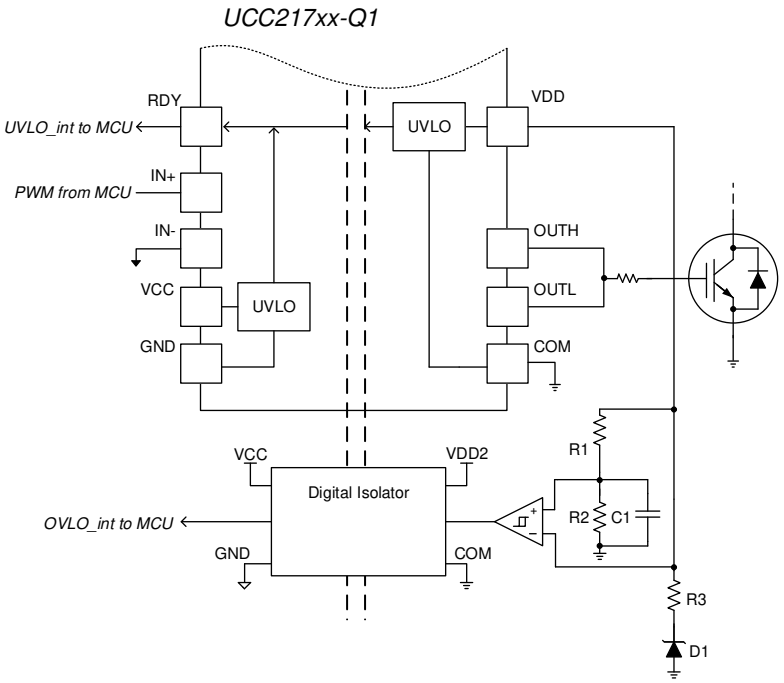

Figure 9. Integrated UVLO and External OVLO Implementation

3.5.2 Over-Current (OC) and Desaturation (DESAT) Detection

Overcurrent (OC) protection (UCC21732-Q1 and UCC21710-Q1) and desaturation (DESAT) protection (UCC21750-Q1) are used to prevent a short-circuit event from destroying the power devices. Both OC and DESAT protection are available with UCC217xx variants and are integrated internally, with a few external components based on the application. The OC and DESAT protection ST (self-test) circuits may be implemented externally and are shown below.

Integrated OC protection is shown in Figure 10. In this example, the IGBT's current is stepped down with an integrated current mirror and is output at the split emitter. The current is then measured via a shunt resistor, R_{Shunt}. The OC pin monitors the current via the voltage across R_{Shunt} and triggers the OC fault when the voltage surpasses the internal threshold of 0.7 V. At this time, the driver will initiate soft turn-off and/or 2-level turn-off to safely shut down the power device.

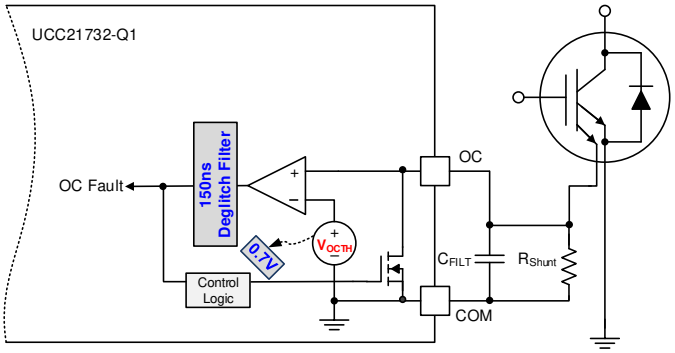

Figure 10. Overcurrent and Short Circuit Protection (UCC21732-Q1 and UCC21710-Q1)

Desaturation detection, or DESAT is a method most commonly used with IGBTs because of their well-defined knee point in the I-V curve at which the device moves from the linear to the active region as a short circuit occurs. The DESAT pin utilizes this information by monitoring the voltage across the IGBT when it is turned on. The DESAT pin is connected to the collector of the IGBT through a series resistor and HV diode, D_{HV}. D_{HV} becomes forward biased when the voltage at the IGBT increases beyond the DESAT threshold voltage of 9 V. R_{DESAT} limits the current flowing to the DESAT pin. The timing is controlled by C_{BLK}, which charges up to the threshold voltage when the driver turns on. The DESAT threshold voltage can be adjusted manually with the addition of more D_{HV} diodes in series or by adding a Zener diode in series.

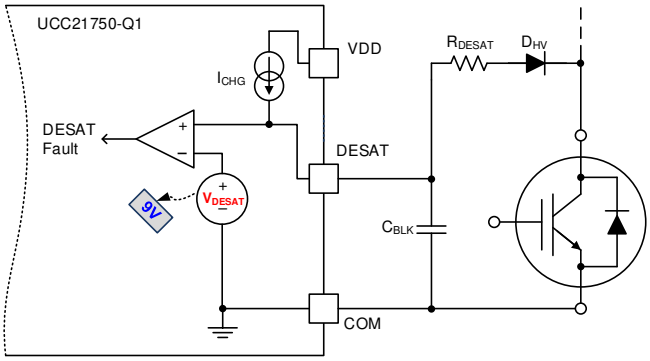

Figure 11. DESAT Protection (UCC21750)

The self-test circuit for the OC or DESAT detection is performed via external circuitry controlled by the MCU through a digital isolator, shown in Figure 12. A digital isolator is used to drive the gate of a NMOS FET to enable a fault at the DESAT/OC pin. The NMOS FET is turned on and causes the upper PMOS FET to become turned on, which allows current sourced from VDD to increase the voltage at the pin to beyond the threshold voltage. At this point, the nFLT will trigger. The input, IN+, must be high during this self-test for nFLT to trigger. If nFLT is triggered, then the short circuit detection is working properly.

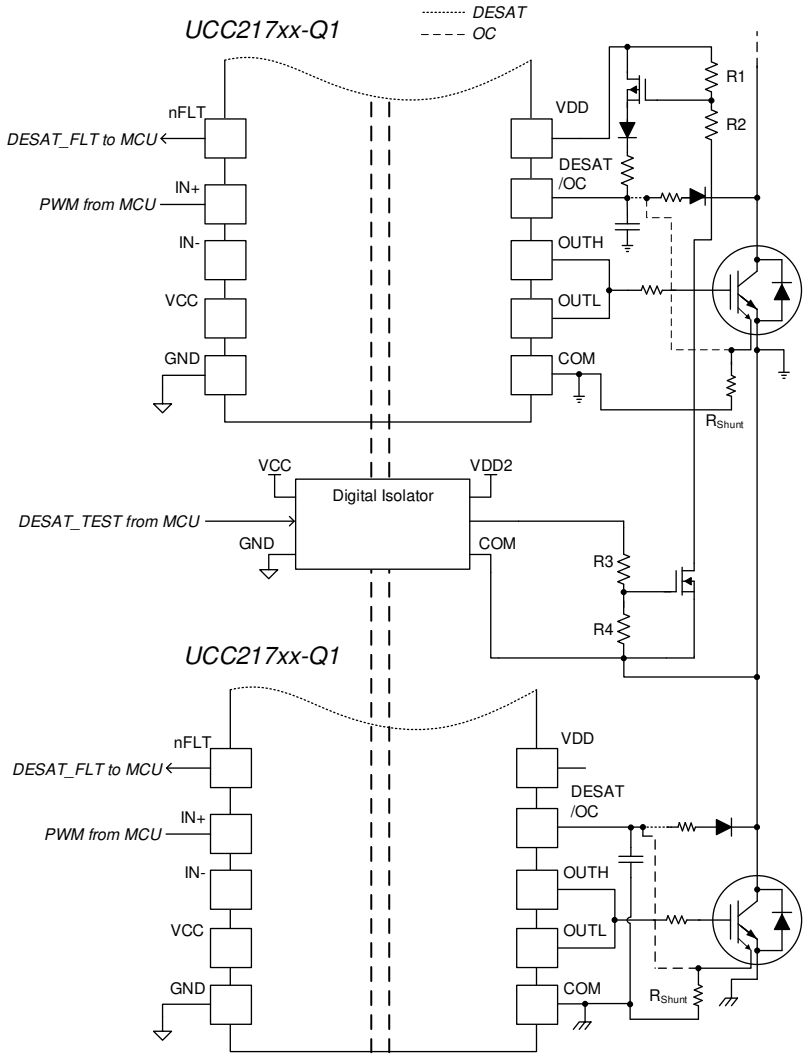

Figure 12. DESAT/OC Detection Self-Test Circuit

3.5.3 2-Level and Soft Turn-Off

As mentioned in the previous section, short circuit detection sends back a fault indication and triggers the driver to turn off the IGBT or SiC MOSFET. The driver initiates either 2-level turn-off or soft turn-off to safely shut down the IGBT or MOSFET, preventing large voltage overshoot across the device as a result of the high current transient.

2-level turn-off, shown in Figure 13, slows down the turn-off transient by pulling the gate to a mid-level voltage, 9 V, during the turn-off transition to reduce the channel current flow through the device. This significantly reduces the energy dissipation during the fault event. After the second voltage level is applied for a period of time, the driver finally pulls the gate down to VEE using a soft pull down current to transition smoothly to the off-state.

Soft turn-off, shown in Figure 14, uses a soft pull down current throughout the entire turn-off transition as opposed to applying a specified gate voltage. The 400 mA current causes the device to transition at a slower rate than it would with a hard turn-off, and thus reduces voltage overshoot while minimizing the amount of energy dissipation.

The inverter benefits not only to prevent the damage or destruction of the power switches, but also prevents high-voltages from being applied to the motor windings, which can also reduce the lifetime of the motor itself.

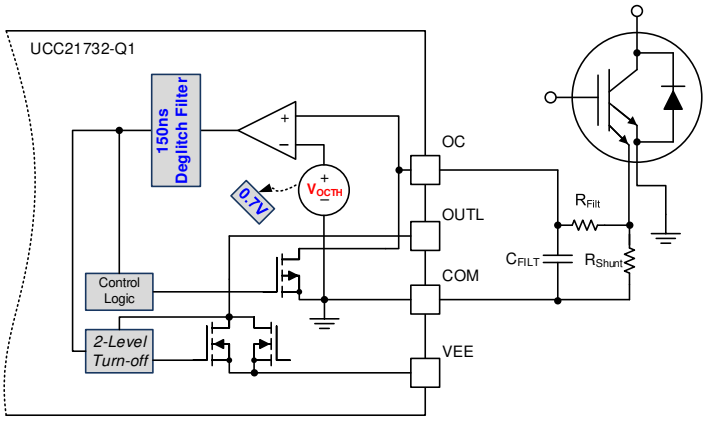

Figure 13. 2-Level Turn-Off Block (UCC21732-Q1)

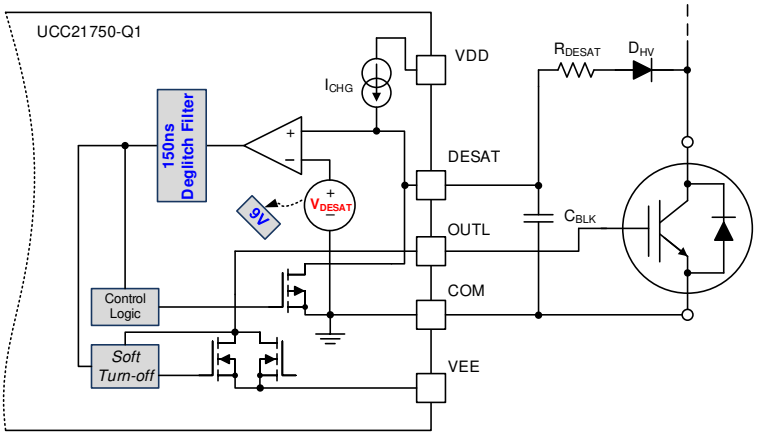

Figure 14. Soft Turn-Off Block (UCC21750-Q1, UCC21710-Q1)

3.5.4 Power Switch Gate Voltage (VGE/VGS) Monitoring

Gate voltage monitoring, as shown in , Figure 15 is used to ensure that the gate voltage is reaching the VDD level when IN+ is pulled high. This is important to ensure the device is being driven efficiently to reduce switching loss and is held on at the proper voltage level to reduce conduction loss. The gate voltage is compared to VDD, with a small voltage divider to account for the gate voltage drop due to the gate resistance, $R_{G,tot}$. The comparator's output is sent back to the MCU using a digital isolator. In case of a fault, the secondary bias supply should also be checked. This function may also be used to monitor V_{GE} when DESAT or OC detection has been detected to ensure proper turn off when the gate is pulled low by the driver.

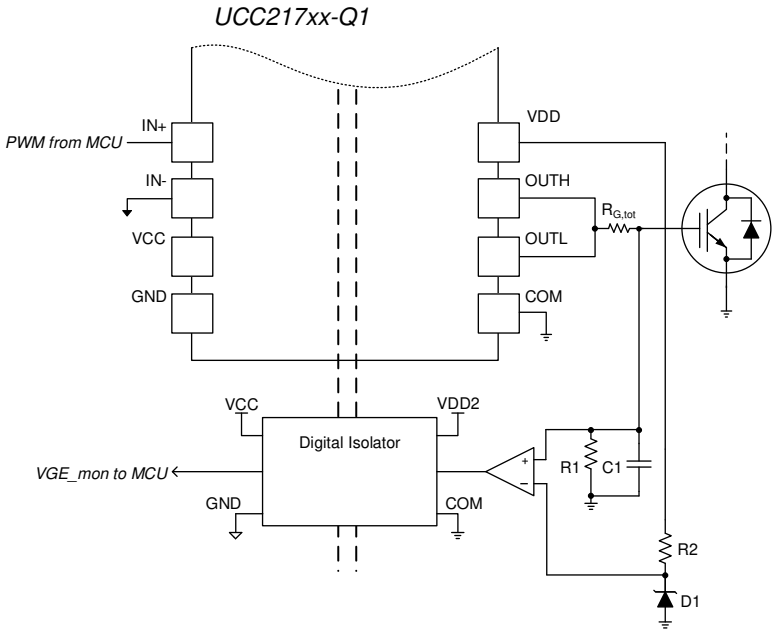

Figure 15. V_{GE} Monitoring Circuit

3.5.5 Power Switch Anti-Shoot-Through

Anti-shoot through circuitry is integrated in UCC217xx to prevent IN+ and IN- from overlapping. This allows for two single-channel drivers to be interlocked, as shown in Figure 16, where IN+ of the upper device is tied to IN- of the lower device, and vise versa. This prevents the upper and lower switches from conducting at the same time, which would result in a short circuit and device over-heating.

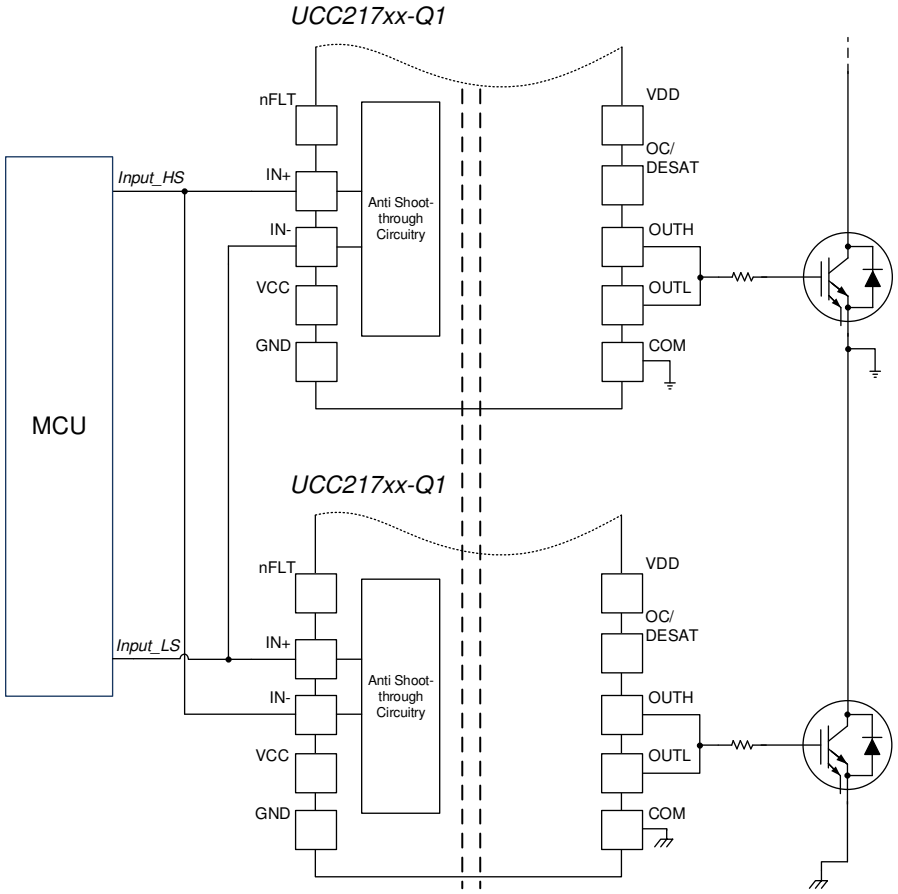

Figure 16. Integrated Anti-Shoot-Through and Interlock Circuit

3.5.6 Integrated Internal or External Miller Clamp

The Miller clamp may be either external or internal depending on the UCC217xx variant. UCC21732-Q1 is shown in Figure 17 with an external Miller clamp driven by the CLMPE pin. When OUTL goes below 2 V, the clamp is turned on to re-direct any current generated by the Miller capacitor, C_{GC}, during a high *dv/dt* transient ensuring that the device remains off during the off-state.

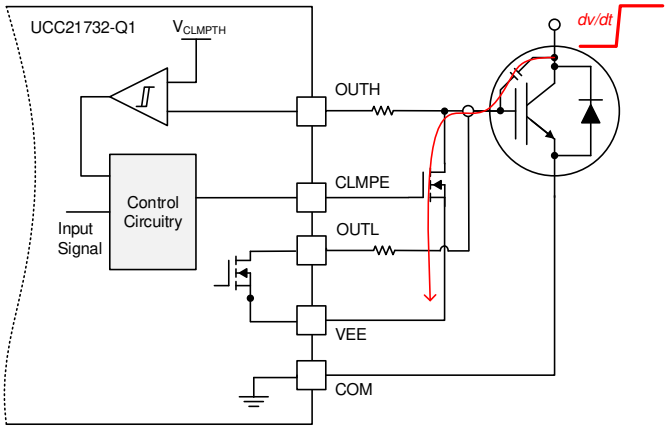

Figure 17. External Active Miller Clamp

3.5.7 Isolated Analog-to-PWM Channel

UCC217xx-Q1's integrated isolated analog-to-PWM channel can be used to monitor any voltage within the range of the AIN to COM pin including the dc bus voltage and phase current. The AIN pin also integrates a current source to bias a temperature sensor, which can be used in conjunction with the internal temperature sensor of the power switch module. Figure 18 shows the internal circuit and external connection for monitoring the IGBT module temperature. Temperature is important to determine the module's health and lifetime and monitor for misoperation.

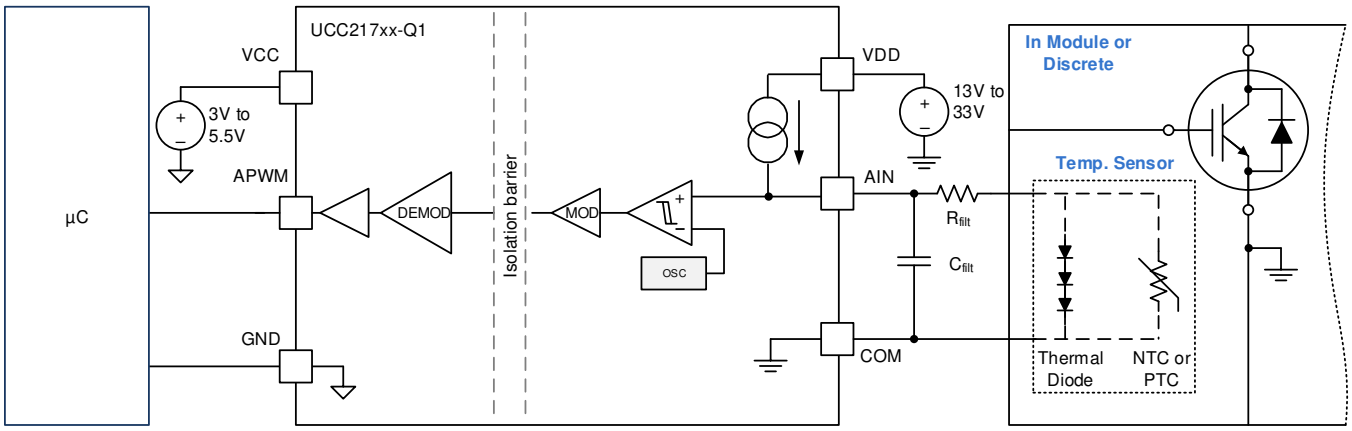

Figure 18. Isolated Analog-to-PWM Signal Block

3.5.8 Short-Circuit Clamping

During a short circuit event, the Miller capacitance, from gate to drain/collector, can source current to the OUTH/OUTL pin due to high dv/dt and may boost the OUTH/OUTL voltage. The clamping feature clamps the OUTH/OUTL pin voltage to slightly higher than VDD to prevent over-voltage at the gate and potential breakdown. The internal diodes from OUTH/OUTL to VDD perform this function as shown in Figure 19.

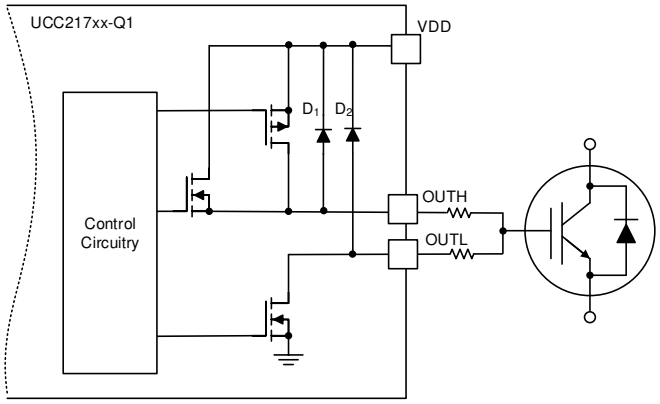

Figure 19. Short Circuit Clamping Block

3.5.9 Active Pulldown

Active pulldown ensures that OUTH/OUTL is clamped to VEE while VDD is not connected. The OUTH/OUTL pin is high-impedance when VDD is open and the pulldown feature prevents false turn on while the device supply is open. This is implemented as shown in Figure 20.

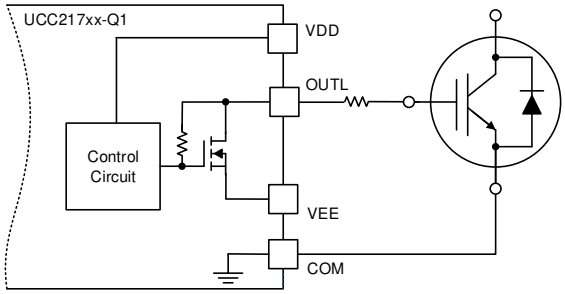

Figure 20. Active Pulldown Block

4 Isolated Bias Supply Architecture

Another important consideration in automotive traction inverter systems with regards to the gate drivers is the bias supply architecture. The bias supplies are used to provide isolated power used to drive each IGBT or SiC MOSFET. The reliability of the single or multiple isolated supplies is necessary to keep the inverter operational. The architectures of the gate driver bias supplies varies based on the required level of reliability. The bias supplies may be shared amongst multiple drivers (centralized), provided separately to each driver (distributed), or partially shared (semi-distributed).

Centralized bias supply architecture has the advantage of low component count, low cost, and generic control. However, the transformer for this architecture may be bulky, can suffer from common mode current, can result in complex PCB routing when shared amongst six drivers and does not inherently contain any redundancy.

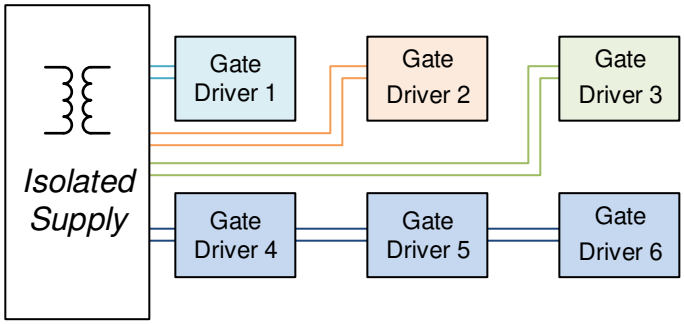

Figure 21. Centralized Bias Supply Architecture

The semi-distributed power consists of several transformers to generate the biases for various groups of drivers. For example, each high-side driver may be supplied with a separate transformer whereas all the low-side drivers may be shared. The advantage of this architecture is the simplicity of transformer construction and PCB layout, the ability to have higher power quality for each bias supply, the distribution of weight of the supplies' transformers, and the simplicity of control. The disadvantages include higher component count, higher cost, and still a lack of redundancy.

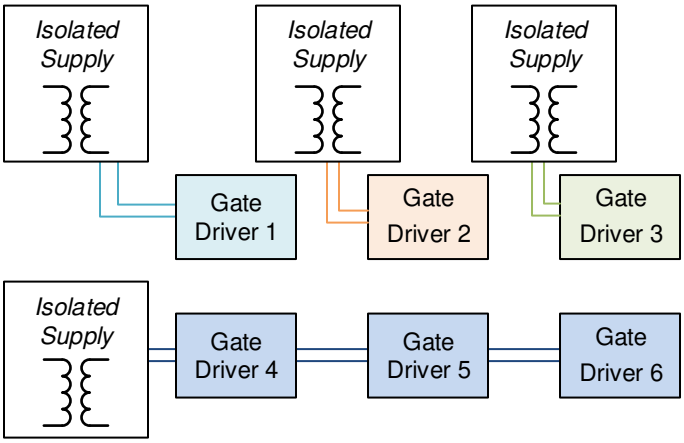

Figure 22. Semi-Distributed Bias Supply Architecture

Finally, the distributed power architecture provides a separate bias supply for each gate driver. Although it requires more components, resulting in higher cost, the advantages include a high level of redundancy, simplified layout and distribution of weight and better power quality.

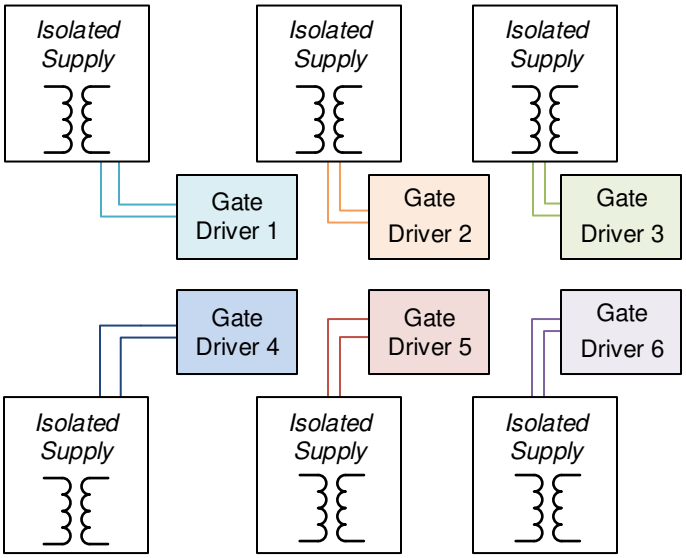

Figure 23. Distributed Bias Supply Architecture

For more information on bias supplies, please see TI's portfolio of high-voltage controllers and this reference design on bias supplies for HEV/EV traction inverters.

5 Summary

The complexity of electronics in electrified vehicles is ever-increasing with enhanced performance and safety regulations. The traction inverter contains some of the most critical components of the electric vehicle which have a direct impact on the drive of the motor. Integrated protection and monitoring features of UCC217xx-Q1 drivers are shown to enable simplification of the system, as well as enhanced performance.

For more information, please see the product folders of UCC21732-Q1,UCC21750-Q1, and UCC21710-Q1 containing design help and technical documentation and visit the Power Management E2E Forum to get answers to your questions.

6 References

1. HEV/EV traction inverter power stage with 3 types of IGBT/SiC bias-supply solutions reference design
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6. S. Jain and L. Kumar, "Fundamentals of Power Electronics Controlled Electric Propulsion," in *Power Electronics Handbook*, M. H. Rashid, Ed. United Kingdom: Butterworth-Heinemann, 2018, pp. 1023-1065.

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