Migrating to UCC25640x from UCC25630x

ABSTRACT

The UCC25640x LLC controller family is tailored for applications requiring low standby power as well as low audible noise and is pin to pin compatible with UCC25630x. This application report walks through key differences between the UCC25640x and UCC25630x LLC controller families.

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1 Introduction

The purpose of this document is to explain the differences between the UCC25640x and UCC25630x LLC controller families. It also demonstrates how to migrate UCC256404 to an existing design. The naming convention of the UCC25640x matches that of the UCC25630x. The new part ending in UCC256403 is similar in feature set to UCC256303 as shown in Table 1. The same is true for the new UCC256404 and existing UCC256304 devices.

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>HIGH VOLTAGE STARTUP</th>
<th>X-CAPACITOR DISCHARGE</th>
<th>REQUIRES EXTERNAL AUXILIARY POWER</th>
</tr>
</thead>
<tbody>
<tr>
<td>UCC256303</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>UCC256403</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>UCC256304</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>UCC256404</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

2 Burst Pattern

In order to satisfy standards such as CoC Tier 2 and DOE Level VI, good light load efficiency is needed. This is especially challenging for LLC converters which require a minimum amount of circulating resonant current in order to maintain regulation of its output voltage. The UCC25630x and UCC25640x address this with the inclusion of a burst mode function to reduce standby power and improve light load efficiency. While this enables LLC designs to greatly improve standby power performance, this can lead to audible noise in some designs, depending on the transformer construction. The UCC25640x addresses this by using a burst pattern tailored to minimize audible noise where transformer current is slowly increased at the beginning of a burst packet and slowly decreased at the end of a burst packet. This burst algorithm avoids sharp changes in the LLC transformer current which can lead to mechanical oscillation of the transformer and result in transformer “humming”.

In addition, the UCC25640x has a larger minimum number of switching cycles within a burst packet than UCC25630x. This allows for a much lower burst packet frequency at standby to further avoid the audible switching frequency range.

<table>
<thead>
<tr>
<th></th>
<th>UCC25630x</th>
<th>UCC25640x</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum number of switching cycles per burst packet</td>
<td>15</td>
<td>40</td>
</tr>
</tbody>
</table>
3 Improved Adaptive Dead Time Control

The UCC25640x and UCC25630x use adaptive dead time control where the switch node is monitored to detect when the switch node is done “slewing” to either $V_{\text{IN}}$ or ground before turning on the next MOSFET.

![Figure 2. Adaptive Dead Time Control](image)

While the UCC25630x is capable of detecting switch node slew rates as low as 1 V/ns, the UCC25640x is capable of detecting switch node slew rates down to 0.1 V/ns. A more sensitive slew rate detector provides numerous benefits. More capacitance on the switch node can be tolerated with a more sensitive slew rate detector, meaning MOSFETs with larger $C_{\text{oss}}$ can be used or larger switch node snubber capacitance can be used to meet EMI requirements. The slew rate detector is only used to determine the dead time between high side off – low side on. The UCC25640x includes a dead time copy feature to match the dead time between low side off – high side on and high side off – low side on. This feature ensures proper switching behavior and reliability.
4 Startup Configurability

The UCC25630x designs rely on the capacitance of the VCR pin to set the switching frequency profile during soft start. In addition, the initial soft start voltage in the UCC25630x is fixed at 0 V. For certain VCR configurations, this can lead to an initial switching frequency that is quite high. The UCC25640x adds the ability to program an initial voltage onto the soft start pin to shift the initial switching frequency lower. 5 V is initially buffered onto the LL/SS pin to determine the programmed initial LL/SS voltage which is configured through external resistance on the pin. The desired precharge voltage is then buffered onto the LL/SS pin for soft start. This configurability allows the designer a second degree of freedom to limit the maximum switching frequency during startup to ensure zero voltage switching.

Unlike the UCC25630x, the BLK pin voltage is not buffered onto the LL/SS pin. Instead, a static 3.5 V is buffered onto the LL/SS pin for burst mode programming of the BMT\_H threshold.

5 FB Pin Clamp

At very light loads, the opto-coupler may draw large current causing opto-coupler saturation. Once the opto-coupler is saturated, there is a delay to bring the opto out of saturation which may lead to poor transient performance. For the UCC25630x, a resistor and Zener are typically added between RVCC and the FB pin to avoid opto-coupler saturation by sourcing more current to the opto-coupler when the FB pin voltage reduces. For the UCC25640x, if the opto-coupler demands greater than I\_FB, a secondary current source is enabled to supply more current to the opto and avoid saturation. This integrated clamp makes the external resistor and Zener unnecessary for most designs.

6 RVCC Voltage

While the RVCC voltage of the UCC25630x is 12 V, the RVCC voltage of the UCC25640x is increased to 13 V. This allows the UCC25640x controller family to power PFC controllers with slightly higher UVLO thresholds such as the UCC28180 directly from the RVCC pin.
7 Migrating from UCC25630x to UCC25640x

The UCC25630x and UCC25640x are pin-to-pin compatible and can be interchanged. This section describes how to migrate an existing design from the UCC25630x to UCC25640x.

7.1 ISNS Pin

While the OCP1 detection threshold of the UCC25630x and UCC25640x are the same, the OCP2 and OCP3 detection thresholds are reduced by 30% in UCC25640x. The greater margin between OCP1 and OCP2 and OCP3 helps to avoid overcurrent fault during full load startup.

To accommodate the change in OCP2 and OCP3 thresholds, the ISNS resistor connected between ISNS and gnd should be reduced by 30%.

<table>
<thead>
<tr>
<th></th>
<th>UCC25630x</th>
<th>UCC25640x</th>
</tr>
</thead>
<tbody>
<tr>
<td>OCP1 Detection Threshold</td>
<td>4 V</td>
<td>4 V</td>
</tr>
<tr>
<td>OCP2 Detection Threshold</td>
<td>0.84 V</td>
<td>0.6 V</td>
</tr>
<tr>
<td>OCP3 Detection Threshold</td>
<td>0.64 V</td>
<td>0.43 V</td>
</tr>
</tbody>
</table>

7.2 LL/SS Pin

For the UCC25640x, this pin is used to program two thresholds: the initial soft start voltage and the burst threshold for exit. Programming an initial voltage onto the LL/SS pin provides a second degree of freedom to limit the maximum switching frequency during startup. Both thresholds are programmed through an external resistor divider connected from RVCC to LL/SS.
The programmable range of the initial LL/SS pin voltage and the BMT_H burst threshold are the following:

\[ 0V < V_{LL/SS, initial} < 1V \]  \hspace{1cm} (1)

\[ 0.2V < V_{BMT_H} < 4V \]  \hspace{1cm} (2)

Once the desired initial LL/SS voltage and BMT_H thresholds are selected by the designer, the following equations can be used to determine appropriate upper and lower resistance for the LL/SS pin divider.

\[ R_{LL/SS, Upper} = R_{BMT} \times \frac{V_{CC} \times V_{LL/SS, initial} - V_{CC} \times V_{BMT_H, H,SW}}{V_{LL/SS, initial} \times (V_{BMT_H, H,SW}) + V_{CC} \times V_{BMT_H, H,SW} + 4 \mu A \times R_{BMT}} \]  \hspace{1cm} (3)

This equation simplifies to the following:

\[ R_{LL/SS, Upper} = 100k\Omega \times \frac{13V \times 5V - 13V \times 3.5V}{5V \times (V_{BMT_H, H,SW}) + 3.5V \times (V_{LL/SS, initial} \times (V_{BMT_H, H,SW}) + 4 \mu A \times 100k\Omega)} \]  \hspace{1cm} (4)

\[ R_{LL/SS, Lower} = R_{BMT} \times \frac{V_{CC} \times V_{LL/SS, initial} - V_{CC} \times V_{BMT_H, H,SW}}{V_{LL/SS, initial} \times (V_{BMT_H, H,SW}) + V_{CC} \times V_{BMT_H, H,SW} + 4 \mu A \times R_{BMT}} \]  \hspace{1cm} (5)

This equation simplifies to the following:

\[ R_{LL/SS, Lower} = 100k\Omega \times \frac{13V \times 5V - 13V \times 3.5V}{(13V - 5V) \times (V_{BMT_H, H,SW}) + (13V - 3.5V) \times (V_{LL/SS, initial} \times (V_{BMT_H, H,SW}) + 4 \mu A \times 100k\Omega)} \]  \hspace{1cm} (6)

Note that a UCC25640x design calculator is available to perform these calculations.

### 7.3 BW Pin

BW serves as a dual purpose pin for the UCC25640x functioning as an output overvoltage detection pin as well as programming the threshold between burst mode entry threshold and burst mode exit threshold. Figure 3 shows the timing of relevant signals used in BW programming.

The ratio between low frequency and high frequency burst is set by the equivalent resistance between the BW pin and ground. A 54 µA current source is fed to the pin and the resulting voltage programs the burst threshold ratio during the startup phase.

\[ R_{BW, th} = \frac{R_{BMT, Upper} \times R_{BMT, Lower}}{R_{BMT, Upper} + R_{BMT, Lower}} \]  \hspace{1cm} (7)

\[ V_{BW, config} = R_{BW, th} \times V_{BW, config} \]  \hspace{1cm} (8)

### Table 4. Burst Mode Threshold Configuration on the BW Pin

<table>
<thead>
<tr>
<th>BMT CONFIGURATION NAME</th>
<th>BMT LOW/HIGH RATIO</th>
<th>BW PIN EQUIVALENT RESISTANCE ((R_{BMT}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>User Option 1</td>
<td>0.95</td>
<td>&gt; 24 730 Ω</td>
</tr>
<tr>
<td>User Option 2</td>
<td>1</td>
<td>17 125 Ω – 19 976 Ω</td>
</tr>
<tr>
<td>User Option 3</td>
<td>0.9</td>
<td>12 562 Ω – 13 624 Ω</td>
</tr>
<tr>
<td>User Option 4</td>
<td>0.8</td>
<td>90 18 Ω – 9 813 Ω</td>
</tr>
<tr>
<td>User Option 5</td>
<td>0.6</td>
<td>6 478 Ω – 6 849 Ω</td>
</tr>
<tr>
<td>User Option 6</td>
<td>BMTL = Minimal</td>
<td>4 430 Ω – 4 732 Ω</td>
</tr>
<tr>
<td>User Option 7</td>
<td>Disable Burst; Ratio =1</td>
<td>2 422 Ω – 3 038 Ω</td>
</tr>
</tbody>
</table>

### 7.4 Using UCC256404 on UCC25630-1EVM-291

Despite the differences described above, the UCC25640x is pin-to-pin compatible with the UCC25630x. Any design with the old device can be modified with the new one. An example presented here shows how UCC25630-1EVM-291 is modified to work with UCC256404. The changes in Table 5 should be made to UCC25630-1EVM-291. Changes can also be seen on the modified schematic in Figure 5.

### Table 5. List of Changes on UCC25630-1EVM-291

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>ORIGINAL VALUE</th>
<th>NEW VALUE</th>
<th>REASONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>R4</td>
<td>140 kΩ</td>
<td>41.2 kΩ</td>
<td>BLK requires a different resistor divider. The recommended value is given in the design calculator.</td>
</tr>
</tbody>
</table>
Table 5. List of Changes on UCC25630-1EVM-291 (continued)

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>ORIGINAL VALUE</th>
<th>NEW VALUE</th>
<th>REASONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>R13</td>
<td>357 Ω</td>
<td>237 Ω</td>
<td>ISNS resistor should be reduced by a factor of 1.5.</td>
</tr>
<tr>
<td>R14</td>
<td>732 kΩ</td>
<td>267 kΩ</td>
<td>LL/SS upper resistor value is determined by setting desired burst mode threshold for exit equal to 1.2 V in the design calculator.</td>
</tr>
<tr>
<td>R15</td>
<td>402 kΩ</td>
<td>147 kΩ</td>
<td>LL/SS lower resistor value is determined by setting desired burst mode threshold for exit equal to 1.2 V in the design calculator.</td>
</tr>
<tr>
<td>R17</td>
<td>42.2 kΩ</td>
<td>41.2 kΩ</td>
<td>BW upper resistor value is determined by setting the burst mode threshold entry and exit ratio to 0.6 (User Option 5) in the design calculator.</td>
</tr>
<tr>
<td>R18</td>
<td>10 kΩ</td>
<td>8.06 kΩ</td>
<td>BW lower resistor value is determined by setting the burst mode threshold entry and exit ratio to 0.6 (User Option 5) in the design calculator.</td>
</tr>
<tr>
<td>R20</td>
<td>6.04 kΩ</td>
<td>1 kΩ</td>
<td>R20 is decreased to prevent opto-coupler saturation and reduce gain to maintain stable compensation.</td>
</tr>
<tr>
<td>C28</td>
<td>0.047 µF</td>
<td>0.01 µF</td>
<td>Compensation adjustment to improve burst mode pattern.</td>
</tr>
<tr>
<td>R22</td>
<td>10 kΩ</td>
<td>33.2 kΩ</td>
<td>Adjustment to keep compensation zero in the same location.</td>
</tr>
<tr>
<td>C17</td>
<td>0.15 µF</td>
<td>0.056 µF</td>
<td>Decrease startup time.</td>
</tr>
</tbody>
</table>
Figure 5. UCC25630-1EVM-291 Modified Schematic
7.5 **Performance of UCC256404 on UCC25630-1EVM-291**

Performance data is taken on UCC25630-1EVM-291 after implementing the changes from Section 7.4. *UCC25630-1EVM-291 User’s Guide* shows the baseline measurements for the UCC25630x on the original EVM.

7.5.1 **Standby and Light Load Power**

Table 6 lists the total standby power measurement for the standalone EVM. The average input power is measured over a two minute interval.

<table>
<thead>
<tr>
<th>$I_{OUT}$ (mA)</th>
<th>$V_{OUT}$ (V)</th>
<th>$P_{OUT}$ (mW)</th>
<th>$V_{IN}$ (V)</th>
<th>$I_{IN}$ (mA)</th>
<th>$P_{IN}$ (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>12.06</td>
<td>0.0</td>
<td>389.82</td>
<td>0.137</td>
<td>53.31</td>
</tr>
<tr>
<td>10.97</td>
<td>12.06</td>
<td>132.30</td>
<td>389.82</td>
<td>0.570</td>
<td>222.21</td>
</tr>
<tr>
<td>20.97</td>
<td>12.06</td>
<td>252.90</td>
<td>389.82</td>
<td>0.970</td>
<td>378.01</td>
</tr>
<tr>
<td>50.95</td>
<td>12.05</td>
<td>613.95</td>
<td>389.81</td>
<td>2.177</td>
<td>848.61</td>
</tr>
<tr>
<td>100.90</td>
<td>12.05</td>
<td>1215.85</td>
<td>389.79</td>
<td>4.168</td>
<td>1624.75</td>
</tr>
</tbody>
</table>

7.5.2 **Efficiency**

Figure 6 illustrates the EVM efficiency graph.

![Figure 6. Efficiency](image)

7.5.3 **Audible Noise**

Figure 7 and Figure 8 show the audible noise measurements during burst mode operation. The measurements are performed in a soundproof container with the microphone 5 mm above the transformer.
Figure 7. Audible Noise Measurement at 10 mA Load

Figure 8. Audible Noise Measurement at 500 mA Load
7.5.4 Steady State

The following waveforms show the resonant capacitor voltage (VCR) and low side gate voltage (LO) with 115 VAC, 60 Hz applied to the AC input, and 390 VDC applied to the DC input. Figure 9 and Figure 10 show the waveforms during burst mode.

Figure 9. Steady State Waveforms at 10 mA Load (Ch1 = VCR; Ch3 = LO)

Figure 10. Steady State Waveforms at 500 mA Load (Ch1 = VCR; Ch3 = LO)
Figure 11. Steady State Waveforms at 1 A Load (Ch1 = VCR; Ch3 = LO)

Figure 12. Steady State Waveforms at 10 A Load (Ch1 = VCR; Ch3 = LO)
7.5.5 Load Transient

The following waveforms show the output voltage with 115 VAC, 60 Hz applied to the AC input, and 390 VDC applied to the DC input.

Figure 13. 10 mA to 10 A Transient (Ch1=V_{out}; Ch4 = I_{out})

Figure 14. 1 A to 10 A Transient (Ch1=V_{out}; Ch4 = I_{out})
7.5.6 Loop Response

The following plot shows the loop response with 115 VAC, 60 Hz applied to the AC input, and 390 VDC applied to the DC input.

![Bode Plot at 10 A Load](image)

**Figure 15. Bode Plot at 10 A Load**

8 Summary

The UCC25630x and UCC25640x are both LLC controller families offering excellent standby power and transient response performance with a rich feature set. The UCC25640x includes additional features to allow for greater flexibility in the LLC converter design as well as features to mitigate audible noise without sacrificing standby power performance. The additional features of UCC25640x allow for reduction in BOM count and superior system performance.
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