Application Report
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Voltage Regulator Solutions for Xilinx™ Virtex™ E Dual Voltage FPGAs

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ABSTRACT

This application report serves as a reference for engineers designing with Xilinx™ 2.5-V and 1.8-V Virtex™ multivoltage FPGA products. It provides basic information on the issues facing engineers not experienced with multivoltage type products.

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1 Introduction

Many devices, such as digital signal processors (DSP), microprocessors, and field-programmable gate arrays (FPGA), are designed to consume minimum power while providing high performance at low cost. This is achieved using advanced technologies that make available smaller process geometries. These smaller geometries require lower operating voltages and very often, multivoltage-power-supply support for proper operation.

Today's leading-edge DSPs are already in production using these 0.25, 0.18, and 0.15 micron processes that require 3.3 V for I/O, and 2.5 V, 1.8 V, or 1.5 V for their cores. Although 2.5-V and 1.8-V power-supply requirements are not new to TI DSPs, these are relatively new to FPGA suppliers and are becoming more common in their products.

Texas Instruments has a complete line of power-supply devices to support low-voltage and multivoltage DSPs. These same devices can be used to support the requirements of the most current Virtex™ FPGA families from Xilinx™. This application report serves as a reference for engineers designing with Xilinx™ 2.5-V and 1.8-V Virtex™ multivoltage FPGA products. The report discusses the following topics:

- Understanding core and I/O requirements for the Virtex™ family
- Potential issues associated with multivoltage components
- Current estimations, ICC_{INT} and ICC_{IO}, for each Virtex family member
- Supply voltage regulation options
- TI recommended solutions for power management

2 Virtex™ Core and I/O Voltage Requirements

Table 1 summarizes the Virtex family core and I/O supply voltage requirements. The core voltage listed is required for proper internal operation. The I/O voltage is more flexible, addressing the particular interface needs of a system.

Virtex™ devices support 5 V tolerant I/Os as well as many different output types LVTTL, CMOS, LVDS, PCI, LVPECL, SSTL, HSTL, AGP, GTL, GTL+, and CTT.

Table 1. Xilinx™ Virtex™ Offering

DEVICE	VCC_{INT}	VCC_{IO}
XCV50/50E	2.5 V/1.8 V	3.3 V
XCV100/100E	2.5 V/1.8 V	3.3 V
XCV150	2.5 V	3.3 V
XCV200/200E	2.5 V/1.8 V	3.3 V
XCV300/300E	2.5 V/1.8 V	3.3 V
XCV400/400E	2.5 V/1.8 V	3.3 V
XCV600/600E	2.5 V/1.8 V	3.3 V
XCV800	2.5 V	3.3 V
XCV1000/1000E	2.5 V/1.8 V	3.3 V
XCV1600E	1.8 V	3.3 V
XCV2000E	1.8 V	3.3 V

3 Multivoltage Device Issues

Smaller feature sizes are driving the need for dual voltage rail ICs. When designing with these type components, be aware of potential issues such as latch-up and device electrical stressing. Latch-up can take place when a device operates in a voltage range that brings about functional uncertainties, placing all or a part of the device in a random unknown state. An example is hot card insertion when subsystems are socketed into an active system before the power supply can provide current to the device's V_{CC} and ground planes. With this scenario, larger than normal currents can be present on the device due to low impedance paths being created from V_{CC} to ground. This could lead to electrical damage and device failure.

Electrical overstressing can also occur when improper V_{CC} power sequencing up and down occurs between the power rails. In multirail devices, differing voltages present the possibility of higher voltages being placed on the gates to the drivers of the I/O. Internal parasitic structures can conduct, reinforcing themselves until potentially destructive conductive currents are produced. These higher potentials across the I/O or other pins can lead to abnormal stresses placed on the oxide levels of the device. The net effect from this is potential long-term reliability problems. These conditions can be avoided if the issues are understood and proper design techniques are used. These include:

- Proper power-up and power-down sequencing of the core and I/Os
- Proper device power ramp-up
- Appropriate system-power management control implementation
- Full understanding of the characteristics of other components in the system, as well as

For proper device operation, suppliers of multivoltage devices often have specific guidelines the designer must follow. TI recommends checking with the supplier to see if special conditions exist for their device and if recommendations are given.

3.1 Xilinx™ Recommendations for Virtex™ Series FPGAs

Xilinx™ has taken the necessary steps in designing their Virtex™ FPGA products to make sure the issues previously covered are of less concern with their products. A summary of their recommendations and claims, documented in the data sheets, is as follows:

- The core (VCC_{INT}) and I/O planes (VCC_{IO}) on Xilinx Virtex FPGAs can be powered in any order however removing VCC_{INT} while still applying VCC_{IO} over extended periods of time may affect reliability of the device over time.
- V_{CC} must rise monotonically and reach proper operating levels in less than 50 milliseconds per device data sheet.
- Signal V_{IN} levels should not exceed VCC_{IO} by more than 3.6 V for protracted periods of time (24 hours).

Virtex™ devices I/Os are held at a known state (pulled up, pulled down, or in 3-state condition) during power up. Once the device exceeds the minimum voltage required for proper operation, the I/Os are released from their 3-state condition and set to their configured voltage levels. If VCC_{INT} is lost, the I/Os will go to the 3-state condition and return to their preconfiguration state.

NOTE: If input and I/O pins are left floating or toggling during configuration, the device may consume additional current.

4 Load Current Estimations for Virtex™ Devices

The power consumption of Xilinx™ Virtex™ FPGAs is design-dependent with a number of factors influencing the final numbers. Typically, multivoltage devices can be broken down into two sections: the core logic and the I/O. For estimation purposes, it is best to treat each section separately to determine current sourcing requirements for the voltage rail supporting that area of the chip. The list below describes various factors that affect the current consumption number. The factors are listed in most significant to least significant order.

4.1 Core

- Internal resources used (number of logic cells/RAM block used)
- Sequential, combinatorial or the ratio of sequential/combinatorial used
- Toggle rates
- Percentage of internal logic cells toggling on the same clock
- Routing
- Standby power (minimal in larger devices)
- I/O power

4.2 I/O

- Output type
- Operating clock frequencies
- Number of outputs toggling at once
- Output loading
- Output drive strength

These factors have been included in the Virtex power estimator tool located on the Xilinx website (*http://www.xilinx.com/support/techsup/powerest/*). Values generated from the estimator are typical results. A more accurate estimate of dynamic power consumption is possible when switching frequencies at each node are known and complete system behavior has been taken into account.

4.3 Assumptions Used: Current Estimations for the Various Devices

Typically, specific design information extracted from the Virtex development tools is used to fill in the necessary categories in the estimator program. A simplified approach using basic assumptions is listed below. These results can serve as a first cut estimate.

4.4 Core Assumptions

- Average ratio of internal elements toggling at each clock, 15% (8–10% is typical)
- Internal makeup is 50% sequential and 50% combinatorial.
- 100% use of internal CLBs/slices in device for extreme worst case
- Single module used for whole chip, driven at one single average clock rate.
- For $I_{CCINT\ ACTIVE}$ estimates, dc standby currents were included in figures.

- For Xilinx™ calculator: 2 slices/CLB, 2 FF/slice, 2 LUT (combinatorial look-up table)/slice were used.
- No PLL or memory blocks used. Medium routing selected.

Table 2. Typical ICC_{INT} Current Draw for Virtex™ Family

	V_{CC} INT (V)	NO. CLBs USED	%FF USED	%LUT (COMB.)	%Int Toggle	(mA) AT 25 MHz	(mA) AT 50 MHz	(mA) AT 100 MHz
XCVxxxx								
XCV50	2.5 V	384	50	50	15	62	119	232
XCV100	2.5 V	600	50	50	15	99	188	366
XCV150	2.5 V	864	50	50	15	143	272	531
XCV200	2.5 V	1176	50	50	15	195	373	728
XCV300	2.5 V	1536	50	50	15	257	491	958
XCV400	2.5 V	2400	50	50	15	481	927	1818
XCV600	2.5 V	3456	50	50	15	592	1136	2222
XCV800	2.5 V	4704	50	50	15	817	1568	3071
XCV1000	2.5 V	6144	50	50	15	1081	2078	4072
XCVxxxxE								
XCV50E	1.8 V	384	50	50	15	38	72	138
XCV100E	1.8 V	600	50	50	15	61	114	219
XCV200E	1.8 V	1176	50	50	15	123	229	442
XCV300E	1.8 V	1536	50	50	15	162	303	584
XCV400E	1.8 V	2400	50	50	15	305	576	1118
XCV600E	1.8 V	3456	50	50	15	381	714	1382
XCV1000E	1.8 V	6144	50	50	15	707	1331	2578
XCV1600E	1.8 V	7776	50	50	15	912	1721	3339
XCV2000E	1.8 V	9600	50	50	15	1176	2199	4245
XCV2600E	1.8 V	12696	50	50	15	1581	2981	5782
XCV3200E	1.8 V	16224	50	50	15	2056	3906	7607

4.5 I/O Considerations

Current drawn from the device I/Os depends on the number of I/Os available and used in the package. Table 3 lists the maximum number of user-available I/Os for each package offered. Information provided by this table, along with assumptions below, was used to calculate current values in Table 4.

4.6 I/O Assumptions

- Output loads are 30 pF
- I_{DCOUT} is ignored because capacitive loads are assumed. LVTTL 3.3 V I/O were used with 8 mA drive output strength. Note that I_{IOOUT} current can vary when using GTL, SSTL, HSTL, and GTL I/Os.
- 25% maximum of outputs switch simultaneously (15% is typical).
- Assume average toggle rate for all I/Os.
- I/O frequency calculated using 33 MHz and 66 MHz data rate speeds.
- 50% of I/Os are inputs and 50% are outputs.

Table 3. Virtex™ Maximum User I/O Available in Package

	V_I	CS 144	TQ 144	PQ 240	HQ 240	BG 256	BG 352	BG 432	BG 560	FG 256	FG 456	FG 676	FG 680	FG 860	FG 900	FG 1156
XCV50/50E	3.3 V	94	98	166		180				176						
XCV100/100E	3.3 V	94	98	166		180				176						
XCV150	3.3 V			166			260			176	260					
XCV200/200E	3.3 V			166			260			176	260					
XCV300/300E	3.3 V			166			260	316			312					
XCV400/400E	3.3 V				166			316	404			404				
XCV600/600E	3.3 V				166			316	404			444	512		512	
XCV800	3.3 V				166			316	404			444	512			
XCV1000/1000E	3.3 V								404				512	660	660	660
XCV1600E	3.3 V												512	660	700	724
XCV2000E	3.3 V												512	660		804
XCV2600E	3.3 V															804
XCV3200E	3.3 V															804

Table 4. Virtex™ ICC_{IO} (Output) mA

	I/O Freq MHz	TQ 144	PQ 240	HQ 240	BG 256	BG 352	BG 432	BG 560	FG 256	FG 456	FG 676	FG 680	FG 860	FG 900	FG 1156
XCV50/50E	33	28	47		51				50						
	66	56	95		103				101						
XCV100/100E	33	28	47		51				50						
	66	56	95		103				101						
XCV150	33		47		51	74			50						
	66		95		103	148			101						
XCV200/200E	33		47		51	74			50	81					
	66		95		103	148			101	153					
XCV300/300E	33		47			74	90		50	81					
	66		95			148	181		101	153					
XCV400/400E	33		45	47			90	115			115				
	66		90	95			181	231			231				
XCV600/600E	33			47			90	115			127	146		146	
	66			95			181	231			254	292		292	
XCV800	33			47			90	115							
	66			95			181	231							
XCV1000/1000E	33			45				115				146	188	188	188
	66			90				231				292	377	377	377
XCV1600E	33							115				146	188	200	207
	66							231				292	377	400	414
XCV2000E	33											146	188		230
	66											292	377		459
XCV2600E	33														230
	66														459
XCV3200E	33														230
	66														459

5 Supply Voltage Regulator Options

Supply power to the core and I/O requires a 5 V, 3.3 V, 2.5 V, and at times a 1.8 V regulator. Depending on the key system requirements, cost and time to market, the solution can be a linear regulator, a switching regulator solution, or switching power supply module. Trade-offs of the linear regulator and switching regulator power supplies are outlined below.

5.1 Linear Regulators

When to use:

- Board space is critical.
- At times the most cost effective in terms of total cost
- Low output noise is important (EMI or ripple).
- Efficiency is less critical.
- Simplistic design is preferred.
- Low to medium output currents needed.
- Fast responses to input and required transients.
- Step down applications

In typical applications, a linear regulator solution requires an input capacitor to reduce the trace inductance effect and any noise present on the input of the LDO. This is usually placed as close as possible to the regulator input pin. The LDO also requires an output capacitor to handle the system transient response and stability. The size and ESR affects stability over load and the ability to respond to transients caused by rapid changes in the load current. This capacitor size and ESR need to be adjusted according to the system accuracy required. For high frequency applications a small ceramic bypass capacitor at the output is recommended to help reduce high frequency noise that may be present.

Some of the more recent members of the TPS family of low dropout linear regulators from TI offer flexibility by allowing the user to select any capacitor type, small size, with low ESR to address the system needs. At times, a lower value and higher value capacitor can be placed in parallel to better address the fast transient current spikes and to reduce overall ESR.

Additional functions such as on/off control (enable) and undervoltage detection (voltage supervisors) have been integrated on-chip and are available in certain families from TI.

Dual output devices available in medium to high-output currents are available as well and are listed in the recommended solutions table.

5.2 Inductive Switching Regulators

Switching supplies are known for excellent efficiency, but their output is noisy. This degrades regulation and performance and at times is critical when powering analog circuits.

When to use:

- Efficiency is critical 80–95%.
- Applications with wide input voltage range
- Larger output currents are required.

- Board space is not a key concern.
- Cost is less an issue.
- Step up, down and inverting applications
- Noise is not a major concern.

Switching regulator solutions require inductors and input and output capacitors for dc-dc conversion. For ac-dc conversion, isolation transformers are required. The TI/Unitrode line of PWMs provide solutions for these types of applications, but will not be covered in this report.

5.3 Inductive Switching-Power-Supply Module

Power supply modules are complete drop-in power supplies by Power Trends (acquired by TI in late 1999). Most are dc-dc converters with various options available in each module family group.

When to use:

- Limited design resources
- Time to market is critical
- Prototyping
- Requirements needed and provided by inductive switchers
  - Efficiency is critical 80–95%.
  - Applications with wide input voltage range
  - Larger output currents are required.
  - Board space is not a key concern.
  - Step up, down, and inverting applications
  - Noise is not a major concern.

6 TI Recommended Solutions

TI can offer a number of different solutions. Below is a summary of TI's offerings in linear regulators that support output currents from 50 mA to 5 A. Although there are many solutions for the same output current, the sub families focus on parameters that are key to different application needs. These include low noise, low Iq, high PSRR, and fast transient response solutions.

Table 5. Linear Regulators

DEVICE	I_O MAX (mA)	V_I MAX	V_O OPTIONS (V)	COMMENTS
50 mA – 150 mA Maximum Supply Current LDO				
TPS760XX	50	16	3, 3.2, 3.3, 3.8, 5	SOT–23, with shutdown
TPS770XX	50	13.5	Adjust, 1.2, 1.5, 1.8, 2.5, 2.7, 3.0, 3.3, 5	SOT–23, with shutdown, 17 μA Iq
TPS761XX	100	16 V	5, 3.8, 3.3, 3.2, 3	SOT–23, with shutdown
TPS769XX	100	13.5	Adjust, 1.2, 1.5, 1.8, 2.5, 2.7, 3, 3.3, 5	SOT–23, with shutdown, 17 μA Iq
TPS763XX	150	10 V	5, 3.3, 2.5, 1.8, adjust	SOT–23, with shutdown
TPS764XX	150	10 V	3.3, 3, 2.7, 2.5	SOT–23, with shutdown
TPS765XX	150	10 V	Adjust, 1.2, 1.5, 1.8, 2.5, 2.7, 3, 3.3, 5	SOIC–8, with shutdown and PG
150 mA up to 250 mA LDO				
TPS74XX	200	7	1.5, 1.8 ,2.5 ,3, 3.3	SO–8, enable, 1 μF capacitor. for stability
UCC386/87/88	200	9	5, 3.3, adjust	TSSOP
TPS766XX	250	10	Adjust, 1.2, 1.5, 1.8, 2.5, 2.7, 3, 3.3, 5	SOIC–8, PG, with shutdown, stable with 4.7 μF capacitor
TPS72XX	250	10	5, 4.8, 3.3, 2.5, adjust	Adjust down to 1.2 – 9.75 V
250 mA up to 500 mA LDO				
TPS71XX	500	10	5, 4.8, 3.3, 2.5, adjust	Adjust 1.2 – 9.75 V
TPS71HXX	500	10	5, 4.8, 3.3, adjust	Adjust 1.2 – 9.75 V, HTSSOP package
TPS7333	500	10	5, 4.8, 3.3, adjust	Adjust 1.2 – 9.75 V, w / SVS
TPS775XX	500	13.5	Adjust, 1.5, 1.8, 2.5, 3.3	With SVS, EN
TPS776XX	500	13.5	Adjust, 1.5, 1.8, 2.5, 3.3	With PG, EN
750 mA LDO				
TPS777XX	750	13.5	5, 3.3, 3, 2.8, 2.7, 2.5, 1.8, 1.5, adjust	With SVS, EN
TPS778XX	750	13.5	5, 3.3, 3, 2.8, 2.7, 2.5, 1.8, 1.5, adjust	With PG, EN
Up to 1 A LDO				
TPS767XX	1000	10	5, 3.3, 3, 2.8, 2.7, 2.5, 1.8, 1.5, adjust	Adjust from 1.5 – 5 V, En, SVS , PowerPad™ package, any capacitor.
TPS768XX	1000	10	5, 3.3, 3, 2.8, 2.7, 2.5, 1.8, 1.5, adjust	Adjust from 1.5 – 5 V, En, PG, PowerPad™ package, any capacitor.
UCC381–X	1000	9	3.3, 5, adjust	Adjust 1.25 – 8.85 V
3 – 5 A LDO				
UCC383–X	3000	9	3.3, 5, adjust	Adjust 1.25 – 8.85
UC382–X	3000	7.5	2.5, 5	Adjust 1.2 – 6
UC385–X	5000	7.5	1.2, 1.5, 2.1, 2.5	

PowerPAD is a trademark of Texas Instruments.

Table 6. Dual-Output 250-mA to 1-A LDOs

DEVICE	Iout1/Iout2 MAX (mA)	V_I MAX	V_O OPTIONS (V)	COMMENTS
TPS701XX	500/250	6	Adjust/adjust, 3.3/2.5,3.3/1.8, 3.3/1.5,3.3/1.2	TSSOP–20 PowerPad™ package, power sequencing control on chip, EN, SVS
TPS73HD3xx	750/250	10	3.3, 2.5, 1.8, Adj	Dual, with SVS and EN
TPS768XX	1000/1000	10	5, 3.3, 3, 2.8, 2.7, 2.5, 1.8, 1.5, adjust	Adjust from 1.5 – 5 V, En, PG, PowerPad package, any capacitor
TPS767D3XX	1000/1000	10	3.3/adjust, 3.3/2.5, 3.3/1.8	Dual with SVS and En., SVS, PowerPad package, any capacitor

6.1 Switching Regulators ≥ 3 Amps

There are a number of switching regulator solutions TI can offer. These include current mode, voltage mode, synchronous hysteretic controllers, as well as a number of PWMs from the TI/Unitrode families. Samples of various devices are listed in Table 7. Go to the TI website, *www.ti.com,* to see the full product offering.

Table 7. Switching Regulator Solutions

DEVICE	Iout RANGE (A)	V_I RANGE (V)	V_O OPTIONS (V)	COMMENTS
TL5001A	3 – 10	3.6 – 40	3.6 – 40	3.6 V – 40 V, PWM
UCC3585	< 8	1.2 – 6	1.25 – 4.5	Released 2H00
TPS5102	<12	4.5 – 25	Down to 1.3	Dual output PWM/skip
TPS5602	3 – 20	4.5 – 25	5, 3.3, 2.5, 1.8, 1.5, Adj	Dual output, hysteretic control ripple
TPS5103	<12	4.5 – 25	Down to 1.3	PWM, skip, or hysteretic
TPS56XX	3 – 20	12	5, 3.3, 2.5, 1.8, 1.5	Hysteretic, single output
TPS56100	3 – 30	5	5, 3.3, 2.5, 1.8, 1.5	Hysteretic, single output
TPS56300	Dual up to 30 A for switcher output	2.8 to 5.5	1.3 to3.3	Ideal for power split rail, sequencing onboard with programmable slow-start. Second output is LDO.

6.2 Power Modules (Power Trends)

The TI/Power Trends modules listed below are 5-V and 3.3-V input devices. Modules not listed support input voltages of 12 V – 75 V and output voltages of up to 18 V. Access the TI website for the full product offering.

Table 8. 5-V/3.3-V Input Switching-Power-Supply Modules

DEVICE	I_O RANGE	V_I RANGE	V_O OPTIONS (V)	COMMENTS
PT550x	1.5A	5 V/3.3 V	1.2 – 3.3	3.3-V input available
PT6405	3.0A	5 V	1.2 – 3.3	
PT650x/20	8A	5 V/3.3 V	1.2 – 3.6	3.3-V input available
PT660x	9A	5 V/3.3 V	1.2 – 3.6	3.3-V input available
PT670x	13A	5 V/3.3 V	1.3 – 3.5	3.3-V input available
PT770x	18A	5 V/3.3 V	1.3 – 3.5	3.3-V input available
PT771x	20A	5/3.3 V	1.3 – 3.5	3.3-V input available
PT7777	32A	5 V/3.3 V	1.3 – 5.5	3.3-V input available

6.3 Summary

Advanced technologies make small geometries available requiring lower operating voltages and multiple-voltage power-supply regulation. These conditions are becoming common in many digital-signal processors (DSPs), field-programmable gate arrays (FPGAs), and general-purpose microprocessors for proper operation. FPGA solutions can radically differ from design to design, making it difficult to predict current consumption. This application report focused on the Xilinx Virtex 2.5-V and 1.8-V core families and attempted to provide the design engineer a first-cut estimate of the currents these devices draw using a simple design example.

Also discussed were potential issues associated with multivoltage components such as latch-up and device overstressing. This was then followed by various TI power-supply solutions which included low-dropout linear regulators from TI/Unitrode, inductive switching regulators from TI/Unitrode, and inductive switching power-supply modules from TI/Power Trends. Please access the TI website: www.ti.com for the most current product offerings.

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