Dual Output Power Supply Sequencing for High Performance Processors

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Abstract

Dual voltage power supply architectures are becoming commonplace in high performance microprocessor and digital signal processor (DSP) systems. To save power and increase processing speeds, processor cores have smaller geometry cells and require lower supply voltages than the system bus voltages. Power management in these systems requires special attention. The reliability, performance, and cost trade-offs facing designers are not adequately addressed by yesterday's power management ICs and application literature. This article addresses these topics and suggests solutions for output voltage sequencing and how a new power management IC can improve system reliability and reduce system cost.

Introduction

In dual voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and I/O voltage supplies during power up and power down operations. Sequencing refers to the order, timing and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long term reliability of the dual voltage device, while the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic or data converter ICs.

The threat to long term reliability of a dual voltage device comes from stress placed on internal circuits that connect portions of the chip powered by separate supply rails. This type of stress is considered low level and occurs when one rail is active while the other is inactive. No permanent damage or reliability problems occur unless the condition persists over extended periods of time. Extended periods are on a time scale that does not apply to ordinary design considerations (i.e. hours, days, or months). The processor is not harmed from a single, or even several, poorly controlled power up and power down cycles. However, cumulative exposure to uncontrolled power up and power down cycles can compromise the reliability of dual voltage devices in systems that are cycled on and off many times a day.

The reliability problem with the interface circuitry can be immediate and catastrophic. A potential for latch-up exists when a processor's I/O interface and the I/O interface of a supporting peripheral such as memory, FPGA, or data converter are not powered from the same supply.Latch-up occurs when current is forced through the substrate of a CMOS device and triggers a self-sustained conduction path in back to back parasitic bipolar transistors. These parasitic transistors are unavoidable in most CMOS technologies, and form a structure similar to an SCR, connected between the power supply and ground. Once triggered, current continues to flow until the current is interrupted. The trigger current may occur if power is applied unevenly to the interfaces on a shared I/O bus. Latch-up can also be triggered when an input pin is driven above or below the supply rails after both devices are powered up. A latch-up
condition may cause sufficient damage that is immediately noticeable, or it may affect reliability over a longer period of time. In order to handle this problem, it is essential to power peripherals connected to the processor and system ICs from the same supply that powers the processor's I/O section.

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bi-directional bus during power up. Bus contention may also affect I/O reliability. Power supply designers should check the requirements regarding bus contention for individual devices.

**Power Sequencing Solutions**

To avoid potential problems with the processor and system ICs, designers can apply three general techniques for power up sequencing: sequential, ratiometric or simultaneous [1]. Sequential power up, as name implies, powers up the two rails one after the other. Typically the second rail begins to ramp up once the first rail reaches regulation. Alternately, the second rail may begin its ramp after a set delay from the start of the first rail. Either method must comply with the processor manufacturer's restriction on the minimum and maximum time one supply is not powered or the duration and amount that one supply exceeds the other. With the second or ratiometric method, the two rails begin to power up and reach regulation at the same time. This requires a higher slew rate for the rail with the higher final voltage, and results in the maximum voltage differential occurring when regulation is reached. However, some processors may not tolerate the instantaneous voltage differences that occur before regulation is reached or the processor may draw high current from one supply during this period. The third approach eliminates instantaneous voltage differences and minimizes the magnitude and duration of stresses. A common way of implementing this method is simultaneous power up, in which the voltage rails rise together and at the same rate, with the higher or I/O voltage rail continuing after the lower or core voltage rail has reached its final value. These three types of power management are shown in Figure 1 below:

![Sequential Startup](image1.png) ![Ratiometric Startup](image2.png) ![Simultaneous Startup](image3.png)

**Figure 1**: Sequential, Ratiometric and Simultaneous Application of power.

Microprocessor manufacturers generally specify restrictions on time and voltage differences during power up but do not specify which sequencing method the power subsystem designer should use. The tightest published restrictions are for the Motorola Power PC devices. The PowerPC specification allows an out of tolerance voltage condition to persist for a maximum of 50 microseconds. PowerPC datasheets recommend that diodes be connected in both directions between the core and I/O rails to prevent the out of tolerance conditions in the absence of coordinated power up of the core and I/O rails. This may be an adequate method when the voltage differences between the core and I/O are small, but as the voltage between the core and I/O supplies becomes larger the "antiparallel" diode method may not be sufficient. The forward voltage drop specifications of diodes are not tight enough for accurate and predictable results. For other processors, the restrictions are not as well defined. While the voltage rails usually do
not have to be powered in a specific order, high startup currents or bus contention may occur. The ideal solution would be to use dual power supply controllers or a power supply controller with linear regulator controller with built-in sequencing functions. These devices are available on the market but often have limitations to the combination of output voltages or levels. A recently released product from Texas Instruments, TPS54610, has the flexibility to implement sequential, ratiometric and simultaneous startup and can accommodate almost any sequencing combination.

The TPS54610 device is a monolithic synchronous buck (step down) regulator that can operate from an input of 3.0 to 6.0 – volts [2]. The device is a power supply controller with integrated power MOSFETs in a thin shrink small outline package (TSSOP) that can deliver more than six amperes to output voltages as low as 0.891V. The device has a solderable thermal tab on the bottom of the package that gives it a very low impedance thermal path that enables it dissipate nearly two watts at an ambient temperature of 70 degrees centigrade. The operating input voltage range makes the device an ideal fit DSP systems that need to operate from 5-V or 3.3-V buses. Its power good, slow start, and synchronization functions are particularly useful in those DSP or ASIC systems that require sequencing of two or more power supplies.

Sequential Startup and the Power Good Function

The power good function is an open drain output that is asserted low when the output voltage (the voltage on the Vsense pin) is less than 90% of the internal reference voltage. The power good pin transitions to high impedance when the output voltage is greater than 93% of the internal reference voltage. The power good pin can be connected to another device's enable pin to implement sequential startup, see Figure 2. When two TPS54610 devices are paired together, a pull-up resistor on the power good pin is not needed since the enable pin has an internal pull up. From Figure 3, the sequential startup waveforms that can be observed are core voltage, I/O voltage, input voltage, and power good voltage on channels 1, 2, 3 and 4, respectively. Note that the momentary "glitch" on the power good voltage occurs before the DSP core voltage and I/O voltage are active and is not a problem for the system. When the input voltage to the power supplies reaches an internal bias threshold (approximately 2 volts), the power good signal becomes active and asserts low. After the input voltage ramps above the under voltage lockout threshold, the core voltage supply starts to ramp linearly from zero to its regulation value of 1.8 Volts. When the core voltage approaches regulation, the power good pin becomes high impedance (open drain). The enable input to the I/O power supply, which is connected to the power good pin of the core supply now goes high and the I/O power supply is allowed to slow-start and regulate. As shown in the block diagram and oscilloscope waveforms Figure 2 and 3, it is very easy to use two TPS54610 devices to implement sequential startup. Since there is a difference in the core and I/O voltage and the total startup time may be longer when implementing sequential startup it may be more desirable to use ratio-metric or simultaneous startup.

Ratio-metric and Simultaneous Startup and the Slow Start Function

Several currently available power supply controllers and regulators implement either an internal slow start or external slow start, but not both on a single device. The TPS54610 has both internal and external slow start functions that linearly increase the reference voltage during slow start. Several devices available on the market implement slow start by limiting the current through the high side power switch at startup. Limiting the current through the high side power switch is adequate to implement slow start, but it is not a good way to provide controlled ratio-metric or simultaneous startup of the output voltage at startup.

The default slow-start time of he TPS54610 is approximately three milliseconds [2]. This can be increased by the addition of a ceramic capacitor on the slow start/enable (SS/ENA) pin to ground. The external capacitor is charged via a 5-microampere current source. The SS/ENA pin also functions as an
enable pin; once the voltage on the pin reaches approximately 1.2V, the device is enabled. The SS/ENA pin and the internal slow start voltages are compared and the lower of the two voltages is coupled to the error amplifier. External slow start capacitor values lower than 0.02 \( \mu \text{F} \) correspond to slow start times lower than the default slow start, which will override the external capacitor programming. Ratio-metric or simultaneous startup is implemented via the slow start function. The SS/ENA pins of two TPS54610 converters are connected together with one ceramic capacitor to ground (see Figures 4 and 6). Since there are two pull-up current sources connected, the capacitor will need to be larger than 0.04 \( \mu \text{F} \) to override the internal slow start time. Figure 5, shows the output voltage of two such converters connected for ratio-metric startup. Here, a 0.1 \( \mu \text{F} \) capacitor is used to give a slow start time of 9 milliseconds. The advantage of ratio-metric startup is that both output voltages will reach the final value at approximately the same time. But the disadvantage is that there is a differential voltage between the core and the I/O during the slow start interval. This voltage differential can be minimized using the simultaneous startup method shown in Figure 6.

To obtain simultaneous startup, both regulators are connected so that they track a common slow start voltage at their SS/ENA pins. The detailed circuit showing this technique is given in Figure 6. Here, the feedback resistor divider ratio on the core and I/O output is set to be the same at startup. In the diagram, the \( R_2/(R_1 + R_2) \) divider on the core supply is the same ratio as \( R_4/(R_3 + R_4) \) divider on the I/O supply. Once the core voltage reaches its regulated value, the PG pin on the 1.8V core supply is de-asserted, slowly pulling the gate up to the input voltage which turns on Q1, connecting R5 in parallel with R4. This action changes the resistor divider ratio of the I/O supply and adjusts its output voltage from 1.8V to 3.3V. The shared slow start interval where both power supplies are ramping up together is set by the 0.1 \( \mu \text{F} \) capacitor on the slow start enable pin, while the continued slow start rate of the I/O power supply is determined by the R-C time constant of R6 and C1. Figure 7 shows the measured simultaneous startup performance of the circuit in Figure 6. Channel 1 is the input voltage. Channel 2 is the core voltage and Channel 3 is the I/O voltage. The 3 millisecond delay of the I/O voltage ramping after the core voltage reaches 1.8V is from the gate voltage of Q1 rising from zero volts to the threshold voltage of Q1. The typical threshold voltage of the 2N7002 chosen for this demonstration is 2.1V. It is necessary for the \( R_{ds(on)} \) of Q1 to be relatively small compared to the feedback resistors so that it will not impact the output accuracy.

**Effects on Line Regulation, Load Regulation, and Stability**

When adding components to the feedback path, caution needs to be exercised when the power supply crossover frequency is high. The parasitic capacitance of Q1 may affect the frequency response of the I/O supply, if the resistance of the high side resistor (i.e. \( R_3 \) in Figure 6) of the voltage divider is relatively high resistance. A voltage divider resistance in the tens of kilo Ohms will not have any significant effect on the frequency response if the on resistance of Q1 is in the one Ohm range. For example, the drain-gate capacitance, drain-source capacitance, and gate-source capacitance of the 2N7002 MOSFET are approximately 5pF, 20pF, and 45pF and it has an on-resistance of 1.7 \( \Omega \) [3]. The ZXM61N02F MOSFET has an approximate drain-gate capacitance of 36pF, drain-source capacitance of 64pF, and gate-source capacitance of 364pF with an on-resistance of 0.18 \( \Omega \) [4]. A Saber model of the circuit shown in Figure 8 was developed for this circuit, and simulation was performed with and without the 2N7002. The simulations showed no significant degradation of the small-signal feedback characteristics of the converter. To demonstrate the impact on phase margin, a second simulation was performed, with a 10-fold increase in the resistor values and a 10-fold decrease in capacitor values versus those in Figure 8 using a higher capacitance MOSFET (the ZXM61N02F) in an effort to exaggerate the effect. The computer simulation results are shown in Figure 9, where the effect on the phase of a MOSFET with higher parasitic capacitance is noticeable above 30kHz. The simulation results with and without the
2N7002 with the compensation components in Figure 9 are almost the same. To confirm these simulations, the open loop frequency response was measured on a printed circuit board using a Venable 350 network analyzer and compared with the simulation results. The lab results showed that there was no significant difference in the frequency response when adding the 2N7002.

Also, the effects of the startup circuit to the DC line and load regulation were investigated. The results are shown in Table 1. The line regulation data was taken by varying the input voltage from 4.5V to 6.0V with a load of 6 amperes on regulators without the startup circuit, with the startup circuit disabled, and with the startup circuit enabled. The regulator tested without the startup circuit had a 0.010% line regulation with an output voltage of 3.3V.

The load regulation was measured at input voltage of 5 volts and varying the output load from 50mA to 6A. The line regulation of the power supply without the startup circuit was 0.05%. The load regulation was also measured on power supplies with the startup disabled and enabled with 0.120% and 0.07% errors, respectively. The load regulation with the startup circuit disabled appears to be twice as high as the circuit with startup circuit enabled but the voltage drop under the load test is the same.

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<tr>
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<th>w/o Startup Circuit</th>
<th>Disabled Startup Circuit</th>
<th>Enabled Startup Circuit</th>
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<tr>
<td>4.5 V to 6.0 V at 6.0A</td>
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<td>0.060%</td>
<td>0.068%</td>
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<tr>
<td>Load Regulation</td>
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<td>50 mA to 6.0 A at 5.0V</td>
<td>0.050%</td>
<td>0.120%</td>
<td>0.070%</td>
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Table 1. DC Line and Load Regulation

Conclusions

The TPS54610 device has slow start, power good, and synchronization functions that can be cost effectively implemented to provide a simple and robust dual output power supply for DSP, FPGA and other dual supply logic systems.

Acknowledgements

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References

Figure 2  Simple Block Diagram of Sequential Startup Configuration

Figure 3  Output Voltage Waveforms for Sequential Startup.
Channel 1: V(I/O)  Channel 2: V(CORE)  Channel 3: V(VIN)  Channel 4: V(PG)
Figure 4  Simple Block Diagram of Ratio-Metric Startup Configuration.

Figure 5  Output Voltage Waveforms for Ratio-metric Startup.
Channel 1: V(I/O) Channel 2: V(CORE) Channel 3: V(VIN)
Figure 6  Simple Block Diagram of Simultaneous Startup Configuration.

Figure 7  Output Voltage Waveforms for Simultaneous Startup.
Channel 1: V(I/O) Channel 2: V(CORE) Channel 3: V(VIN) Channel 4: V(PG)
Figure 8. TPS54610 Regulator with Feedback Compensation Components.

Figure 9. Saber Simulation Results.
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