ADVANCE INFORMATION

The Spartan™-3 FPGA configuration and JTAG ports commonly use signals with a 2.5-V swing. Alternatively, it is possible to use 3.3-V signals simply by adding a few external resistors. The 3.3-V signals can cause a reverse current that flows from certain configurations and JTAG input pins, through the FPGA, to the $V_{CCAUX}$ power rail. Xilinx recommends this current be limited to 10 mA (or less) per pin by adding a resistor $R_2$ (30 $\Omega$ or greater†) in series with each of these $V_{CCAUX}$-powered inputs.

The output of the switching converter or linear regulator provides $V_{CCAUX}$. To prevent the output from rising above its 2.5-V regulated voltage due to the reverse current flow, an additional resistor ($R_1$) connected from the output of the converter or regulator to GND is required. The maximum value for $R_1$ is computed as follows:

$$R_1 = \frac{2.5 \text{ V}}{(I_1 + \cdots + I_X)}$$

where $I \leq 10$ mA.

† Avoid choosing the series resistor value so high as to adversely affect signal quality.
‡ The regulator is assumed to be a typical linear regulator, such as TPS79425, which cannot sink reverse current, and thus requires $R_1$.

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