VREG Considerations in a 5-V and 3.3-V System Using the TPS2300/01/10/11

ABSTRACT

This application report illustrates the use of the TPS2300/2301/2310/2311 for a common dual 5-V/3.3-V application. The TPS2300/2301/2310/2311 are dual-channel hot-swap controllers that eliminate high-frequency, hot-plug or hot-removal transients, reduce inrush current, and provide overcurrent protection. The TPS2300 family can be easily configured for a 5-V/3.3-V application providing a unified input hot-swap function, system power-good signal, and power bus overload protection.

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1 Introduction

Electronic systems have used 5 V as the main high-current power source for many years. Digital and analog ICs are using 3.3 V more to make integrated circuit geometries smaller and consume less power. Although some may consider 5 V to be a legacy voltage, it is still common to see both as the main power sources for an electronic system.

This application report allows designers to quickly integrate a hot-swap function into a 5-V/3.3-V system.
2 Device Description

The TPS2300/2301/2310/2311 devices are dual-channel, hot-swap controllers that use external N-channel MOSFETs as high-side switches. These devices integrate features such as overcurrent protection, inrush current control, output-power status reporting, and separation of load transients from actual increases in load current. All support 3 V to 13 V on channel 1, 3 V to 5.5 V on channel 2, and provide the same basic functionality; see the device data sheets (SLVS265, SLVS275) for details.

2.1 Typical Application Diagram

A typical hot-swap application diagram using the TPS23xx family of hot-swap controllers is illustrated in Figure 1.

The block diagram in Figure 2 shows the internal functional circuits. These are low-voltage circuits and require an internal linear regulator for supply voltages greater than 5 V. The device logic is powered by the linear regulator called PREREG that creates 4.1 V from a VIN1 of 5 V to 13 V. The PREREG output is brought out to a pin called VREG so that a noise-decoupling capacitor can be added to provide a low-noise supply for the device internal circuits.

In designs where VIN1 is 5 V or less, the internal regulator is fully saturated and not necessarily required. This application report offers benefits and consequences of operating with a VIN1 of less than 5 V.

![Figure 1. Typical Schematic](image-url)
3 Bypassing the Internal Linear Regulator

Various benefits can be obtained if the PREREG linear regulator dropout and tolerance are removed. The schematic of Figure 3 shows this implementation.

The dropout voltage of the linear regulator can be neglected if the VREG pin is connected directly to VIN1. In this scenario, the 0.1-V drop of the internal regulator is eliminated. The VREG decoupling capacitor is no longer needed if VIN1 has a 1-µF to 10-µF capacitor.

Limitations of bypassing the internal regulator are:
1. VIN2 may not be connected to VREG because this will damage the linear regulator pass element in the PREREG block.
2. Because the PREREG linear input is connected internally to VIN1, a shorted condition can exist between VIN1 and VIN2 if VIN2 is connected to the PREREG output at VREG.
3. The maximum recommended voltage on VREG is 5.5 V, preventing VIN1 from being above 5.5 V.
3.1 **PREREG Linear Regulator, VREG Output, and the UVLO Function**

The VIN1 channel has been constructed to support 3-V up to 12-V operation whereas the VIN2 channel supports 3-V to 5.5-V operation. However, the PREREG linear regulator obtains its input only from VIN1. As with most controllers, this device has a UVLO, undervoltage lockout function, which is derived by looking at the PREREG output at VREG. Device start-up is not allowed until VREG is 2.85 V ±0.1 V. After turnon, the device does not turn off until VREG is 0.1 V below the turnon point.

Applying 5 V to VIN1 allows the PREREG linear to operate in the linear region. Its output at VREG is approximately 4.1 V. By operating in the linear region, this helps to prevent erroneous UVLO shutdown due to noise transients on the VIN1 input. Data-sheet specifications for PREREG are obtained with VIN1=4.5 V to 13 V as shown in **Table 1**.
A 3.3-V source applied to VIN1 requires evaluation of the UVLO function. The VREG UVLO specifications are shown in Table 2.

Table 2. VREG UVLO Thresholds

<table>
<thead>
<tr>
<th>VREG UVLO</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V_{(TO_UVLOstart)}</td>
<td>Output threshold voltage, start</td>
<td>2.75</td>
<td>2.85</td>
<td>2.95</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V_{(TO_UVLOstop)}</td>
<td>Output threshold voltage, stop</td>
<td>2.65</td>
<td>2.78</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V_{(UVLO_hysteresis)}</td>
<td>Hysteresis</td>
<td>50</td>
<td>75</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>UVLO sink current, GATEx</td>
<td>V_{(GATEx)} = 2.7 V</td>
<td>10</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

To determine where the device turns on, use the VREG UVLO limits, and add in the effects of the PREREG internal linear regulator and solve for the minimum VIN1.

\[
\text{VIN1_{min}} = V_{(TO\_UVLOstart)} \text{ max} + V_{(DROP\_PREREG)} \text{ max}
\]

PREREG dropout voltage = 0.1 V\(_{\text{max}}\)

\[
V_{(TO\_UVLOstart)} \text{ max} = 2.95 \text{ V}
\]

Therefore:

\[
\text{VIN1}_{\text{min}} = 2.95 \text{ V} + 0.1 \text{ V} = 3.05 \text{ V}
\]

Now compare this to a 3.3-V input source with a negative tolerance applied.

\[
\text{VIN1} = 3.3 \text{ V} - 10\% = 2.97 \text{ V}
\]

\[
\text{VIN1} = 3.3 \text{ V} - 5\% = 3.135 \text{ V}
\]

The minimum input to VIN1 must be 3.05 V to account for the dropout and UVLO tolerance. For a -10% variation of a 3.3-V input, this is not satisfied (2.97 V < 3.05 V). Although the -5% tolerance does satisfy the 3.05 V minimum, it does not allow much margin for input noise (3.135V > 3.05V by 0.085V). Therefore a designer would need to consider the tolerance of the VIN1 input and possible negative noise spikes and voltage drops across connectors and PCB traces that could affect this input.

With VREG connected to VIN1, the PREREG 0.1-V dropout variable is removed; so, the UVLO threshold is more accurate.

\[
\text{VIN1}_{\text{min}} = V_{(TO\_UVLOstart)} \text{ max} + V_{(DROP\_PREREG)} \text{ max}
\]

Now becomes

\[
\text{VIN1}_{\text{min}} = V_{(TO\_UVLOstart)} \text{ max}
\]

Because VREG UVLO start threshold is 2.75 V min, 2.85 V typical, 2.95 V max, VIN1 = 2.75 V min, 2.85 V typical, 2.95 V max for device turnon.

With VIN1 connected to 3.3 V, the UVLO provides a good input supervisor on VIN1. Supplying 3.3 V -10% = 2.97 V to VIN1 and with VIN1_{min} = 2.95 V max, the undervoltage lockout does not allow the 3.3-V input to be applied to OUT1 while it is less than -10% of regulation.

The UVLO function also provides hot-swap output sequencing. Device UVLO turnon is derived from VIN1 when VREG is connected to VIN1. Therefore, VIN2 is not turned on until VIN1 = 2.75 V min, 2.85 V typical, 2.95 V max.

A beneficial example of this would be a system with 5 V applied to VIN1 and 3.3 V applied to VIN2. Frequently, a system does not operate properly if the lower voltage rail is forced above the higher voltage rail during turnon. In this case, the VIN2 3.3-V output would not be turned on before the VIN1 5-V rail is above the UVLO of 2.85 V, close enough to 3.3 V to prevent parasitics from turning on.
Sequencing also works on power down to turn off the outputs when 5 V is falling; the controller turns off before the 5-V source was below the 3.3-V source.

3.2 Power-Good Circuitry

Normally the PWRGD signals would not be accurate during device disable because the disable mode turns off the PREREG linear and removes power to the internal circuitry. This puts the part in a low-power state drawing less than 5-μA total quiescent current. Subsequently, there is no voltage to drive the gate of the internal PWRGD MOSFETs so that they are at high impedance.

When operating with VIN1=VREG, the ENABLE function controls the device, turns off the GATEx, and resets a fault, but there is still power to drive the internal power-good circuitry. Because voltage is applied to the VREG output, the internal circuitry still has power when disabled, and the normal quiescent current of 1 mA max for Ii(IN1) and 200 μA max for Ii(IN2) applies.

With VREG connected to VIN1, the power-good circuitry is powered anytime with VIN1>1.1 V. This means that the minimum VIN1 input for valid PWRGDx is 1.1 V. Power good is low whenever VREG < UVLO.

The state of the ENABLE input and UVLO determines the state of the PWRGD outputs when VREG=VIN1. If the part is disabled or below UVLO turnon, the PWRGD outputs are both forced low regardless of the voltage present on VSENSEx. This is described in Table 3.

<table>
<thead>
<tr>
<th>STATE</th>
<th>UVLO</th>
<th>VSENSE1</th>
<th>VSENSE2</th>
<th>PWRGD1</th>
<th>PWRGD2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enabled or disabled</td>
<td>Below turn on</td>
<td>Don’t care</td>
<td>Don’t care</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Disabled</td>
<td>Above turn on</td>
<td>Don’t care</td>
<td>Don’t Care</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Enabled</td>
<td>Above turn on</td>
<td>&gt; 1.23 V</td>
<td>&lt; 1.23 V</td>
<td>Open Drain</td>
<td>Low</td>
</tr>
<tr>
<td>Enabled</td>
<td>Above turn on</td>
<td>&lt; 1.23 V</td>
<td>&gt; 1.23 V</td>
<td>Low</td>
<td>Open Drain</td>
</tr>
</tbody>
</table>

Power good is normally used to tell the system when the voltage after the driven MOSFET is within an acceptable range. However, the power-good VSENSE inputs are not dedicated to monitoring just the output voltage. This circuit can be used to monitor any system voltage.

A voltage other than the OUT1 and OUT2 can be sensed with the internal power-good comparators. The voltage applied to the VSENSE inputs must be less than the applied VIN1 to avoid parasitic conduction in the device. The PWRGD outputs work as shown in Table 3 when sensing a voltage other than OUT1 or OUT2.

3.3 Load Sequencing

The PWRGDx outputs may also be used to control the turnon of a downstream converter or linear regulator. It is desirable to allow the hot-swap controller to go through its start-up sequence before any transient loads like a converter are applied. When PWRGDx is configured to indicate valid OUTx (VSENSEx monitoring OUTx), then PWRGDx can provide an enable signal to the load converter or regulator. If the load converters have an active low enable input, the PWRGDx signal must be inverted.

When VREG=VIN1, the state of device enable and UVLO controls the PWRGD outputs, so that disabling the controller, or VIN1 being below the UVLO turnon, forces the load converters to turn off also.

Figure 4 represents a Power Trends PTH03050W 3.3-V to 0.8-V, 6-A module being controlled by both power-good outputs. In this configuration, the module will not start until both the OUT1 of 5 V and the OUT2 of 3.3 V are within their operating limits and the TPS23xx device is enabled. The power-good threshold for OUT1 is set for 4.5 V, and the OUT2 is set for 3 V. The module minimum operating input voltage is 2.95 V; so, it will not start until its input, OUT2, is above 3 V, determined by PG2, and OUT1 is above 4.5 V, determined by PG1.

The PTH03050W inhibit input can only be controlled by an open-drain active pulldown because the module provides the pullup mechanism internally. When using the inhibit or enable input on a converter that does not have an internal pullup, an external pullup is required because the power-good outputs are open drain.
3.4 Gate Output Voltage

VREG is used as the source for the charge pump that creates the gate drive voltage to turn on the external power MOSFETs. With VREG connected to VIN1, the charge pump operates directly from the VIN1 input voltage and not a regulated lower voltage. This allows the voltage applied to the gates of external power MOSFETs, from GATE1 and GATE2, to vary slightly. Table 4 shows these variations for GATE1, and Table 5 shows GATE2 variations.

Table 4. GATE1

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{G(GATE1_3V)}$</td>
<td>Gate voltage $I_{GATE1}=500 \text{ nA, DISCH1 open}$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{G(GATE1_4.5V)}$</td>
<td>$V_{(IN1)}=3 \text{ V}$</td>
<td>9</td>
<td>11.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{G(GATE1_10.8V)}$</td>
<td>$V_{(IN1)}=4.5 \text{ V}$</td>
<td>10.5</td>
<td>14.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{(IN1)}=10.8 \text{ V}$</td>
<td>16.8</td>
<td>21</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 5. GATE2

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{G(GATE2_3V)}$</td>
<td>Gate voltage $I_{GATE2}=500 \text{ nA, DISCH2 open}$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{G(GATE2_4.5V)}$</td>
<td>$V_{(IN2)}=3 \text{ V}$</td>
<td>9</td>
<td>11.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{(IN2)}=4.5 \text{ V}$</td>
<td>10.5</td>
<td>14.7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
The data sheet shows VGATE for VIN1=3 V, 4.5 V and 10.8 V. Therefore, designers should use the 3-V and 4.5-V data when designing with VREG connected to VIN1 in a 3.3-V/5-V system.

A VIN1 of 5 V provides a higher gate voltage to drive the MOSFETs, allowing better saturation characteristics. A VIN1 of 3.3 V works just as well considering the preceding guidelines.

3.5 **FAULT Output**

Connecting VREG to VIN1 has no effect on the FAULT output functionality. See the device data sheets (SLVS265, SLVS275) for details of the FAULT functionality.

4 **Conclusion**

Connecting VREG to VIN1 increases the flexibility of the TPS2300/01/10/11 dual hot-swap controllers when used in a lower voltage 5-V and 3.3-V system. Although common design practice uses the highest voltage, 5 V, for VIN1 and the lower voltage, 3.3 V for VIN2, the 3.3-V source can also be used for VIN1 with VIN2, using 5 V. Considerations must be observed with either method, but benefits can be obtained with both methods.

Advantages of connecting VREG to VIN1.
1. The device internal circuits remain powered during disable, allowing the PWRGDx outputs to be driven during device disable.
2. The VREG 0.1-V dropout variation is removed, so that the UVLO threshold is more accurate.
3. Eliminates VREG decoupling capacitor
4. Device disable forces the state of the power-good outputs to be LOW when the part is disabled, rather than being at high impedance. This can be beneficial for system operation.

Possible undesirable consequences of connecting VREG to VIN1
1. The operating current when disabled will no longer be the standby current of 5 µA maximum. It will be the normal operating current of 1 mA max, 500 µA typical on I\textsubscript{(I[IN1])}, and 200 µA max, 75 µA typical for I\textsubscript{(I[IN2])}.
2. VIN1 is limited to 5.5 V to prevent damage to the internal circuitry powered by VREG.
3. Device disable forces the state of the power-good outputs to be low regardless of the voltage present on VSENSE.

4.1 **References**
1. **TPS2300/01, Dual Hot-Swap Controllers With Independent Circuit Breaker and Power-Good Reporting** data sheet (SLVS265)
2. **TPS2310/11, Dual Hot-Swap Controllers With Independent Circuit Breaker and Power-Good Reporting** data sheet (SLVS275)
3. **PTH03050W, 6-A, 3.3-V Input Non-Isolated Wide-Output Adjust Power Module** data sheet (SLTS212)
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