ABSTRACT
This document is provided as a supplement to the DRV8800/01 datasheet. It details the hardware implementation of the DRV8800 or the DRV8801 devices connected in parallel for an effective increase in current handling capability.

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1 Introduction

The DRV8800 and DRV8801 devices are single H Bridge power stages designed to drive DC motors requiring up to 2.8 A of current. In order to provide greater system design flexibility and address the many DC motor applications that require currents exceeding the 2.8 A a single device can not provide, it is sometimes desirable to have larger current delivery capability in order to quickly accelerate to the desired speed or simply gain the torque response.

A technique is offered in which multiple DRV8800 or DRV8801 devices are connected in parallel, thereby effectively increasing the current available to drive the motor. With said technique, various driver chips are meant to share the increased load. This application note details pertinent connections as well as external components needed to safely connect the multiple devices together and drive larger inductive loads.

2 Block Diagrams

Connecting multiple DRV8800 or DRV8801 devices in parallel requires certain pins to be tied together across devices, whereas the remaining pins can be connected on an individual basis.

**Note:** It is not recommended that one connect a DRV8800 in parallel with a DRV8801. Only place like devices in the configuration outlined in this document.

2.1 Parallel Connections

Figure 1 shows the signals that need to be connected together. These are:

ENABLE, PHASE, MODE 1 and MODE 2 (on the DRV8801), nSLEEP, OUT+, OUT-, SENSE, VM and GND.

![Figure 1. Functional Block Diagram (Connected Signals)](image-url)
2.2 Non-Parallel Connections

Figure 2 shows the signals that should not be connected together and will be driven on an individual basis. These are:

VCP, CP1, CP2, and VPROPI (on the DRV8801)

Figure 2. Functional Block Diagram (Individual Signals)

2.3 Wiring nFAULT as Wired OR

Since nFAULT is an open drain output, multiple nFAULT outputs can be paralleled with a single resistor. The end result is a wired OR configuration. When any individual nFAULT output goes to a logic low, the wired OR output will go to the same logic low. There is no need to determine which device signaled the fault condition, as once they are connected in parallel they function as a single device.

Figure 3. nFAULT as Wired OR
3 Electrical Considerations

3.1 Device Spacing

It is recommended that devices be connected as close as possible and with trace lengths as short as possible. Doing this minimizes the potential of generating timing differences between devices. Although it may seem like a harmful situation for the power stage, the DRV8800 and DRV8801 devices contain enough protection to effectively deal with enable time skews from device to device. This consideration focuses on motion quality, as total current needed for acceleration and proper speed control will only be available when all power stages are brought online.

3.2 Recirculation Current Handling

During recirculation, it is not possible to synchronize all devices connected in parallel so that the current is equally distributed. Also, during the asynchronous portion of the current decay, the body diode with the lowest forward voltage will start conducting and sink all of the current. Said body diode is not meant to handle the new increased current capacity and will be severely affected if allowed to sink current of said magnitude.

In order to assure proper operation when devices are connected in parallel, it is imperative that external Schottky diodes be used. These Schottky diodes will conduct during the asynchronous portion of the recirculation mode and will sink the inductive load current until the respective FET switches are brought online.

Schottky diodes should be connected as shown in Figure 4.

![Figure 4. Schottky Diodes Connection](image)

3.3 Sense Resistor Selection

Selection of the SENSE resistor follows same guidelines as outlined in the datasheet. Specifically, \( I_{\text{TRIP}} \) will be configured according to Equation 1.

\[
I_{\text{TRIP}} = \frac{500 \, mV}{R_{\text{SENSE}} \, \Omega}
\]  

(1)

As the goal of this configuration is to evenly distribute the current load across multiple devices, the SENSE resistor should be the same for each device connected in parallel. It is not recommended to have devices configured to different \( I_{\text{TRIP}} \) settings.
Connection of the SENSE resistors should be as shown in Figure 5.

![Figure 5. SENSE Resistors Connection](image)

3.4 Maximum System Current

The idea behind placing multiple DRV8800/01 devices in parallel is to increase maximum drive current. At first glance, it may seem that the new increased $I_{\text{TRIP}}$ setting is given by Equation 2.

$$\text{System } I_{\text{TRIP}} = (I_{\text{TRIP}} \times N)$$

Where:

- $N$ is the number of DRV8800/01 devices connected in parallel.
- $I_{\text{TRIP}}$ is the individual $I_{\text{TRIP}}$ value per device.

However, although in theory accurate, due to tolerances in internal SENSE amplifier/comparator circuitry, the system $I_{\text{TRIP}}$ should be expected to be less than the addition of all the individual $I_{\text{TRIP}}$. The reason for this is that as soon as one of the devices senses a current for which the H Bridge should be disabled, the remaining devices will end up having to conduct the same current but with less capacity. Therefore, remaining devices are expected to get disabled shortly after.

A good rule of thumb is to expect 90% of the theoretical maximum.

By way of example, if the system level requirements indicate that 6 A of current are required to meet the motion control requirements, then:

$$6 \text{ A} = (2.8 \text{ A} \times 0.9)N$$

$$N = (6 \text{ A}) / (2.8 \text{ A} \times 0.9)$$

$$N = 2.38$$

In this example, three DRV8800/01 devices would be required to safely meet the needs of the system.
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