ABSTRACT
This document describes a reference design for multifaceted reflector MR-16 LED lighting by using the TPS40211 to construct a SEPIC converter. This driver provides 700 mA to a string of three white LEDs and has the capability to operate with 12 Vac or 12 Vdc. The TPS40211 has been selected for SEPIC application because it offers many advantages – long lifetime as the discard of E-cap in the design and good performance in power factor. This document presents a thorough analysis of SEPIC converter operation and performance along with design optimization guidelines. Experimental results obtained on 10-V/700-mA MR-16 lighting are provided.
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1 Introduction

This document provides the detail description of the implementation of the MR-16 LED lighting design by using the TPS40211 dc/dc controller. The block diagram of a 10-V, 700-mA, MR-16 LED lighting system is shown in Figure 1. The input voltage source of the LED driver can be supplied from a 12-Vdc input or a 12-Vac input, which is converted from a universal ac input via an electronic transformer, respectively. In addition, in order to keep the lumen of LED constant, the lighting system of the MR-16 is made of a constant current control scheme for the feedback loop circuit.

![Figure 1. Block Diagram of 10-V, 700-mA, MR-16 LED Lighting System](a) MR-16 LED Lamp with Electronic Transformer (b) System Block Diagram

2 Features

- Power driver without E-Cap design
- Longer lifetime of LED lamp
- Power factor higher than 0.9
- Compatible with 12-Vac electronic transformers without glitter
- Output current accuracy less than 1%
- Improve input inrush current
- OVP, OCP, and SCP protection
3 Application Schematic

Figure 2. MR-16 Design Example – I/P: 12 Vdc/12 Vac, O/P: 10-V at 700-mA LED Driver
4 Basic Operation

The SEPIC converter topology shown in Figure 3 consists of an input capacitor (C_{IN}), output capacitor (C_{OUT}), coupled inductors (L1, L2), ac coupling capacitor (C_p), power MOSFET (Q1), and freewheel diode (D1). The SEPIC converter is operated in the continuous conduction mode (CCM) during the switching-on period shown in Figure 6. The SEPIC converter is operated in the continuous conduction mode (CCM) during the switching-off period shown in Figure 7. The waveforms of the SEPIC converter switching voltage and current are shown in Figure 4 and Figure 5, respectively.

![Figure 3. Simple Circuit Diagram of SEPIC Converter](image)

![Figure 4. SEPIC Component Voltages During CCM](image)
4.1 During Switching Turnon

During the switch (Q1) ON time, the voltage across both inductors is equal to $V_{IN}$. When the switch is ON, capacitor $C_p$ is connected in parallel with $L_2$. The voltage across $L_2$ is the same as the capacitor voltage, $-V_{IN}$. Diode $D_1$ is the reverse bias, and the load current is being supplied by capacitor $C_{OUT}$. During this period, energy is being stored in $L_1$ from the input and in $L_2$ from $C_p$. 
During Switching Turnoff

During the switch (Q1) OFF time, the current in L1 continues to flow through Cp and D1, and then into C\text{OUT}. In the meantime, the Cp is charged and ready for the next cycle. The current in L2 also flows into C\text{OUT} and the load, ensuring that C\text{OUT} is ready for the next cycle.

5 SEPIC Converter Design Guide

This SEPIC converter uses current mode control to simplify the stabilization of the control loop. Peak current in the FET is limited by the pulse current limiting of the TPS40211. Switching frequency is 560 kHz, allowing low output current handling and low output ripple with small inductors and capacitors while remaining in the continuous inductor current mode. When the converter is operated in continuous conduction mode and the duty cycle is 50% or greater, the remedy for this condition is to apply a compensating ramp from the oscillator to the signal going to the pulse width modulator.

5.1 Duty Cycle Consideration

Assuming 100% efficiency, the duty cycle, D, for a SEPIC converter operated in CCM is given by

- Calculate minimum duty cycle

\[
D_{\text{min}} = \frac{V_{\text{OUT}} + V_{\text{D}}}{V_{\text{In}} + V_{\text{OUT}} + V_{\text{D}}}
\]  

(1)

where \(V_{\text{D}}\) is the forward voltage drop of the Schottky diode D1.

- Calculate maximum duty cycle

\[
D_{\text{max}} = \frac{V_{\text{OUT}} + V_{\text{D}}}{V_{\text{In}} + V_{\text{OUT}} + V_{\text{D}}}
\]  

(2)
5.2 Inductor Selection

The inductance ripple current is to allow approximately 20% to 40% of the maximum input current at the minimum input voltage. The ripple current is given by

\[ \Delta I = \frac{I_{OUT} \times (V_{OUT} + V_D)}{V_{INmin} \times \eta} \times 40\% \]  

(3)

To account for load transients, the coupled inductor's saturation current rating needs to be at least 20% higher than the steady-state peak current in the high-side inductor, is given by

\[ I_{L1peak} = \frac{I_{OUT} \times (V_{OUT} + V_D)}{V_{INmin} \times \eta} \times \left[ 1 + \frac{40\%}{2} \right] \]  

(4)

\[ I_{L2peak} = I_{OUT} + \frac{\Delta I}{2} \]  

(5)

Ideally, a single core wound the same number of windings; the mutual inductance forces the ripple current to be split equally between the two coupled inductors. In a real coupled inductor, because the inductors do not have equal inductance, the ripple currents are not exactly equal. Regardless, for a desired ripple-current value, the inductance required in a coupled inductor is estimated to be half of what is needed. With two separate inductors, the inductance is given by

\[ L_1 = L_2 > \frac{V_{INmin} \times D_{max}}{2/s \times \Delta I_L} \]  

(6)

The converter is ensured to be operated in a continuous conduction mode (CCM) at light load; the inductor value L1 and L2 is given by

\[ L_1 = L_2 > \frac{V_{INmax} \times D_{min}}{f/s \times I_{OUT} \left( \frac{V_{OUT} + 1}{V_{INmax}} \right)} \]  

(7)

5.3 Output Capacitor Selection

When the Q1 is on, the output capacitor must provide the load current. The output capacitor, therefore, must have enough capacitance. In this EVM design, the ceramic capacitors are used, the ESR can be ignored and the equation is given by

\[ C_{OUT} \geq \frac{I_{OUT} \times D_{max}}{\Delta V_{RPL} \times f/s} \]  

(8)

where \( \Delta V_{RPL} \) is the output voltage ripple which is desired by the requirement of the design.

5.4 Input Capacitor Selection

The input capacitor can be very small, because of the filtering properties of the SEPIC topology. Usually, \( C_{IN} \) can be ten times smaller than \( C_{OUT} \).

\[ C_{IN} = \frac{C_{OUT}}{10} \]  

(9)

5.5 Coupling Capacitor Selection

The coupling capacitor, \( C_P \), sees large RMS current relative to the output power:
The coupling capacitor $C_P$ is given by

$$C_P = \frac{I_{OUT} \times D_{\text{max}}}{\Delta V_{CP} \times f_s}$$  \hspace{1cm} (11)$$

where $\Delta V_{CP}$ is the ripple voltage which is across $C_P$.

The maximum voltage across $C_P$ is $V_{IN}$.

### 5.6 Power MOSFET Consideration

This topology places higher stresses on both the Q1 and the D1 than do other PWM topologies. The power MOSFET, Q1, must be carefully selected for handling the peak voltage and current. The current rating of the power FET determines the SEPIC converter’s maximum output current. The maximum voltage across the drain to the source is $V_{IN_{\text{max}}} + V_{OUT}$. The peak current is given by:

$$I_{Q1\text{peak}} = \frac{I_{OUT} \times (V_{OUT} + V_D)}{V_{IN_{\text{min}}} \times \eta} + I_{OUT} + \Delta I$$  \hspace{1cm} (12)$$

The RMS current of the Q1 is given by

$$I_{Q1\text{rms}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN_{\text{min}}} \times \eta \times \sqrt{D_{\text{max}}}}$$  \hspace{1cm} (13)$$

### 5.7 Output Diode Consideration

The output diode D1 must be able to handle the same peak current as Q1, $I_{Q1\text{peak}}$, do. The diode must also be able to withstand a reverse voltage greater than the maximum voltage of Q1 to account for transients and ringing. Because the average diode current is the output current, the diode’s package must be capable of dissipating up to $P_{D1} = I_{OUT} \times V_D$.

### 6 TPS40211 Design Guide

#### 6.1 Current Sense and Overcurrent

![Figure 8. Current Sense Circuit](image)

The TPS40210 and TPS40211 are current mode controllers and use resistors in series with the source
terminal power FET to sense current for both the current mode control and the overcurrent protection. The device enters a current limit state, if the voltage on the ISNS pin exceeds the current limit threshold voltage $V_{\text{ISNS}}$ from the electrical specifications table. When this happens, the controller discharges the SS capacitor through a relatively high impedance, and then attempt to restart. The load current over-current threshold is set by proper choice of $R_{\text{ISNS}}$. If the converter is operated in discontinuous mode, the current sense resistor is given by

$$R_{\text{ISNS}} = \frac{f_s \times L1 \times V_{\text{ISNS}}}{\sqrt{2 \times L1 \times f_s \times V_{\text{OUT}} + V_D - V_{\text{INmin}}}}$$

If the converter is operated in continuous conduction mode, the current sense resistor is given by

$$R_{\text{ISNS}} = \frac{V_{\text{ISNS}}}{1 - D_{\text{max}}} + \frac{D_{\text{max}} \times V_{\text{INmin}}}{2 \times f_s \times L1}$$

(14)

(15)

6.2 Soft-Start Capacitor

Because $V_{\text{DD}} > 8$ V, the soft-start capacitor is given by

$$C_{\text{SS}} = 20 \times T_{\text{SS}} \times 10^{-6}$$

(16)

where $T_{\text{SS}}$ is a timing of soft-start.

6.3 Setting the Oscillator Frequency

The oscillator frequency is determined by a resistor and capacitor connected to the RC pin of the TPS40211. The capacitor is charged to a level of approximately $V_{\text{DD}}/20$ by current flowing through the resistor and is then discharged by a transistor internal to the TPS40211. The required resistor for a given oscillator frequency is given by

$$R_T = \frac{1}{5.8 \times 10^{-8} \times f_s \times C_T + 8 \times 10^{-10} \times f_s^2 + 1.4 \times 10^{-7} \times f_s - 1.5 \times 10^{-4} + 1.7 \times 10^{-6} \times C_T - 4 \times 10^{-9} \times C_T^2}$$

(17)

Where:

- $R_T$ is the timing resistance in kΩ
- $f_s$ is the switching frequency in kHz
- $C_T$ is the timing capacitance in pF

For most applications, a capacitor is in the range of 68 pF to 120 pF gives the best results. Resistor values must be limited to between 100 kΩ and 1 MΩ as well.
6.4 Current Feedback Resistor

The only difference between the TPS40210 and the TPS40211 is the reference voltage that the error amplifier uses to regulate the output voltage. The TPS40211 uses a 260-mV reference and is intended for applications where the output is actually a current instead of a regulated voltage. The current in the LED string is set by the choice of the resistor \( R_{FB} \) as shown in the following equation:

\[
R_{FB} = \frac{V_{FB}}{I_{OUT}}
\]

(18)

Where \( V_{FB} \) is the reference voltage for the TPS40211 in V (0.26 V typ)

7 Design Example

Design Specifications

1. Allowed maximum input voltage (V): \( V_{IN_{max}} = 12 \text{ V} \)
2. Allowed minimum input voltage (V): \( V_{IN_{min}} = 5 \text{ V} \)
3. LED series number: \( S_{LED} = 3 \)
4. LED voltage drop: \( V_{LED} = 3.2 \text{ V} \)
5. Output current: \( I_{OUT} = 700 \text{ mA} \)
6. Converter efficiency: \( \eta = 90\% \)
7. Switching frequency: \( f_s = 560 \text{ kHz} \)

Design Results

A. SEPIC Converter Design Guide

Inductance of \( L_1 \) and \( L_2 \): \( L_1 = L_2 > L_{CCM} \)

Output capacitance:

Input capacitance:

Coupling capacitance:

MOSFET current and voltage stress

Voltage stress:

Current stress:

Diode current and voltage stress

Voltage stress:

Current stress:

B. TPS40211 Design Guide

Current sense resistance:

Soft-Start capacitance (F):

\[ R_{ISNSCCM} = 0.044 \Omega \]
\[ R_1 = 50 \text{ m\Omega} \text{ selected} \]
\[ C_{SS} = 1 \times 10^{-7} \text{ selected} \]
Current FB resistance:

R-C Oscillator
Resistance $R_T$ (kΩ)

Capacitance $C_T$ (pF):

R$_{FB}$ = 0.371 Ω
R6=R7 = 0.7 Ω selected

$R_T$ = 402.411
R3 = 402 kΩ selected

$C_T$ = 68
C8 = 68 pF selected

8 Test Data

**12 V AC EFFICIENCY**

![Graph 1](#)

**12 V DC EFFICIENCY**

![Graph 2](#)

**OUTPUT CURRENT ACCURACY (12 V AC INPUT)**

![Graph 3](#)

**OUTPUT CURRENT ACCURACY (12 V DC INPUT)**

![Graph 4](#)
Figure 14. 12-Vac Input With ac Transformer

Figure 15. CH2: Input Current, CH4: Input Voltage After Rectifier

Figure 16. CH2: Output Current, CH4: Input Voltage After Rectifier
9 EVM Assembly Drawing and Layout

A two-layer, printed-circuit board (PCB) was designed using the top and bottom layers. The dimensions of PCB are 12mm × 10mm, and the other PCB diameter is 21mm, with a design goal of maintaining all components to be a height less than 12mm that is measured from the surface of the top layer. Figure 20 shows the top-side driver photo placement for the EVM, and all other layers are also shown in Figure 21 through Figure 25, respectively.
10 Bill of Materials

Table 1 lists the EVM components as configured corresponding to the schematic shown in Figure 2. Part types and manufacturers can be modified according to specific application requirements.
Table 1. Bill of Materials

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11 References

1. Versatile Low Power SEPIC Converter Accepts Wide Input Voltage Range design note DN-48 (SLUA158)
2. Designing DC/DC Converters Based on SEPIC Topology, Texas Instruments Analog Applications Journal, 4Q 2008
3. TPS40211, 4.5-V to 52-V Input Current Mode Boost Controller data sheet (SLUS772)
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