Application Report
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Compensating the Current-Mode-Controlled Boost Converter

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ABSTRACT

This application report summarizes one method for compensating a current-mode-controlled boost. A detailed description of both the power stage and the feedback network is provided. The design procedures are explained step by step. A design example using TPS61175 is provided. Similar design steps are used for the TPS61199 as well.

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1 Simplified Small Signal Model

Figure 1 shows a simplified block diagram of a current-mode boost converter with a transconductance amplifier providing the feedback.

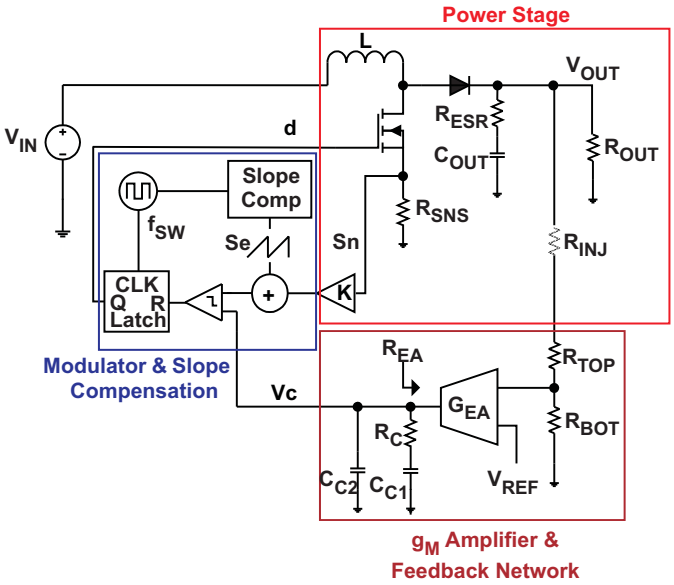

Figure 1. Simplified Diagram of a Current-Mode Boost Converter with g_M Amplifier

With inductor current information fed back by R_{SNS} (and possibly gained by factor K) as well as output voltage feedback, this boost converter's inductor and switches effectively combine into a current source driving an RC load. By removing the inductor, the small-signal, control-loop model of the power stage reduces from a two-pole system, created by L and C_{OUT}, to a single-pole (f_P) system, created by R_{OUT} and C_{OUT}. The single-pole system is easily used with Type-II compensation.

The single-pole system only holds true if the slope of the external compensation signal, Se, is not too large in relation to the ramp sensed across R_{SENSE}, Sn or the natural slope. If the Se slope dominates Sn, for example, when the inductance is oversized in order to give ripple current much smaller than the recommended 0.2-0.4 times the average input current, then the converter begins behaving more like a voltage-mode converter and the full model, included in Appendix A, must be used.

Regardless of which model is used, the right-half-plane zero (f_{RHPZ}), created by lack of continuous current flow to the output, is still present.

Including the slope compensation, the new power stage small-signal model is presented mathematically as follows:

$$G_{PS}(S) = \frac{R_{OUT} * (1 - D)}{2 * R_{SENSE}} * \frac{(1 + \frac{S}{2\pi * f_{ESR}})(1 - \frac{S}{2\pi * f_{RHPZ}})}{1 + \frac{S^2}{2\pi * f_P}} * He(s) \quad (1)$$

Where D is the duty cycle and the single pole is:

$$f_P = \frac{2}{2\pi * R_{OUT} * C_{out}} \quad (2)$$

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi * R_{ESR} * C_{out}} \quad (3)$$

For a boost converter having multiple, identical output capacitors in parallel, simply combine the capacitors and ESR in parallel and use the result in Equation 2 and Equation 3. For boost converters with ceramic capacitor(s) in parallel with a much larger, high-ESR capacitor, use the total capacitance in parallel for C_{OUT} in Equation 2 but only use the high-ESR capacitor's capacitance and ESR for Equation 3.

The right-hand plane zero is:

$$f_{RHPZ} = \frac{R_{out}}{2\pi * L} * (\frac{V_{IN}}{V_{out}})^2 \tag{4}$$

He(s) models the inductor current sampling effect as well as the slope compensation effect on the small-signal response.

$$He(s) = \frac{1}{1 + \frac{s * [(1 + \frac{Se}{Sn}) * (1 - D) - 0.5]}{f_{SW}} + \frac{s^2}{(\pi * f_{SW})^2}} \tag{5}$$

The equation for Se is unique to each IC and is found in the IC's datasheet. Equation 6 gives the typical equation for Sn regarding a peak current mode converter.

$$S_n = \frac{V_{IN}}{L} * R_{SNS} \tag{6}$$

The natural slope may change for other types of current mode converters.

Figure 3 in the design example section shows a bode plot of a typical CCM boost converter power stage, assuming the ESR pole is at a very high frequency.

Equation 7 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA} = G_{EA} * R_{EA} * \frac{R_{BOT}}{R_{BOT} + R_{TOP}} * \frac{1 + \frac{S}{2\pi * f_z}}{(1 + \frac{S}{2\pi * f_{P1}}) * (1 + \frac{S}{2\pi * f_{P2}})} \tag{7}$$

Where G_{EA} and R_{EA} are the error amplifier's transconductance and output resistance.

$$f_{P1} = \frac{1}{2\pi * R_{EA} * C_{C1}} \tag{8}$$

$$f_{P2} = \frac{1}{2\pi * R_C * C_{C2}} \text{ (Optional)} \tag{9}$$

C_{C2} is optional and is modeled as 10-pF stray capacitance.

and

$$f_Z = \frac{1}{2\pi * R_C * C_{C1}} \tag{10}$$

Figure 4 in the design example shows a typical shape of a bode plot for transfer function $H_{EA}(s)$ with Type-II compensation components.

2 Design Steps

The steps to compensate the loop are as follows:

1. Choose the desired loop crossover frequency, fc

   The higher in frequency that the loop gain stays above zero before crossing over, the faster the loop response is and, therefore, the lower the output voltage droops during a step load. It is generally recommended that the loop-gain crossover point is no higher than the lower of either 1/5 of the switching frequency, f_{SW}, or 1/3 of the RHPZ frequency, f_{RHPZ}. It is also recommended to cross over at a frequency where the power stage gain is decreasing at approximately a -20 dB/decade slope (after the dominant pole and well before the effects of an RHPZ).

   The size of the output capacitor plays a significant role in how wide the loop bandwidth is. Once the minimum capacitance is met, meeting the output ripple specification, Equation 11 is used to estimate the capacitance needed to meet the application's load transient requirement for the maximum voltage dip (V_{TRAN}) after a given load step (ΔI_{TRAN}).

$$C_{out} = \frac{\Delta I_{TRAN}}{2\pi * f_C * V_{TRAN}} \tag{11}$$

2. Properly size the compensation resistor, Rc

   By placing f_Z below f_C, for frequencies above f_C, Rc| $|R_{REA}$ ~= R_C and so $R_C \times G_{EA}$ sets the compensation gain. Setting the compensation gain, $K_{COMP\text{-}dB}$, at f_C , results in the total loop gain, T(s) = $G_{PS}(s) \times H_{EA}(s) \times He(s)$ being zero at f_C. Therefore, to approximate a single-pole roll-off up to f_{P2}, rearrange Equation 12 to solve for R_C so that the compensation gain, $K_{COMP\text{-}dB}$, at f_C is the negative of the gain, $K_{PW\ -dB}$, read at frequency f_C for the power stage bode plot or more simply

$$K_{COMP-dB}(f_c) = 20 * \log(G_{EA} * R_C * \frac{R_{BOT}}{R_{BOT} + R_{TOP}}) = -K_{PW-dB}(f_c) \tag{12}$$

3. Properly size the compensation capacitor, C_{C1}

   Compensation capacitor C_{C1} is sized so that $f_Z \approx f_C/10$ and optional $f_{P2} > f_C \times 10$

4. Optionally, size the compensation capacitor, C_{C2}.

   Equation 9 is for a pole produced by RC and C_{C2}. This pole may be necessary to ensure that the gain continues to roll off after the crossover frequency. Alternatively, for boost circuits with high ESR output capacitors, and therefore a low-frequency ESR zero per Equation 3, this pole is useful for canceling unhelpful effects of the ESR zero.

The preceding steps lead to a loop with a phase margin near 45 degrees. Lowering R_C, while keeping fz ≈ f_{BW}/10, increases the phase margin without significantly changing the gain and therefore increases the time it takes for the output voltage to settle following a step load.

3 Design Example using the TPS61175

Figure 2 shows the EVM schematic and Table 1 gives the specifications for the design example. In order to meet the transient requirement, the output capacitance value may need to changed.

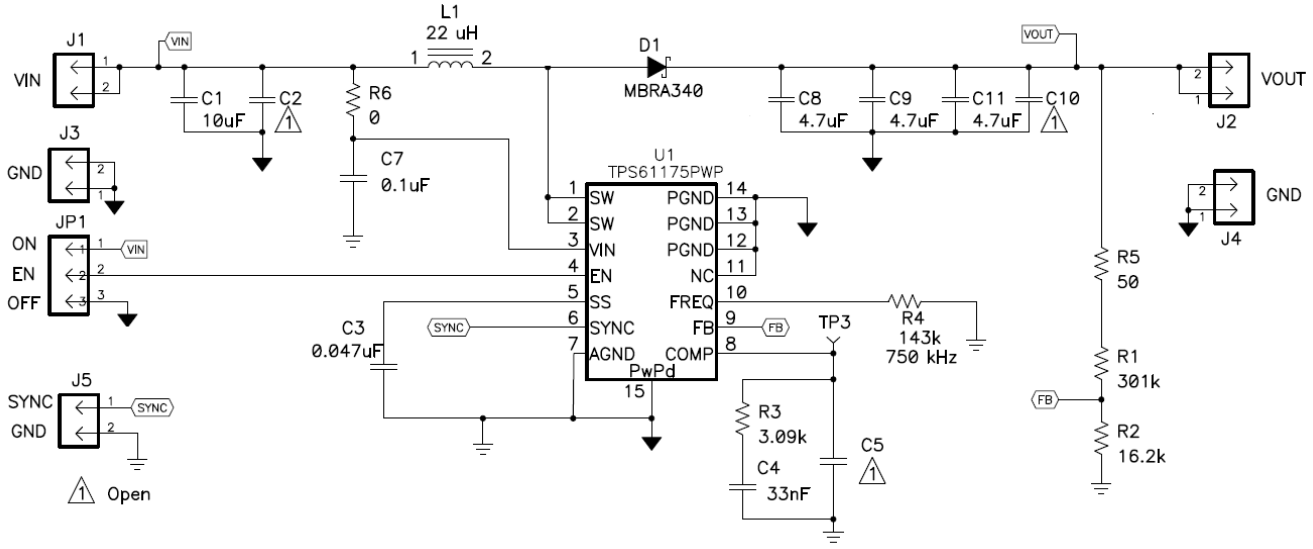

Figure 2. TPS61175 Design Example Schematic

Table 1. TPS61175EVM-326 Performance Specification Summary for V_{IN} = 12.0 V

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input Voltage			12		V
f_{SW}	Switching Frequency			750		kHz
OUTPUT CHARACTERISTICS						
V_O	Output Voltage		23	24	25	V
I_O	Output Current		1		1.2	A
TRANSIENT RESPONSE						
ΔI_{TRAN}	Load Step			0.35		A
$\Delta_{IO}/\Delta T$	Load slew rate			9		A/µs
ΔV_{TRAN}	V_O undershoot			500		mV
t_S	Settling time			300		µs

Equation 13 and Equation 14 give Sn and Se for the TPS61175.

$$S_n = \frac{V_{IN}}{L} * R_{SNS} = \frac{12V}{22\mu H} * 40m\Omega \quad (13)$$

$$S_e = \frac{\frac{0.32V}{R_4}}{16*(1-D)*6pF} + \frac{0.5uA}{6pF} \quad (14)$$

Where R_4 is the frequency setting resistor.

1. Choose the desired loop crossover frequency, fc.

One fifth of the switching frequency is

$$\frac{f_{SW}}{5} = \frac{750kHz}{5} = 150kHz \tag{15}$$

f_{RHPZ} is calculated using Equation 4

Where:

$$R_{OUT} = \frac{V_{OUT}}{I_{OUT}} = \frac{24V}{1.2A} = 20\Omega \tag{16}$$

From Equation 4

$$f_{RHPZ} = \frac{20}{2\pi * 22uH} * (\frac{12V}{24V})^2 = 36.2kHz \tag{17}$$

one-third of f_{RHPZ} is

$$\frac{f_{RHPZ}}{3} = \frac{36.2kHz}{3} = 12.1kHz \tag{18}$$

thus, try f_C = 10 kHz.

2. Find the output cap value using Equation 11

$$C_{out} = \frac{\Delta I_{TRAN}}{2\pi * f_C * V_{TRAN}} = \frac{350mA}{2\pi * 10kHz * 500mV} = 11.14\mu F \tag{19}$$

Three 4.7 µF capacitors in parallel yield a total of 14.7 µF for the output capacitance (C8, C9, and C11 in Figure 2)

3. Properly size the compensation resistor, R_C (R3 in Figure 2). Using MathCAD, plot the power stage, $G_{PS}(s)$, with R_{SENSE} = 40 mΩ (given in the datasheet)

from Equation 2

$$f_P = \frac{2}{2\pi * R_{OUT} * C_{out}} = \frac{2}{2\pi * 20\Omega * 3 * 4.7uF} = 1.1kHz \tag{20}$$

From Equation 4, f_{RHPZ} is 36.2 kHz. Neglecting the ESR zero produced by the ceramic output capacitors gives the plot found in Figure 3.

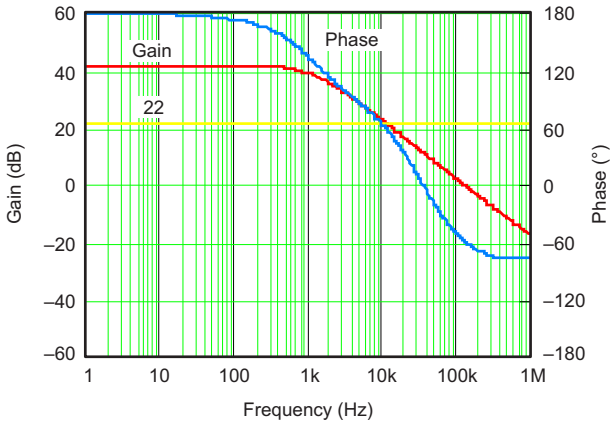

Figure 3. Simulated Bode Plot of Power Stage Gain and Phase

The crossover frequency, f_C, was chosen as 10 kHz and from Figure 3, K_{PW} (10 kHz) = 22 dB. With R_{TOP} = 301 kΩ, R_{BOT} = 16.2 kΩ (R1 and R2 respectively in Figure 2), and $G_{EA(TYP)}$ = 340 µmho, solving Equation 12 for R_C gives:

$$K_{COMP-dB}(f_c) = 20 * \log(G_{EA} * R_C * \frac{R_{BOT}}{R_{BOT} + R_{TOP}}) = -K_{PW-dB}(f_c) \Rightarrow \tag{21}$$

$$R_C = \frac{10^{\frac{K_{COMP-dB(fc)}}{20dB}}}{G_{EA} * \frac{R_{BOT}}{R_{BOT}+R_{TOP}}} = \frac{10^{\frac{-22}{20}}}{340umho * \frac{16.2k\Omega}{16.2k\Omega+301k\Omega}} = 4.57k\Omega \quad (22)$$

4. Properly size the compensation capacitor, C_{C1} (C4 in Figure 2).

   Solving Equation 10 for C_{C1} and setting $f_z = f_c/10 = 1$ kHz gives

$$C_{C1} = \frac{1}{2\pi * R_C * f_z} = \frac{1}{2\pi * 4.57k\Omega * 1kHz} = 34.82nF \Rightarrow 33nF \quad (23)$$

5. Optionally, size the compensation capacitor, C_{C2} (C5 in Figure 2)

   A stray capacitance of 10 pF is assumed for C5.

   Figure 4 displays the plot for the Type II compensated amplifier and Figure 5 shows T(s) = G_{PS}(s) × H_{EA}(s) × He(s) with R_C (R_3) reduced to 3.09 kΩ, getting closer to the desired 60 degree phase margin.

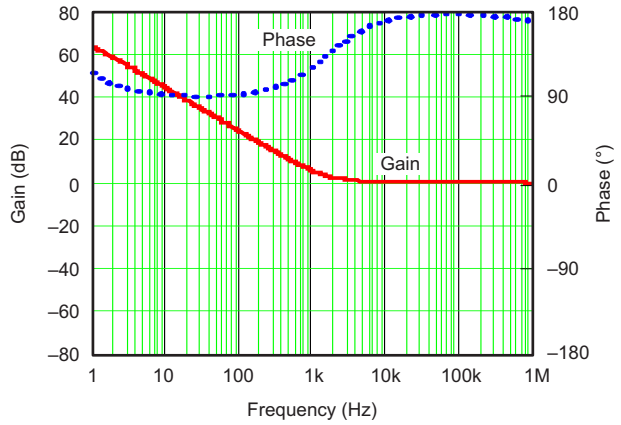

Figure 4. Simulated Bode Plot of the Type II Compensation (Including Feedback Network) for a g_m Error Amplifier

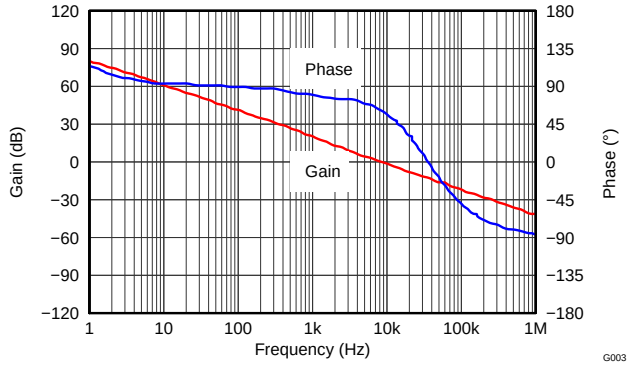

Figure 5. Modeled Bode Plot of the Total Open Loop

As Figure 6 shows, the measured loop compares favorably with the simulated loop.

Figure 6. Loop Gain and Phase

Appendix A Additional Data

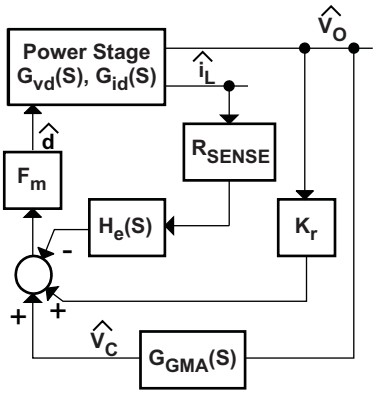

Figure 7. Full Model Diagram

$$G_{id}(s) = \frac{\frac{2V_O^3}{V_{IN}^2}\left(1 + \frac{R_O C_O}{2}s\right)}{1 + \frac{V_O^2 L}{V_{IN}^2 R_{OUT}}s + \frac{V_O^2 L C_O}{V_{IN}^2}s^2} \tag{24}$$

Where:

$$G_{PS}(s) = \frac{v_o}{v_c} = \frac{F_m G_{vd}(s)}{1 + F_m R_{SENSE} H_e(s) G_{id}(s) - F_m K_r G_{vd}(s)} \tag{25}$$

$$F_m = \frac{1}{(S_e + S_n)T_s} \tag{26}$$

$$G_{vd}(s) = \frac{\frac{V_O^2}{V_{IN}}\left(1 - \frac{V_O^2 L}{V_{IN}^2 R_O}s\right)(1 + R_{ESR} C_O s)}{1 + \frac{V_O^2 L}{V_{IN}^2 R_O}s + \frac{V_O^2 L C_O}{V_{IN}^2}s^2} \tag{27}$$

$$He(s) = 1 - \frac{T_S}{2}s + \frac{T_S}{\pi^2}s^2 \tag{28}$$

A.1 References

He, Dake, and R. M. Nelms, “Peak Current-Mode for a Boost Converter Using an 8-bit Microcontroller,” IEEE 34th Annual Power Electronics Specialist Conference 2, June 2003 Record, pp. 938–943.

Ridley, R. D., “Current-Mode Control Modeling,” *Switching Power Magazine*, 2006, pp. 1–12.

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