Compensating the Current-Mode-Controlled Boost Converter

Jeff Falin, Tahar Allag, Ben Hopf

Contents
1 Simplified Small Signal Model ................................................................. 2
2 Design Steps .......................................................................................... 4
3 Design Example using the TPS61175 ....................................................... 5
Appendix A Additional Data ....................................................................... 9

List of Figures
1 Simplified Diagram of a Current-Mode Boost Converter with \( g_m \) Amplifier ............................................. 2
2 TPS61175 Design Example Schematic .................................................. 5
3 Simulated Bode Plot of Power Stage Gain and Phase ............................. 6
4 Simulated Bode Plot of the Type II Compensation (Including Feedback Network) for a \( g_m \) Error Amplifier ............................................................ 7
5 Modeled Bode Plot of the Total Open Loop .......................................... 7
6 Loop Gain and Phase ............................................................................. 8
7 Full Model Diagram ............................................................................. 9

ABSTRACT
This application report summarizes one method for compensating a current-mode-controlled boost. A detailed description of both the power stage and the feedback network is provided. The design procedures are explained step by step. A design example using TPS61175 is provided. Similar design steps are used for the TPS61199 as well.
1 Simplified Small Signal Model

Figure 1 shows a simplified block diagram of a current-mode boost converter with a transconductance amplifier providing the feedback.

Figure 1. Simplified Diagram of a Current-Mode Boost Converter with $g_M$ Amplifier

With inductor current information fed back by $R_{SNS}$ (and possibly gained by factor $K$) as well as output voltage feedback, this boost converter’s inductor and switches effectively combine into a current source driving an RC load. By removing the inductor, the small-signal, control-loop model of the power stage reduces from a two-pole system, created by $L$ and $C_{OUT}$, to a single-pole ($f_P$) system, created by $R_{OUT}$ and $C_{OUT}$. The single-pole system is easily used with Type-II compensation.

The single-pole system only holds true if the slope of the external compensation signal, $S_e$, is not too large in relation to the ramp sensed across $R_{SENSE}$, $S_n$ or the natural slope. If the $S_e$ slope dominates $S_n$, for example, when the inductance is oversized in order to give ripple current much smaller than the recommended 0.2-0.4 times the average input current, then the converter begins behaving more like a voltage-mode converter and the full model, included in Appendix A, must be used.

Regardless of which model is used, the right-half-plane zero ($f_{RHPZ}$), created by lack of continuous current flow to the output, is still present.

Including the slope compensation, the new power stage small-signal model is presented mathematically as follows:

\[
G_{PS}(s) = \frac{R_{OUT} \cdot (1 - D)}{2 \cdot R_{SENSE}} \cdot \frac{(1 + \frac{S}{2\pi \cdot f_{ESR}})(1 - \frac{S}{2\pi \cdot f_{RHPZ}})}{1 + \frac{S^2}{2\pi \cdot f_p}} \cdot He(s) \tag{1}
\]

Where $D$ is the duty cycle and the single pole is:

\[
f_p = \frac{2}{2\pi \cdot R_{OUT} \cdot C_{OUT}} \tag{2}
\]

The zero created by the ESR of the output capacitor is:

\[
f_{ESR} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_{OUT}} \tag{3}
\]
For a boost converter having multiple, identical output capacitors in parallel, simply combine the capacitors and ESR in parallel and use the result in Equation 2 and Equation 3. For boost converters with ceramic capacitor(s) in parallel with a much larger, high-ESR capacitor, use the total capacitance in parallel for $C_{OUT}$ in Equation 2 but only use the high-ESR capacitor’s capacitance and ESR for Equation 3.

The right-hand plane zero is:

$$f_{RHPZ} = \frac{R_{\text{out}}}{2\pi * L} * \left(\frac{V_{\text{IN}}}{V_{\text{out}}}\right)^2$$  \hspace{1cm} (4)

$He(s)$ models the inductor current sampling effect as well as the slope compensation effect on the small-signal response.

$$He(s) = \frac{1}{s * [(1 + \frac{Se}{Sh}) * (1 - D) - 0.5]} + \frac{s^2}{(\pi * f_{SW})^2}$$  \hspace{1cm} (5)

The equation for $Se$ is unique to each IC and is found in the IC’s datasheet. Equation 6 gives the typical equation for $Sn$ regarding a peak current mode converter.

$$S_n = \frac{V_{\text{IN}}}{L} * R_{\text{SNS}}$$  \hspace{1cm} (6)

The natural slope may change for other types of current mode converters.

Figure 3 in the design example section shows a bode plot of a typical CCM boost converter power stage, assuming the ESR pole is at a very high frequency.

Equation 7 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA} = G_{EA} * R_{EA} * \frac{R_{BOT}}{R_{BOT} + R_{TOP}} * \frac{1 + \frac{S}{2\pi * f_z}}{(1 + \frac{2\pi * f_{p1}}{S}) * (1 + \frac{2\pi * f_{p2}}{S})}$$  \hspace{1cm} (7)

Where $G_{EA}$ and $R_{EA}$ are the error amplifier’s transconductance and output resistance.

$$f_{p1} = \frac{1}{2\pi * R_{EA} * C_{C1}}$$  \hspace{1cm} (8)

$$f_{p2} = \frac{1}{2\pi * R_C * C_{C2}} \text{ (Optional)}$$  \hspace{1cm} (9)

$C_{C2}$ is optional and is modeled as 10-pF stray capacitance.

and

$$f_z = \frac{1}{2\pi * R_C * C_{C1}}$$  \hspace{1cm} (10)

Figure 4 in the design example shows a typical shape of a bode plot for transfer function $H_{EA}(s)$ with Type-II compensation components.
2 Design Steps

The steps to compensate the loop are as follows:

1. Choose the desired loop crossover frequency, f_c

   The higher in frequency that the loop gain stays above zero before crossing over, the faster the loop response is and, therefore, the lower the output voltage droops during a step load. It is generally recommended that the loop-gain crossover point is no higher than the lower of either 1/5 of the switching frequency, f_{SW}, or 1/3 of the RHPZ frequency, f_{RHPZ}. It is also recommended to cross over at a frequency where the power stage gain is decreasing at approximately a -20 dB/decade slope (after the dominant pole and well before the effects of an RHPZ).

   The size of the output capacitor plays a significant role in how wide the loop bandwidth is. Once the minimum capacitance is met, meeting the output ripple specification, Equation 11 is used to estimate the capacitance needed to meet the application’s load transient requirement for the maximum voltage dip (\Delta V_{TRAN}) after a given load step (\Delta I_{TRAN}).

\[
C_{out} = \frac{\Delta I_{TRAN}}{2\pi f_c V_{TRAN}}
\]  

(11)

2. Properly size the compensation resistor, R_c

   By placing f_z below f_c, for frequencies above f_c, R_c | R_{REA} ∼ = R_c and so R_c \times G_{EA} sets the compensation gain. Setting the compensation gain, K_{COMP-dB}, at f_c, results in the total loop gain, T(s) = G_{PS}(s) \times H_E(s) \times He(s) being zero at f_c. Therefore, to approximate a single-pole roll-off up to f_{P2}, rearrange Equation 12 to solve for R_c so that the compensation gain, K_{COMP-dB}, at f_c is the negative of the gain, K_{PW-dB}, read at frequency f_c for the power stage bode plot or more simply

\[
K_{COMP-dB}(f_c) = 20 \log \left( G_{EA} \times R_c \times \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \right) = -K_{PW-dB}(f_c)
\]  

(12)

3. Properly size the compensation capacitor, C_{C1}

   Compensation capacitor C_{C1} is sized so that f_z ∼ = f_c/10 and optional f_{P2} > f_c \times 10

4. Optionally, size the compensation capacitor, C_{C2}

   Equation 9 is for a pole produced by RC and C_{C2}. This pole may be necessary to ensure that the gain continues to roll off after the crossover frequency. Alternatively, for boost circuits with high ESR output capacitors, and therefore a low-frequency ESR zero per Equation 3, this pole is useful for canceling unhelpful effects of the ESR zero.

   The preceding steps lead to a loop with a phase margin near 45 degrees. Lowering R_c, while keeping f_z ∼ = f_{SW}/10, increases the phase margin without significantly changing the gain and therefore increases the time it takes for the output voltage to settle following a step load.
3 Design Example using the TPS61175

Figure 2 shows the EVM schematic and Table 1 gives the specifications for the design example. In order to meet the transient requirement, the output capacitance value may need to be changed.

![Figure 2. TPS61175 Design Example Schematic](image)

### Table 1. TPS61175EVM-326 Performance Specification Summary for $V_{IN} = 12.0 \, \text{V}$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Input Voltage</td>
<td>12</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$f_{SW}$</td>
<td>Switching Frequency</td>
<td>750</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUTPUT CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{O}$</td>
<td>Output Voltage</td>
<td>23</td>
<td>24</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>$I_{O}$</td>
<td>Output Current</td>
<td>1</td>
<td>1.2</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>TRANSIENT RESPONSE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta I_{TRAN}$</td>
<td>Load Step</td>
<td>0.35</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$\Delta V/\Delta T$</td>
<td>Load slew rate</td>
<td>9</td>
<td>A/µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{TRAN}$</td>
<td>$V_{O}$ undershoot</td>
<td>500</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$t_S$</td>
<td>Settling time</td>
<td>300</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

Equation 13 and Equation 14 give Sn and Se for the TPS61175.

\[
S_n = \frac{V_{IN}}{L} * R_{SNS} = \frac{12V}{22\mu\text{H}} * 40\text{mΩ}
\]

\[
S_c = \frac{0.32V}{16 * (1 - D) * 6\text{pF}} + \frac{0.5\mu\text{A}}{6\text{pF}}
\]

Where $R_i$ is the frequency setting resistor.

1. Choose the desired loop crossover frequency, $f_c$.

One fifth of the switching frequency is...
\[ f_{SW} = \frac{750kHz}{5} = 150kHz \]  

\[ f_{RHPZ} \] is calculated using Equation 4

Where:

\[ R_{OUT} = \frac{V_{OUT}}{I_{OUT}} = \frac{24V}{1.2A} = 20\Omega \]  

From Equation 4

\[ f_{RHPZ} = \frac{20}{2\pi * 22uH} * \left( \frac{12V}{24V} \right)^2 = 36.2kHz \]

one-third of \( f_{RHPZ} \) is

\[ f_{RHPZ} = \frac{3}{3} = 12.1kHz \]

thus, try \( f_c = 10kHz \).

2. Find the output cap value using Equation 11

\[ C_{out} = \frac{\Delta I_{TRAN}}{2\pi * f_c * V_{TRAN}} = \frac{350mA}{2\pi * 10kHz * 500mV} = 11.14\mu F \]

Three 4.7 \( \mu F \) capacitors in parallel yield a total of 14.7 \( \mu F \) for the output capacitance (C8, C9, and C11 in Figure 2)

3. Properly size the compensation resistor, \( R_c \) (R3 in Figure 2). Using MathCAD, plot the power stage, \( G_{PS}(s) \), with \( R_{SENSE} = 40 \Omega \) (given in the datasheet)

from Equation 2

\[ f_p = \frac{2}{2\pi * R_{OUT} * C_{out}} = \frac{2}{2\pi * 20\Omega * 3 * 4.7\mu F} = 1.1kHz \]

From Equation 4, \( f_{RHPZ} \) is 36.2 kHz. Neglecting the ESR zero produced by the ceramic output capacitors gives the plot found in Figure 3.

**Figure 3. Simulated Bode Plot of Power Stage Gain and Phase**

The crossover frequency, \( f_c \), was chosen as 10 kHz and from Figure 3, \( K_{PW} \) (10 kHz) = 22 dB. With \( R_{TOP} = 301 \Omega \), \( R_{BOT} = 16.2 \Omega \) (R1 and R2 respectively in Figure 2), and \( G_{EA(TYP)} = 340 \mu mho \), solving Equation 12 for \( R_c \) gives:

\[ K_{COMP-db}(f_c) = 20 * \log(G_{EA} * R_c * \frac{R_{BOT}}{R_{BOT} + R_{TOP}}) = -K_{PW-db}(f_c) \Rightarrow \]
4. Properly size the compensation capacitor, $C_{C1}$ (C4 in Figure 2).

Solving Equation 10 for $C_{C1}$ and setting $f_z = f_c/10 = 1$ kHz gives

$$C_{C1} = \frac{1}{2\pi R_C f_z} = \frac{1}{2\pi \times 4.57k\Omega \times 1kHz} = 34.82nF \Rightarrow 33nF$$

(23)

5. Optionally, size the compensation capacitor, $C_{C2}$ (C5 in Figure 2)

A stray capacitance of 10 pF is assumed for $C_5$.

Figure 4 displays the plot for the Type II compensated amplifier and Figure 5 shows $T(s) = G_{PS}(s) \times H_{EA}(s) \times H_{e}(s)$ with $R_C$ ($R_3$) reduced to 3.09 kΩ, getting closer to the desired 60 degree phase margin.

Figure 4. Simulated Bode Plot of the Type II Compensation (Including Feedback Network) for a $g_m$ Error Amplifier

Figure 5. Modeled Bode Plot of the Total Open Loop
As Figure 6 shows, the measured loop compares favorably with the simulated loop.

Figure 6. Loop Gain and Phase
Appendix A Additional Data

Figure 7. Full Model Diagram

\[
G_{id}(s) = \frac{2V_o^3}{V_{in}^2} \left( 1 + \frac{R_o C_o}{2} s \right) \left( 1 + \frac{V_o^2}{V_{in}^2} \frac{1}{s} + \frac{V_o^2}{V_{in}^2} \frac{L C_o}{s^2} \right)
\]

Where:

\[
G_{PS}(s) = \frac{v_e}{v_c} = \frac{F_m G_{vd}(s)}{1 + F_m R_{SENSE} H_e(s) G_{id}(s) - F_n K_r G_{vd}(s)}
\]

\[
F_m = \frac{1}{(S_e + S_n)T_s}
\]

\[
G_{vd}(s) = \frac{V_o^2}{V_{in}^2} \left( 1 - \frac{V_o^2}{V_{in}^2} \frac{1}{s} + \frac{V_o^2}{V_{in}^2} \frac{R_o}{s^2} \right) \left( 1 + \frac{V_o^2}{V_{in}^2} \frac{1}{s} + \frac{V_o^2}{V_{in}^2} \frac{L C_o}{s^2} \right)
\]

\[
H_e(s) = 1 - \frac{T_s}{2} s + \frac{T_s}{\pi} s^2
\]

A.1 References


Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Audio</td>
<td>Automotive and Transportation</td>
</tr>
<tr>
<td>Amplifiers</td>
<td>Communications and Telecom</td>
</tr>
<tr>
<td>Data Converters</td>
<td>Computers and Peripherals</td>
</tr>
<tr>
<td>DLP® Products</td>
<td>Consumer Electronics</td>
</tr>
<tr>
<td>DSP</td>
<td>Energy and Lighting</td>
</tr>
<tr>
<td>Clocks and Timers</td>
<td>Industrial</td>
</tr>
<tr>
<td>Interface</td>
<td>Medical</td>
</tr>
<tr>
<td>Logic</td>
<td>Security</td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>Space, Avionics and Defense</td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>Video and Imaging</td>
</tr>
<tr>
<td>RFID</td>
<td></td>
</tr>
<tr>
<td>OMAP Mobile Processors</td>
<td>TI E2E Community</td>
</tr>
<tr>
<td>Wireless Connectivity</td>
<td><a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a></td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated