Creating a Universal Car Charger for USB Devices From the TPS54240 and TPS2511

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ABSTRACT

This application report describes how to design a Universal Car Charger for USB devices. The TPS2511 auto-detect feature monitors USB data line voltage, and automatically provides the correct electrical signatures on the data lines to charge compliant devices among the following dedicated charging schemes:

1. Divider DCP for Apple® devices, required to apply 2.7 V/2.0 V or 2.0 V/2.7 V on the D+/D– lines respectively
2. BC1.2 DCP, required to short the D+ line to the D– line
3. 1.2 V/1.2 V on the D+/D– lines for Samsung Tablets

The form factor of the design complies to the UL standard 2089 and ANSI/SAE J563 specification and can be easily adapted to meet other form factors.

Contents

1 Universal Car Charger Design Requirements ................................................................. 2
2 Input Protection Circuitry ................................................................................................. 4
   2.1 Design Example with FET and Linear Regulator Zener Selection .................................... 4
3 Switching Power Supply Specifications Using the TPS54240 ................................................. 5
   3.1 Switching Frequency .................................................................................................. 5
   3.2 Output Inductor Selection .......................................................................................... 6
   3.3 Output Capacitor ....................................................................................................... 6
   3.4 Catch Diode ................................................................................................................ 7
   3.5 Input Capacitor .......................................................................................................... 8
   3.6 Slow Start Capacitor ................................................................................................. 8
   3.7 Bootstrap Capacitor Selection .................................................................................... 8
   3.8 Undervoltage Lockout Set Point .................................................................................. 8
   3.9 Output Voltage and Feedback Resistors Selection .......................................................... 9
   3.10 Compensation .......................................................................................................... 9
4 Current-Limit Switch Specifications Using the TPS2511 ...................................................... 11
   4.1 Selecting the Current-Limit Resistor .......................................................................... 11
   4.2 DCP Auto-Detect ..................................................................................................... 11
5 Experimental Results ....................................................................................................... 13
6 Board Layout .................................................................................................................... 18

List of Figures

1 Universal Car Charger ....................................................................................................... 2
2 USB iPhone Car Charger Input Protection Circuit Schematic .............................................. 4
3 5-V Output TPS54240 Design Example .............................................................................. 6
4 5-V Output TPS2511 Design Example ................................................................................ 11
5 TPS2511 DCP Auto-Detect Functional Diagram ................................................................. 12
6 Efficiency Versus Load Current Prior to the Load Switch .................................................... 13
The input voltage supply for a car charger is typically 12 V, but can range from 6 V to 14.5 V with input surges of up to 40 V for multiple 16-ms durations. The power supply must be able to tolerate these surges, and regulate the output to a nominal 5 V with a tolerance of 4.75 V to 5.25 V. Since the USB cable may cause the output voltage to fall at heavy loads, it is desirable to have droop compensation to raise the output voltage during this condition. Short-circuit protection is required in case of a fault with the USB port. The average current consumption depends on the device connected to the USB port, but can be as high as 2.1 A continuous.

The form factor of the design is an important consideration, allowing for the car charger to be inserted and removed easily, with little material extending beyond the socket. The form factor must be small enough to meet UL standard 2089 and ANSI/SAE J563 specification.
Additionally, to charge devices quickly, the car charger must support the data handshaking protocol required to support USB 2.0 BC1.2 and Divider Mode devices such as iPod® and iPhone® to allow charging currents as much as four times greater than USB 2.0 allows. Without this handshaking protocol, many handsets and smartphones on the market fail to charge.

The report goes through a step-by-step procedure to design the car charger power supply with the help of a reference design implemented using TPS54240 and TPS2511. If a design requires a higher power level, consider the TPS54340. It has a higher minimum peak current limit of 4.5 A and a 92-mΩ, high-side FET.

The TPS54240 SWIFT™ converter has the following features:

- Current mode control: Provides simple external compensation and flexible component selection.
- Pulse skip mode: Reduces no load supply current.
- 200-mΩ, high-side MOSFET (FET) provides a cost-effective power supply for 1-A to 2-A transient load with a minimum current limit of 3.5 A.
- Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin.
- Slow Start controls the output voltage start-up ramp and can also be configured for sequencing/tracking.
- An open-drain, power-good signal indicates the output is within 93% to 107% of its nominal voltage.
- A wide switching frequency range allows efficiency and external component size to be optimized.
- Frequency foldback and thermal shutdown protects the part during an overload condition

The TPS2511 USB Charging Port Power Switch and Controller has the following features:

- Meets Battery Charging Specification BC1.2 for DCP.
- Support Sleep-Mode Charging for most available Apple devices.
- Compatible with USB 2.0 and 3.0 Power Switch requirements.
- 70-mΩ, high-side MOSFET for low power dissipation
## Input Protection Circuitry

Several different options are available for protecting the car charger from large voltage swings during normal operation, double battery jump start, or load dump when the battery is disconnected. The solution chosen for this example is a simple Zener diode and FET to regulate the voltage to 39 V. This allows the use of the TPS54240 (42-V converter), which is cost effective and efficient. If a wider input voltage is expected, a higher voltage FET can be used to extend the range as high as necessary. Care needs to be taken that the safe operating area of the FET is not exceeded under transient conditions. The diode D1 provides protection against reverse polarity connection of the input. F1 is a 2-A fuse used to protect against catastrophic failures.

### 2.1 Design Example with FET and Linear Regulator Zener Selection

The maximum voltage for the TPS54240 is 42 V, therefore the input voltage to the converter is limited to 39 V. Q2 and D2 form a linear regulator that clamps the voltage at 39 V if the input goes higher. To be able to handle 40-V surges, a 60-V, P-Channel FET is chosen. This provides some margin on the input voltage spikes and not exceed the VDS of the FET. Care must also be taken to ensure that the SOA of the FET is not exceeded. For this case, a FDC5614P from Fairchild is used. The Zener diode D2 sets the regulation voltage point, so a 39-V part is used. The other components (Q1, D100, R2, R4, R6, R10, and C101) provide the bias and control for the gate of the FET.
3 Switching Power Supply Specifications Using the TPS54240

Consider the following system parameters:

- Output Voltage 5 V
- Transient Response 1-A to 2-A load step Vout between 4.75 V and 5.25 V (5%)
- Output Current up to 2.1A (DC)
- Input Voltage 12 V nom. 8 V to 40 V
- Output Voltage Ripple 1% of Vout
- Start Input Voltage (rising VIN) 8 V
- Stop Input Voltage (falling VIN) 6 V

### NOTE:
The equations given in the following design examples come from TPS54240 (SLVSA6) data sheet. For detailed variable names and assumptions refer to the data sheet.

#### 3.1 Switching Frequency

Higher switching frequencies enable the use of smaller (and cheaper) output filter components whereas lower switching frequencies tend to have higher efficiencies. To meet both the size requirements as well as thermal requirements, a suitable switching frequency must be a compromise. The TPS54240 can be operated at switching frequencies from 100 kHz to 2500 kHz.

The following equations impose limits over the maximum switching frequency:

1. **To avoid pulse-skipping:** As the frequency is increased, the on time for a given duty cycle is decreased ($D = T_{ON} \times f_{sw}$). For consistent switching action without pulse skipping, the on time must be greater than the minimum controllable on time. For the TPS54240, this minimum controllable on time is typically 135 ns.

2. **Frequency Foldback:** During overcurrent conditions, the output voltage decreases as the overcurrent protection is activated. As the foldback voltage at VSENSE decreases below 0.6 V, the switching frequency is reduced by 50% of the nominal value. At a VSENSE voltage of 0.4 V, the switching frequency is reduced to 25%, and finally when the VSENSE voltage falls below 0.2 V, the switching frequency is reduced to 12.5% of the nominal set frequency. This is done so that in any individual switching cycle, sufficient time is available for the inductor current to ramp below the overcurrent threshold. This feature is known as Frequency Foldback.

\[
\begin{align*}
 f_{SW(max\,skip)} &= \frac{1}{t_{ON}} \times \frac{I_L \times R_{DC} + V_{OUT} + V_d}{(V_{IN} - I_L \times R_{HS} + V_d)} \\
 f_{SW(shift)} &= \frac{f_{div}}{t_{ON}} \times \frac{I_L \times R_{DC} + V_{OUTSC} + V_d}{(V_{IN} - I_L \times R_{HS} + V_d)}
\end{align*}
\]

Where:

- $I_L$ = inductor current
- $R_{DC}$ = inductor resistance
- $V_{IN}\text{MAX}$ = maximum input voltage
- $V_{OUT}$ = output voltage
- $V_{OUTSC}$ = output voltage during short
- $I_{OUTS}$ = output short circuit current
- $V_d$ = diode voltage drop
- $R_{DS(on)}$ = switch on resistance
- $t_{ON\,min}$ = minimum controllable on time
- $f_{div}$ = frequency division factor (1, 2, 4, or 8)

Using **Equation 1** and **Equation 2**, the maximum skip and shift frequencies are 3.38 MHz and 5.5 MHz, thus the switching frequency is less than 2.5 MHz (the lesser value of maximum skip and shift frequencies or 2.5 MHz).

This design uses a nominal switching frequency of 500 kHz to allow for high efficiency and good thermal performance. The switching frequency is set by placing a resistor, R5, from the RT/CLK pin to ground.
The value of the R5 is calculated by Equation 3:

\[
RT \text{ (kOhm)} = \frac{206033}{f_{sw} \text{ (kHz)}^{1.0888}}
\]  

(3)

For 500 kHz – switching frequency, R5 must be 237 kΩ.

3.2 **Output Inductor Selection**

The output inductor is typically selected so that the peak-to-peak ripple current is 30% of the output current. Verify that the RMS and saturation current ratings for the inductor exceed application specifications.

Once the inductor is chosen, the peak-to-peak inductor current can be calculated using Equation 5.

\[
L_0 \text{ min} = \frac{V_{\text{in max}} - V_{\text{out}}}{I_o \times K_{\text{IND}}} \times \frac{V_{\text{out}}}{V_{\text{in max}} \times f_{\text{sw}}}
\]

(4)

\[
I_{\text{RIPPLE}} = \frac{V_{\text{OUT}} \times (V_{\text{in max}} - V_{\text{OUT}})}{V_{\text{in max}} \times L_0 \times f_{\text{sw}}}
\]

(5)

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from:

\[
I_{L_{\text{rms}}} = \sqrt{(I_o)^2 + \frac{1}{12} \times \left(\frac{V_{\text{OUT}} \times (V_{\text{in max}} - V_{\text{OUT}})}{V_{\text{in max}} \times L_0 \times f_{\text{sw}}}\right)^2}
\]

(6)

\[
IL_{\text{peak}} = I_{\text{out}} + \frac{I_{\text{ripple}}}{2}
\]

(7)

Using a Kind of 2, the required minimum inductor is calculated to be 20.8 µH. The nearest standard value inductor is 22 µH. The rms current rating is 3.5 A, and the saturation current rating is 3.6 A before a 20% drop in inductance. The calculated peak-to-peak ripple current, rms current, and peak currents are 390 mA, 2.1 A, and 2.3 A.

3.3 **Output Capacitor**

The output capacitor determines the modulator pole, the output voltage ripple, and response of the regulator to a large change in load current. It needs to be selected based on the most stringent of these three criteria.
The desired response to a large change in the load current is the first criteria. The output capacitor (Cout = C4 || C5) needs to supply the load with current when the regulator can not.

\[
\text{Cout} > \frac{2 \times \Delta I_{\text{out}}}{f_{\text{sw}} \times \Delta V_{\text{out}}}
\]  

(8)

For this example, the transient load response is specified as a 5% change in Vout for a load step from 1 A to 2 A. Thus, \(\Delta I_{\text{out}} = 1\) A and \(\Delta V_{\text{out}} = 0.05 \times 5 = 0.250\) V. Using these numbers gives a minimum capacitance of 9 \(\mu\)F.

When the load current rapidly decreases, the stored energy in the inductor produces an output voltage overshoot. To absorb this energy, the output capacitor needs to be sized properly, thereby maintaining the desired output voltage during these transient periods. Equation 9 is used to calculate the minimum capacitance required to keep the output voltage overshoot to a desired value.

\[
\text{Cout} > \text{Lo} \times \frac{(I_{\text{OH}}^2 - I_{\text{OL}}^2)}{(V_{f}^2 - V_{i}^2)}
\]  

(9)

Where L is the value of the inductor, \(I_{\text{OH}}\) is the output current under heavy load, \(I_{\text{OL}}\) is the output under light load, \(V_{f}\) is the final peak output voltage, and \(V_{i}\) is the initial capacitor voltage. For this example, the worst-case load step is from 2 A to 0.1 A. The output voltage increases during this load transition and the stated maximum in our specification is 5% of the output voltage. This makes \(V_{f} = 1.05 \times 5 = 5.25\).

\(V_{i}\) is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 9 yields a minimum capacitance of 26 \(\mu\)F.

Equation 10 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where \(f_{\text{sw}}\) is the switching frequency, \(V_{\text{ORIPPLE}}\) is the maximum allowable output voltage ripple, and \(I_{\text{RIPPLE}}\) is the inductor ripple current. The maximum ESR an output capacitor can have to meet the output voltage ripple specification is calculated using following:

\[
\text{Cout} > \frac{1}{8 \times f_{\text{sw}}} \times \frac{1}{V_{\text{ORIPPLE}}} \times \frac{1}{I_{\text{RIPPLE}}}
\]  

(10)

Equation 11 indicates the ESR is less than 75 m\(\Omega\). The most stringent criterion for the output capacitor is found to be 26 \(\mu\)F of capacitance to keep the output voltage in regulation during a load transient.

\[R_{\text{ESR}} < \frac{V_{\text{ORIPPLE}}}{I_{\text{RIPPLE}}}
\]  

(11)

Additional capacitance de-ratings for aging, temperature, and dc bias must be factored, which increases this minimum value. For this example, a 22-\(\mu\)F and 10-\(\mu\)F, 10-V ceramic capacitors with 3 m\(\Omega\) of ESR are used.

Using Equation 12 the total rms current in the output capacitors is calculated. For this application, following equation yields 115 mA.

\[
I_{\text{coms}} = \frac{V_{\text{out}} \times (\text{Vin max} - V_{\text{out}})}{\sqrt{12} \times \text{Vin max} \times \text{Lo} \times f_{\text{sw}}}
\]  

(12)

The ceramic capacitor used has an rms current rating of 2 A.

### 3.4 Catch Diode

The selected diode must have a reverse voltage rating equal to or greater than Vinmax. The peak current rating of the diode must be greater than the maximum inductor current. The diode must also have a low forward voltage.

For the example design, the SK24-TP Schottky diode with 40V reverse voltage is selected for its lower forward voltage and it comes in a smaller package size which has good thermal characteristics. The typical forward voltage of the SK24-TP is 0.55 V.
During the converter on time, the output current is provided by the internal switching FET. During the off time, the output current flows through the catch diode. The average power in the diode is given by Equation 13:

\[
P_d = \frac{(V_{\text{in}} - V_{\text{out}}) \times I_{\text{out}} \times V_{\text{f}} \times C_j \times f_{\text{sw}} \times (V_{\text{in}} + V_{\text{f}})^2}{V_{\text{in}} \times 2}
\]

(13)

The SK24-TP has a junction capacitance of 50 pF. The selected diode dissipates up to 0.75 W, as the package is rated at 20°C/W.

### 3.5 Input Capacitor

The TPS54240 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54240. The input ripple current can be calculated using Equation 14:

\[
I_{\text{cirms}} = I_{\text{out}} \times \sqrt{\frac{V_{\text{out}}}{V_{\text{in}}} \times \frac{(V_{\text{in}} - V_{\text{out}})}{V_{\text{in}}}}
\]

(14)

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15:

\[
\Delta V_{\text{in}} = \frac{I_{\text{out}} \times 0.25}{C_{\text{in}} \times f_{\text{sw}}}
\]

(15)

### 3.6 Slow Start Capacitor

The slow start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Using the slow-start time as 3.5 ms, the value of slow-start capacitor is computed with the help of Equation 16 to be 8.75 nF. For this design, the next larger standard value of 10 nF is used.

\[
T_{\text{ss}} > \frac{C_{\text{out}} \times V_{\text{out}} \times 0.8}{I_{\text{ssavg}}}
\]

(16)

Where:

- Issavg = Average slow start current
- Tss = Minimum slow start time

### 3.7 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. The capacitor must have a 10 V or higher voltage rating.

### 3.8 Undervoltage Lockout Set Point

The programmable UVLO and enable voltages are set using the resistor divider of R1 and R4 between Vin and ground to the EN pin. Equation 17 and Equation 18 can be used to calculate the necessary resistance values.

For the example application, a 200 kΩ between Vin and EN (R3) and a 34.8 kΩ between EN and ground (R7) are required to produce the 8 V and 6 V start and stop voltages.

\[
R1 = \frac{V_{\text{START}} - V_{\text{STOP}}}{I_{\text{HYS}}}
\]

(17)

\[
R2 = \frac{V_{\text{ENA}}}{R1} \times \frac{V_{\text{START}} - V_{\text{ENA}} + I_{\text{f}}}{R1}
\]

(18)

Where \(I_{\text{HYS}} = 2.9 \, \mu\text{A}\) and \(I_{\text{f}} = 0.9 \, \mu\text{A}\).
3.9 Output Voltage and Feedback Resistors Selection

For the example design, 2.00 kΩ was selected for R9 and R1 was calculated to be 10.5 kΩ using Equation 19:

$$\text{R1} = \text{R2} \times \left(\frac{\text{Vout} - 0.8V}{0.8 \text{ V}}\right)$$

(19)

3.10 Compensation

To stabilize the closed-loop circuit, a compensation network is required. The compensation components are connected from the COMP pin to GND. For this example, some simplifying assumptions are made so as to ease the design procedure.

To properly compensate the closed-loop circuit, the gain characteristics of the power stage must be determined. In general, the power stage pole, and the power stage zero frequency must be known. These terms are defined as follows:

$$\text{fp mod} = \frac{\text{Ioutmax}}{2 \times \pi \times \text{Vout} \times \text{Cout}}$$

(20)

$$\text{fz mod} = \frac{1}{2 \times \pi \times \text{Resr} \times \text{Cout}}$$

(21)

For Cout, a de-rated value of 19 µF is used.

Use Equation 22 and Equation 23, to estimate a starting point for the crossover frequency, fco, to design the compensation.

For the example design:

$$\text{fpmod} = 3.52 \text{ kHz} \{\text{V OUT} = 5 \text{ V, I OUT} = 2.1 \text{ A, Cout} = 19 \text{ µF bias de-rated}\}$$

$$\text{fzmod} = 5584 \text{ kHz} \{\text{Resr} = 3 \text{ mΩ / 2 = 1.5 mΩ , Cout} = 19 \text{ µF bias de-rated}\}$$

Equation 22 is the geometric mean of the modulator pole and the ESR zero and Equation 23 is the mean of modulator pole and the switching frequency.

$$\text{fco} = \sqrt{\text{fpmod} \times \text{fzmod}}$$

(22)

$$\text{fco} = \frac{\sqrt{\text{fpmod} \times \text{fzmod}}}{2}$$

(23)

Equation 22 yields 140 kHz and Equation 23 gives 29.7 kHz. Using the lower value of Equation 22 or Equation 23 as the upper limit for an initial crossover frequency, the target cross-over frequency(\(\text{fco}\)) is 15 kHz.

Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

To determine the compensation resistor, R5, use Equation 24.

$$\text{R5} = \left(\frac{2 \times \pi \times \text{fco} \times \text{Cout}}{\text{gm} \times \text{Cout}}\right) \times \left(\frac{\text{Vout}}{\text{VREF} \times \text{gmea}}\right)$$

(24)

Assume the power stage transconductance, \(\text{gm} \), is 10.5 A/V. The output voltage, \(\text{Vout}\), reference voltage, \(\text{VREF}\), and amplifier transconductance, \(\text{gmea}\), are 5 V, 0.8V and 310 mA/V, respectively.

R5 is calculated to be 2.94 kΩ, use the nearest standard value of 3.01 kΩ. Use Equation 25 to set the compensation zero to the modulator pole frequency. Equation 25 yields 0.016 µF for compensating capacitor C8, a 0.01 µF is used for this design.

$$\text{C8} = \frac{1}{2 \times \pi \times \text{R4} \times \text{fp mod}}$$

(25)
A compensation pole can be implemented if desired using an additional capacitor C7 in parallel with the series combination of R5 and C8. Use the larger value of Equation 26 and Equation 27 to calculate C7 to set the compensation pole. 330 pF is selected for C7.

\[
C_7 = \frac{C_O \times R_{esr}}{R_4}
\]  
\[
C_7 = \frac{1}{R_4 \times f_{sw} \times \pi}
\]  

(26)  
(27)
4 Current-Limit Switch Specifications Using the TPS2511

The TPS2540 is operated as a dedicated charging port. Two modes are used, divider mode and BC1.2 mode. Divider mode is used to charge Apple devices. BC1.2 mode is used to charge any BC1.2 mode device that can include Android phones, Blackberry phones, and other compliant devices. As an optional feature, a LED (D4) provides a status indicator.

Figure 4. 5-V Output TPS2511 Design Example

4.1 Selecting the Current-Limit Resistor

R11 is used to set the current limit for the switch. The current limit is set to the maximum value to ensure that the device is able to provide the full 2.1 A for charging. Equation 28 is used to calculate the nominal short-circuit protection level. Equation 29 and Equation 30 calculate the minimum and maximum protection levels.

\[
I_{\text{SHORT}} = \frac{51228}{R_{\text{LIMx}}}
\]

(28)

\[
I_{\text{SHORT \_ min}} = \frac{51228}{1.03 R_{\text{LIMx}}}
\]

(29)

\[
I_{\text{SHORT \_ max}} = \frac{51228}{0.967 R_{\text{LIMx}}}
\]

(30)

4.2 DCP Auto-Detect

The TPS2511 integrates an auto-detect feature to support Divider mode, short mode and 1.2 V/1.2 V mode. If a divider device is attached, 2.7 V and 2.0 V are presented on DP and DM pins. If a BC1.2-compliant device is attached, the TPS2511 will automatically switch into short mode. If a device compliant with 1.2 V/1.2 V charging scheme is attached, 1.2 V will be applied on both DP and DM. The functional diagram of DCP auto-detect is shown in Figure 5.
Figure 5. TPS2511 DCP Auto-Detect Functional Diagram
5 Experimental Results

Figure 6 to Figure 17 show the experimental test results of the Figure 3 design. The input current draw at no load at 12-V input voltage is 6 mA (most of which is powering the optional LED).

Figure 6. Efficiency Versus Load Current Prior to the Load Switch

Figure 7. Efficiency Versus Load Current After the Load Switch

Figure 8. Output Voltage Versus Load Current Before the Switch

Figure 9. Output Voltage Versus Load Current After the Switch
Figure 10. Output Voltage Ripple Before the Switch, I_{out} = 2 A

Figure 11. Output Voltage Ripple After the Switch, I_{out} = 2 A
Experimental Results

Figure 12. Input Voltage Ripple, I_{\text{out}} = 2 \text{ A}

Figure 13. Load Transient 1-A to 2-A Step
Experimental Results

Figure 14. Load Transient 0.1-A to 2-A Step

Figure 15. Start-Up Relative to Vin
Figure 16. Vout, Inductor Current and PH, CCM

Figure 17. Overall Loop Frequency Response, iout = 2 A
6  Board Layout

This section provides a description of the board layout and layer illustrations. The board layout for the reference designs is shown in Figure 18 through Figure 21. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for VIN, VOUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54240 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including six vias directly under the TPS54260 device to provide a thermal path from the top-side ground area to the bottom-side ground plane. The input decoupling capacitor (C3) and bootstrap capacitor (C1) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper VOUT trace past the output capacitors.

Figure 18. PMP5951 Top Side Assembly
Figure 19. PMP5951 Top Side Layout

Figure 20. PMP5951 Bottom Side Assembly
Figure 21. PMP5951 Bottom Side Layout
## Table 1. Bill of Materials

<table>
<thead>
<tr>
<th>Count</th>
<th>RefDes</th>
<th>Value</th>
<th>Description</th>
<th>Size</th>
<th>Part Number</th>
<th>Mfr</th>
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<td>C1, C10</td>
<td>0.1 µF</td>
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<td>0402</td>
<td>Std</td>
<td>Std</td>
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<td>0402</td>
<td>Std</td>
<td>Std</td>
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<tr>
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<td>0805</td>
<td>Std</td>
<td>Std</td>
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<td>22 µF</td>
<td>Capacitor, ceramic, 6.3 V, X5R, 20%</td>
<td>0805</td>
<td>Std</td>
<td>Std</td>
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<tr>
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<td>0603</td>
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<td>Std</td>
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<td>Std</td>
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<td>Diode, Zener, 39 V, 100-mA, 200 mW</td>
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<td>LTST-C190KGKT</td>
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<td>F1</td>
<td>2 A</td>
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<td>F0603E3R00FSTR</td>
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<td>Bead, SMD ferrite, 26 Ω, @ 100 MHz, 10 mΩ DC, 6A</td>
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<td>22 µH</td>
<td>Inductor, Toroid 8 mm, 25 turns #24AWG</td>
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<td>MOSFET, Pch, -60 V, 3.4 A , 112 mΩ</td>
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<td>3</td>
<td>R1, R6, R14</td>
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<td>R9</td>
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<td>IC, 3.5 V-42 V Stepdown SWIFT, DC-DC Converter With ECO-Mode</td>
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<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
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<tbody>
<tr>
<td>Audio</td>
<td>Automotive and Transportation</td>
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<tr>
<td>Amplifiers</td>
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<td>Data Converters</td>
<td>Computers and Peripherals</td>
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<td>DLP® Products</td>
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