

# Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheet

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## ABSTRACT

The stability boundary conditions charts in the TL431, TL432 data sheet (<u>SLVS543</u>) are often misinterpreted leading to designs with occasional problems with oscillation. This application note gives design guidance.

# **Choosing a Shunt Capacitor**

The TL431, TL432 family of shunt regulators were designed to have wide bandwidth while ensuring stability without any external frequency compensation. This makes the device very useful in a control loop application and as a reference voltage generator without external capacitance.

Adding an external capacitor across cathode to anode (ground) when used as a reference generator will create an output pole. This pole will reduce the phase margin and potentially cause oscillation. The acceptable range for load capacitance can be determined from the typical stability boundary conditions in the TL431, TL432 data sheet. The first step is to determine which of the two charts to use. There are two stability charts in the typical characteristics section of the data sheet because the two die designs have different stability boundaries. The chart titles list the devices covered by the chart.

The application cathode voltage determines which chart series to use. The series are Vref, 5V, 10V, and 15V and labeled as A, B, C, and D respectively. Other application voltages can be visually interpolated between the other series. The point where the application cathode current (Y axis) intersects the VKA series has a corresponding capacitance value on the X axis.

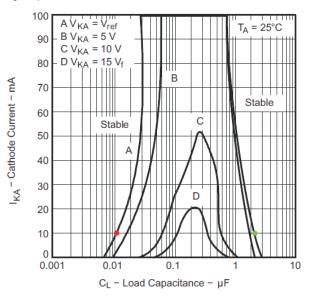


Figure 1. Stability Boundary Conditions For all TL431 and TL431A Devices (Except for SOT23-3, SC-70, and Q-Temp Devices)

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Figure 1 Series "A" is needed because VKA = V<sub>ref</sub>. The 10 mA cathode current line intersects series "A" close to 0.01 µF (red dot) and a second time at 2.2 µF (green dot). This means the capacitance range between 0.01 µF and 2.2 µF would cause a typical device to oscillate. Using capacitance less than 0.01  $\mu$ F or greater than 2.2  $\mu$ F would not oscillate with a typical device.

However, this chart represents a typical device and no phase margin. As a point of reference, figure 2 shows stability with 30° phase margin. A robust design must have a significant phase margin for all devices to prevent oscillation or ringing on transients.

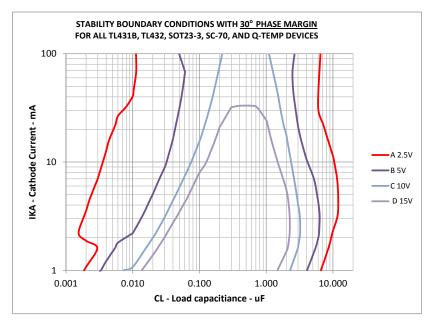
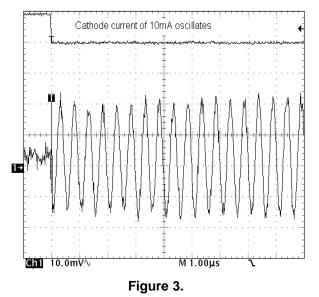


Figure 2. Stability Boundary Conditions For all TL431B and TL432 Devices

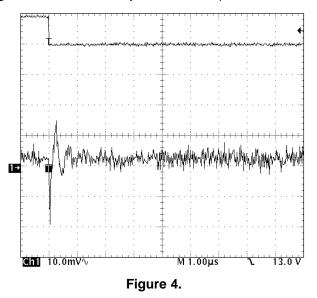
Using a value ½ the capacitance 0.01 µF does not provide enough design margin. A randomly chosen TL431AILP sample had a low level oscillation using a 5 nF capacitor. The oscilloscope capture shows the cathode voltage that is initially has 12 mA of cathode current. At 1 µS (one division), the cathode current is lowered to 10 mA. The cathode begins to oscillate at an amplitude of approximately 35 mV peak-to-peak.



2



Robust protection from oscillation requires phase margin for all samples across temperature so the recommend capacitance is less than 1/10 of the left boundary line or greater than 10 times the right boundary line. For the example, the recommended range is less than 1 nF or greater than 22  $\mu$ F. The cathode waveform using 1 nF on the randomly selected sample with a 1 nF capacitor is in Figure 4.



With 1 nF capacitive load, the output is stable and the transient ringing falls into the noise floor.

# 1 Output capacitor zero as a solution

The output capacitor pole greatly limits the capacitors that can be used. However, any capacitor could be used if a series resistor was added that created an output zero at a low enough frequency. The zero can cancel most of phase lag of the output pole at the unity gain bandwidth frequency of the loop.

The charts in figures 5 through 8 show the series resistance that needs to be added to create an output zero at ½ the typical unity gain frequency of the shunt when loaded with the capacitance directly (no series resistance) and a low cathode current of 1mA. Adding the resistor or increasing cathode current will increase the loop unity gain frequency a little and device variance could reduce the bandwidth a little. The 2:1 bandwidth to zero ratio will provide good phase margin relief to make a stable reference generator.

Figures 5 through 8 show the minimum recommended series resistance to add for desired output capacitance. There is no limit to the maximum resistance.

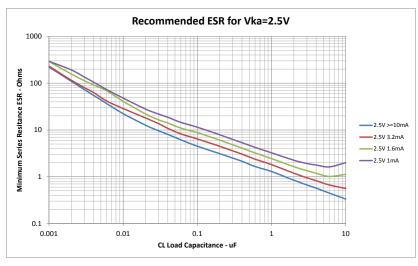


Figure 5. ESRs @ Vka=2.5V



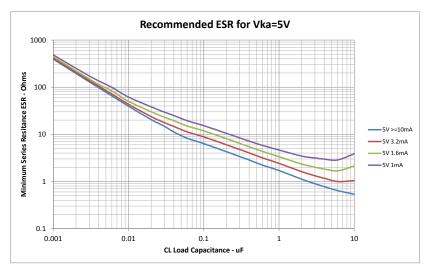


Figure 6. ESRs @ Vka=5V

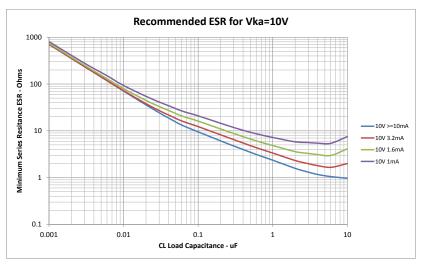


Figure 7. ESRs @ Vka=10V

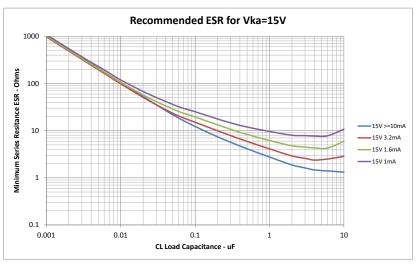


Figure 8. ESRs @ Vka=15V

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**Revision History** 

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# **Revision History**

Cł	Changes from Original (September 2011) to A Revision Pag				
•	Added Stability Boundary Conditions graph.	2			
•	Added ESR section and graphs	3			

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision History

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