

Understanding the Absolute Maximum Ratings of the SW Node

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ABSTRACT

The typical TPS62xxx synchronous buck converter has a minimum SW node voltage rating of -0.3 V . However, most buck converters appear to violate this limit during switching operation, dropping below -1 V briefly every switching cycle. This is normal operation and does not damage the part, because this voltage is caused by the output inductor driving current through a MOSFET body diode during switching operation. The minimum voltage rating found in the data sheet is actually a dc rating and means that the part could be damaged if a constant voltage below -0.3 V is applied at the SW node from a source other than the output inductor during switching operation. For instance, a dc source, if supplying a voltage lower than -0.3 V , could theoretically supply infinite current through the low-side MOSFET body diode, damaging the device. This application note explains the operation of a synchronous buck converter, demonstrates why the SW node negative rating might be exceeded during switching operation, gives guidance for properly measuring the SW node voltage, and provides good layout practices for synchronous buck converters. This application note applies to all of the TPS62xxx synchronous buck converters.

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1 Introduction

The Absolute Maximum Ratings table in a device data sheet specifies dc limits to voltages or currents that may be applied to the device pins. For the SW node, the maximum voltage rating refers to the maximum voltage that can be applied before the oxide layer in the low-side MOSFET silicon begins to break down and causes a short between the drain and source. However, the negative voltage rating for the SW node refers to the parasitic p-n junction in the low-side MOSFET, which forms its body diode. During switching operation, the negative rating is exceeded due to the operating principles of a synchronous buck converter. This does not violate the absolute maximum rating, because the current causing the voltage excursion is applied by the output inductor during switching operation. In the case of a source other than the output inductor, the -0.3-V voltage rating should never be exceeded. A dc source, if supplying a voltage lower than -0.3 V , could theoretically source infinite current through the body diode, which could damage the MOSFET.

Likewise, the SW node should not be externally forced above the input voltage plus 0.3 V with a dc source, due to the presence of a body diode across the high-side MOSFET. Again, during switching operation, the output inductor may briefly drive the SW node above this rating, but in a controlled, predictable, and understood manner. This application note explains why these voltage excursions are normal and expected behaviors of the synchronous buck converter and, as such, do not damage the device.

Additionally, this application note demonstrates a technique to properly measure the SW node voltage. Improper measurement techniques introduce extra noise that adds to the voltage excursions observed at the SW node. Properly measuring the SW node voltage allows the designer to observe the stress that the device actually undergoes without the distortion caused by the high-frequency rise and fall times of the SW node. Finally, this application note discusses design considerations for the PCB layout. A good layout minimizes EMI and noise in the system.

2 Synchronous Buck Converter Operation

Figure 1 shows a synchronous buck converter. In a buck converter, the MOSFETs act as switches and are ideally either completely on or completely off. The diodes shown are the MOSFET parasitic body diodes. V_{SW} is the voltage at the switch (SW) node of the converter.

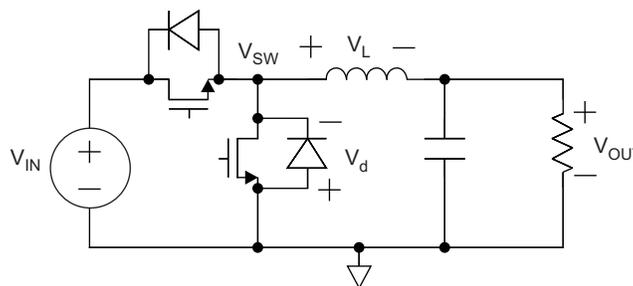


Figure 1. Synchronous Buck Converter

For proper circuit operation, only one MOSFET should be on at a time. If both MOSFETs are on at the same time, the input power supply would be shorted to ground, which could damage the power supply or the MOSFETs. This is known as shoot-through. To prevent both MOSFETs from ever being on at the same time, a short delay between the turnoff of one and the turnon of the other is required. The non-ideal behavior of MOSFETs, with their associated rise and fall times, further reinforces a need for such a delay to ensure that one MOSFET is fully off before the other begins to turn on.

This delay causes a short period of time where both MOSFETs must be off. This time between the turnoff of one MOSFET and the turnon of the other is known as the dead time. During the dead time, the inductor current must continue to flow in the same direction and with the same magnitude, because inductor current cannot change instantaneously. The only path available to positive-flowing inductor current (current flowing into the positive node of the inductor in Figure 1) is through the low-side MOSFET body diode via the load and output capacitor. This completes the current loop and causes a voltage drop across the body diode, which leads to a value lower than -0.3 V at the SW node due to the relatively high forward voltage drop of the body diode. As soon as the low-side MOSFET turns on, current stops flowing through the body diode and flows through the MOSFET, whose voltage drop is lower than the 0.3 V that might turn on the body diode. The dead time and resulting voltage drop across the synchronous FET body diode is necessary for operation of a buck converter and does not damage the IC, because the current is supplied by the inductor and is a result of the basic operating principles of the converter.

Likewise, if the inductor current flows negatively (out of the positive terminal of the inductor in Figure 1) during the dead time, the negative inductor current must flow through the high-side MOSFET body diode, through the input capacitor, and back through the output capacitor to complete its loop. This action forces the SW node to exceed the input voltage and turns on the body diode until the high-side MOSFET turns on. This operation properly maintains the negative inductor current during the dead time and does not damage the device.

Figure 2 shows an example of both positive and negative inductor current during dead times. This waveform was taken on the TPS62660 EVM with the following conditions: $V_{IN} = 3.6$ V, $V_{OUT} = 1.8$ V, and $I_{OUT} = 100$ mA. I_L is the current through the inductor.

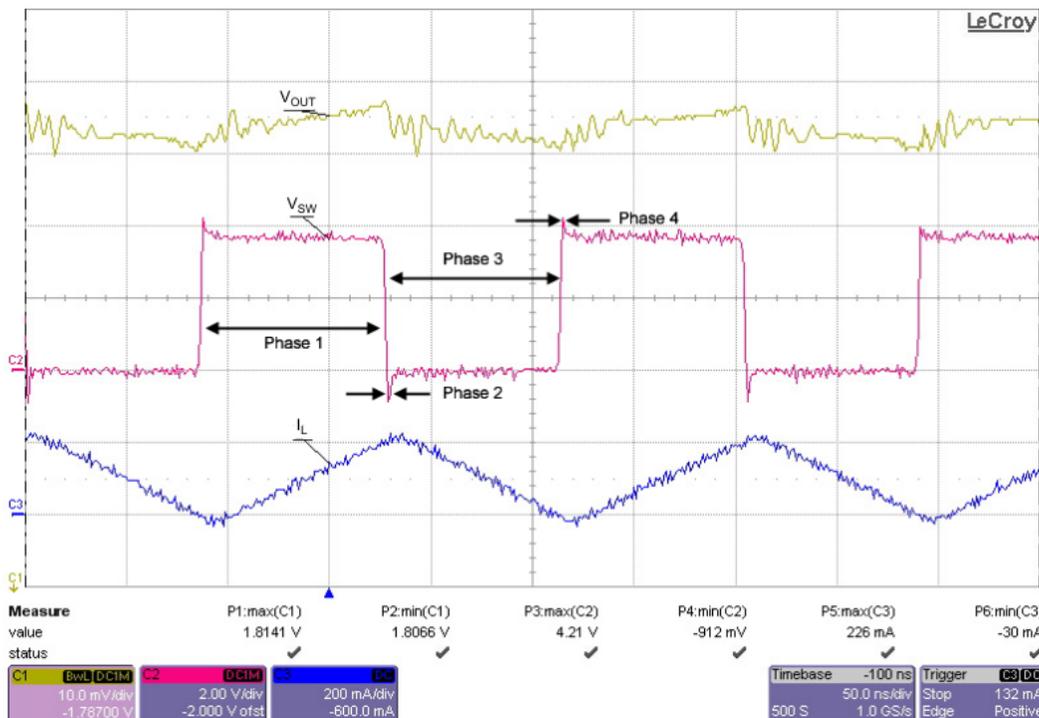


Figure 2. TPS62660 SW Node Behavior

First, consider when the high-side MOSFET is on, and the low-side MOSFET is off. In Figure 2 this is Phase 1, where the voltage at the SW node is equal to V_{IN} , and the current through the inductor is rising. In Phase 2, the high-side MOSFET switches off, meaning that the device is in a dead time. Because the inductor current cannot change instantaneously, it must continue flowing in the same direction. The only path available for the current to flow is through the low-side MOSFET body diode. This causes the voltage at the SW node to drop to about -0.7 V. After a short delay, the low-side MOSFET turns on, and the voltage at the SW node rises to approximately 0 V due to the lower voltage drop across the MOSFET $r_{DS(on)}$. This is Phase 3 in the figure. During this phase, the current through the inductor decreases. Just before Phase 3 ends, the inductor current decreases far enough to be negative. Finally, the low-side MOSFET turns off. Because the inductor current is negative, the current must flow through the high-side MOSFET body diode. In Figure 2, this transition corresponds to Phase 4, where the voltage peaks at a voltage higher than V_{IN} . This voltage excursion is not as large as in Phase 2, because the magnitude of the inductor current causing the excursion is smaller, therefore causing a smaller forward voltage drop across the body diode.

These voltage dips and peaks that occur on the SW node when the device switches are well-known and understood. Any synchronous switching converter shows this behavior. As long as these voltages are the result of switching operation and good layout techniques are followed, the IC is not stressed beyond its capabilities.

3 Proper Measurement Technique

To properly measure the voltage at the SW node, it is important to use the right measurement techniques. Extra noise can be mistakenly acquired in a measurement if the measurement is taken in the wrong location or with the wrong technique.

To achieve the most-accurate, noise-free measurement, a low-inductance probe should be used between the SW node pin and the power GND pin on the IC. This setup is illustrated in Figure 3. A low-inductance probe can be created from the traditional oscilloscope probe. Simply remove the *hat* from the probe tip and wrap a wire around the probe barrel for the ground connection. This minimizes the inductance by reducing the length of the ground return loop.

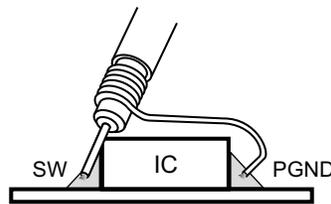


Figure 3. Low-Inductance Probe Technique

Figure 4 illustrates why the use of a low-inductance probe is important to measure the voltage at the SW node. The waveform in Figure 4 uses exactly the same operating conditions as Figure 2, except that a low-inductance probe was used to measure in Figure 2. Figure 4 uses a probe with the traditional ground clip lead that is not connected to ground in the immediate vicinity of the IC. This creates extra length and inductance in the ground connection, which distorts the measured signal. Notice that the voltage excursions are much greater in this waveform. However, these higher voltage deviations are only due to the improper measurement technique and are not what the IC actually undergoes.

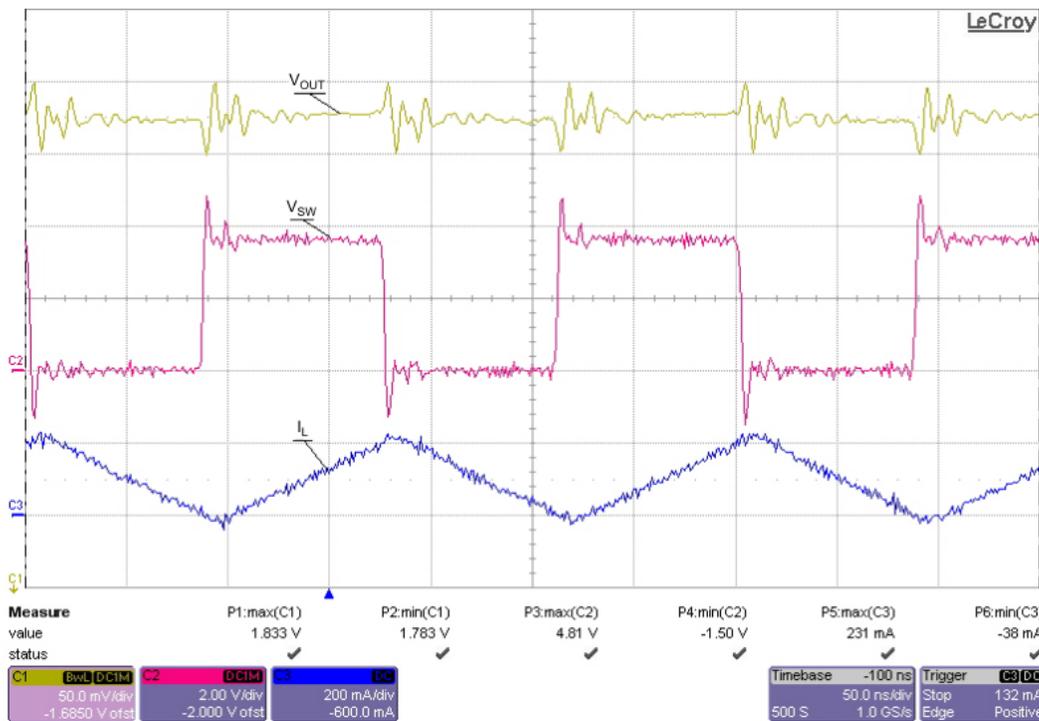


Figure 4. TPS62660 SW Node Behavior, Measured Without a Low-Inductance Probe

The voltage excursions at the SW node are short and require a high bandwidth to see. Turn off the bandwidth limiting on the oscilloscope to allow these voltage excursions to be seen fully. Figure 5 shows how bandwidth limiting creates a nice smooth curve, but does not show the actual SW node behavior. The waveform in Figure 5 uses exactly the same operating conditions and measurement technique as Figure 2, except that 20-MHz bandwidth limiting is turned on in Figure 5. This bandwidth limiting does not show the true SW node signal.

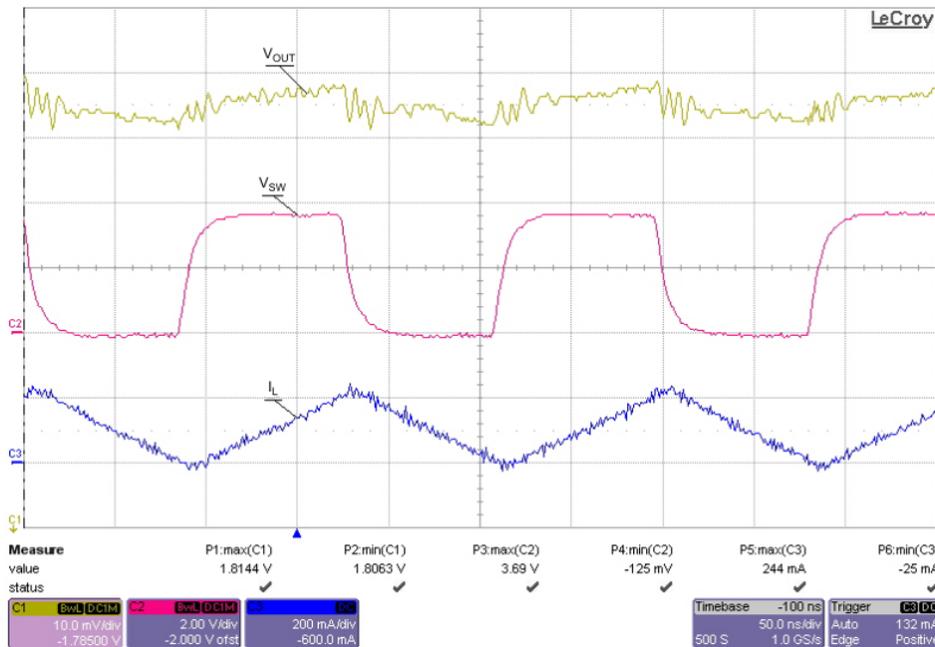


Figure 5. TPS62660 SW Node Behavior, With Low-Inductance Probe but With Bandwidth Limiting

These two techniques, low-inductance probing and using the full bandwidth, reduce coupled noise and allow the oscilloscope to accurately capture the full voltage excursions at the SW node.

4 Good Buck Converter Layout Practices

Practicing good layout techniques for buck converters reduces EMI and helps the buck converter operate smoothly. The most important component to place is the input capacitor. Place this as close to the IC as possible, minimizing the distance between the capacitor ground pad and the IC ground pad, as well as minimizing the distance between the input voltage connections of the two. Poor input capacitor placement can cause excessive positive overshoot. Next, the inductor should be placed close to the IC so that the area of the SW node is small. This reduces EMI, because this area, switching from below ground to V_{IN} , is smaller and therefore does not radiate as much. Finally, the output capacitor completes the circuit. Keep the distance around the loop of the low-side MOSFET, inductor, and output capacitor as small as possible. Poor output capacitor placement can cause excessive negative undershoot.

These steps create low-inductance ground-return loops and minimize EMI. The part functions with non-ideal layouts as long as the absolute maximum SW node rating (7 V, not -0.3 V) is not exceeded. As the parasitic inductances increase due to non-optimal component placement or routing, the voltage stress to the SW pin and the EMI increase. Increasing EMI does not damage the IC but could cause problems to the overall system.

As an example of what poor layout can do, compare Figure 6 and Figure 7. Figure 6 shows a plot of the standard TPS62240 EVM, while Figure 7 shows this same EVM with poor output capacitor placement. The output capacitor in Figure 7 has a much longer ground-return loop back to the IC than does the circuit in Figure 6. A ripple of about 500 mV occurs with this poor placement. Compare this to the 20-mV ripple that occurs normally. Test conditions for both Figure 6 and Figure 7 are: $V_{IN} = 6$ V, $V_{OUT} = 1.8$ V, and $I_{OUT} = 300$ mA.

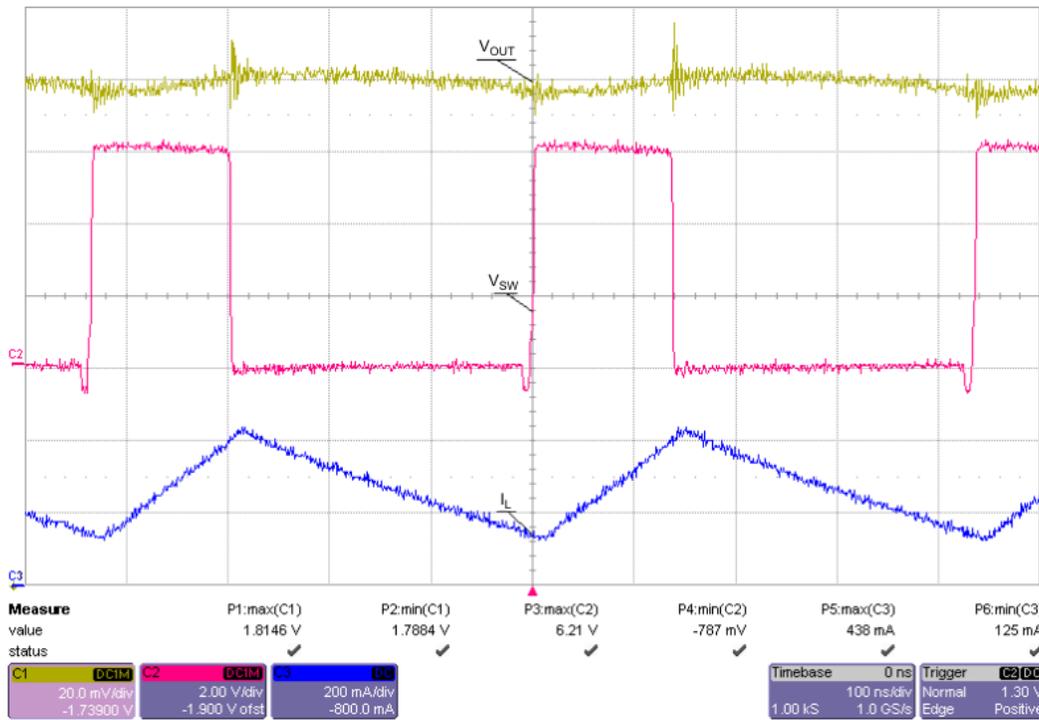


Figure 6. TPS62240 EVM, Good Output Capacitor Placement

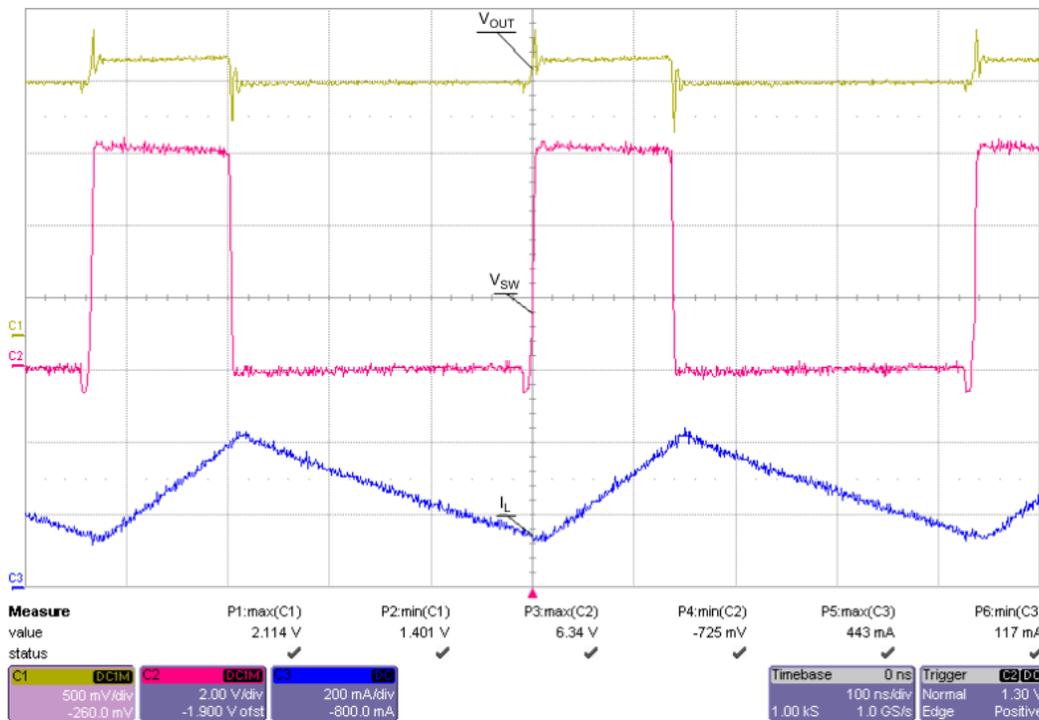


Figure 7. TPS62240 EVM, Poor Output Capacitor Placement

5 Conclusion

Switching operation of synchronous buck converters causes the SW node to briefly exceed its absolute maximum ratings of typically -0.3 V and $V_{\text{IN}} + 0.3\text{ V}$. This is allowed because those ratings are dc ratings and are not violated by short voltage excursions caused by the inductor current forced through a MOSFET body diode during dead time. These voltage excursions are normal and expected behavior for a synchronous buck converter. Through good board layout and proper measurement technique, this behavior is properly measured and minimized, and the EMI of the TPS62xxx-based power supply is reduced.

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