Fault Tree Analysis (FTA)

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ABSTRACT

ASIC level FTA used in automotive applications in cabin temperature environment. FTA analysis completed from perspective of fault(s) causing hazard regardless of time when fault(s) occur. This could be from time \( t = 0 \) onward.

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ABBREVIATIONS

<table>
<thead>
<tr>
<th>AMP</th>
<th>Amplifier</th>
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<tbody>
<tr>
<td>BG</td>
<td>Bandgap</td>
</tr>
<tr>
<td>BVDSS</td>
<td>Drain Source Breakdown Voltage</td>
</tr>
<tr>
<td>BW</td>
<td>Bond Wire</td>
</tr>
<tr>
<td>COMP</td>
<td>Comparator</td>
</tr>
<tr>
<td>EPB</td>
<td>Electronic Park Brake</td>
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<tr>
<td>IDDQ</td>
<td>Quiescent Supply Current</td>
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<td>OVST</td>
<td>Over Voltage Stress Test</td>
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<tr>
<td>PT</td>
<td>Production Test</td>
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<tr>
<td>PTAT</td>
<td>Proportional to Absolute Temperature</td>
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<tr>
<td>REF</td>
<td>Reference</td>
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<tr>
<td>REG</td>
<td>Regulator</td>
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<tr>
<td>S/C</td>
<td>Short Circuit</td>
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<tr>
<td>SOA</td>
<td>Safe Operating Area</td>
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<tr>
<td>URA</td>
<td>Unintended Relay Actuation</td>
</tr>
<tr>
<td>V5AOV</td>
<td>V5A Regulator Over Voltage</td>
</tr>
<tr>
<td>V5OV</td>
<td>V5 Regulator Over Voltage</td>
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</tbody>
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1 References

SLVS726 - 3-V TO 6-V INPUT, 6-A OUTPUT SYNCHRONOUS BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™) - January 2007 (http://www.ti.com/lit/gpn/tps54610-q1)
2 Diagrams

Figure 1. Device Block Diagram
Figure 2.  TPS54310-Q1 Undervoltage Fault Tree
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Faulty Regulation Fault Tree

Figure 3. Faulty Regulation Fault Tree
Figure 4. Faulty Voltage Monitoring Fault Tree
Figure 5. HS Pre-Driver Failure Fault Tree
Voltage Reference Failure Fault Tree

Figure 6. Voltage Reference Failure Fault Tree
Figure 7. OSC Frequency Setting Failure
Figure 8. LS Pre-Driver Failure Fault Tree
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VIN Supply failure

VIN UV

VIN UVLO Monitor Failure

VIN PIN FAULT

VIN pin and/or bond wire fault

VIN LOW

VIN Supply Voltage Low

VIN LOW

VIN supply low

VIN LOW

Q=5.200e-5

VIN UVLO FAULT

Q=1.300e-5

VIN supply low

VIN UV

Q=6.760e-10

Figure 9. VIN Failure Fault Tree
Figure 10. VSENSE Power Good Detection failure fault tree
Figure 11. Set/Reset Circuit Failure fault tree
Figure 12. PWM Generation failure fault tree
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Figure 25. Adaptive PWM Control Circuit fault tree importance diagram
3 Hazards

a. Faulty Switch Regulator leading to undervoltage condition

4 Analysis

4.1 Description

Cut Set: A group of events which will cause system failure when occurring together.

1\textsuperscript{st} Order Cut Set: Single event failure causing hazard.

2\textsuperscript{nd} Order Cut Set: Two failing events causing hazard.

3\textsuperscript{rd} Order Cut Set: Three failing events causing hazard.

4\textsuperscript{th} Order Cut Set: Four failing events causing hazard.

Base Event: Description of base events in associated fault tree diagram. Base events and their description referenced to TI’s design database.

4.2 Faulty Switch Regulator Cut Sets

Hazard: Faulty Switch regulator leading to under voltage condition.

For this hazard a total 36 individual cut sets have been analyzed.

5 Conclusion

ASIC level hazard FTA completed. Switch regulator proactive system level monitoring and protection considerations were included.
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