Application Report
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Introduction to Logic

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ABSTRACT

Logic circuits are the building blocks of the digital world. Computers and electronics use 1s and 0s (bits) to transfer data. In the physical world, the 1s and 0s are represented by voltages on a wire, on microscopic traces within an integrated circuit, or on a copper printed circuit board (PCB) trace. Computers perform calculations and store data by using combinational and sequential logic circuits. There are many different types of logic circuits that will be described in this report, including logic gates, registers, flip-flops, and more. These devices receive the 1s and 0s as voltages on their inputs, and they perform specific operations on those signals to produce an output. When used in the proper sequence, these devices can manipulate the signals in such a way that can result in anything from a simple adding circuit to a fully-functional supercomputer.

TI makes microcontroller units, which contain millions of small logic circuits used to perform complex operations. However, TI also makes the individual building blocks as integrated circuits (ICs) that engineers can use to build smaller-scale digital logic into their own systems. These individual building blocks can also be used for voltage translation or signal conditioning.

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1 Combinational Logic Gates

Combinational logic gates, or simply "logic gates", are the simplest type of logic circuits. They produce an output that is either 1 (high) or 0 (low) depending in the states of one or more of their inputs. In other words, they perform the basic functions of Boolean algebra. Logic gates are the building blocks for more complicated logic.

Figure 1 describes each type of logic gate.

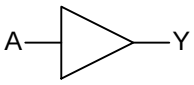
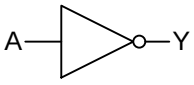
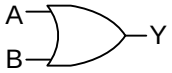
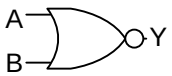
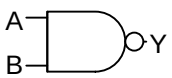
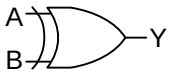
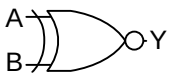
Gate name and symbol	Function description	Truth table
Buffer  $Y = A$	Output matches the input.	A Y 0 0 1 1
Inverter  $Y = \overline{A}$	Output is the opposite of the input.	A Y 0 1 1 0
OR Gate  $Y = A + B$	Output is high if at least one input is high.	A B Y 0 0 0 0 1 1 1 0 1 1 1 1
AND Gate  $Y = A \bullet B$	Output is high only if all inputs are high.	A B Y 0 0 0 0 1 0 1 0 0 1 1 1
NOR Gate  $Y = \overline{A + B}$	Output is high only if none of the inputs are high.	A B Y 0 0 1 0 1 0 1 0 0 1 1 0
NAND Gate  $Y = \overline{A \bullet B}$	Output is high unless all inputs are high.	A B Y 0 0 1 0 1 1 1 0 1 1 1 0
XOR Gate  $Y = A \oplus B$	Output is high only if an odd number of inputs are high.	A B Y 0 0 0 0 1 1 1 0 1 1 1 0
XNOR Gate  $Y = \overline{A \oplus B}$	Output is high only if an even number of inputs are high.	A B Y 0 0 1 0 1 0 1 0 0 1 1 1

Figure 1. Combinational Logic Gates and their Functions

1. Gate name and symbol: The name and standard symbol associated with the gate, including a standard equation used to describe the function it performs.
2. Function description: A verbal description of what the gate does.
3. Truth table: A table describing what happens to the output at every possible combination of the inputs. In general, inputs are designated "A, B, C, ..." while the output is designated with "Y". In truth tables, sometimes there is an "X" instead of 0 or 1 listed as an input state. This "X" refers to "Don't Care", and means that particular input has no effect on the output.

The OR, AND, NOR, NAND, XOR, and XNOR gates are not limited to 2 inputs. For example, a 3-input AND gate, like the SN74LVC1G11, requires that inputs A, B, and C are all high before output Y will be high.

Many TI devices contain multiple independent logic gates. For example, the SN74LVC2G08 contains 2 separate AND gates, and the SN74LVC32244 contains 32 buffers.

2 Sequential Logic

Other logic circuits are designed for moving and storage of 1s and 0s. Often, but not always, these devices will have what is known as a "Clock" input. Most commonly, the clock input is a square-shaped waveform that runs at a constant frequency and controls when the device performs a certain action. For example, a device may be designed to output a specific value or move a bit of information when the rising edge of the clock input occurs.

2.1 Flip-Flops

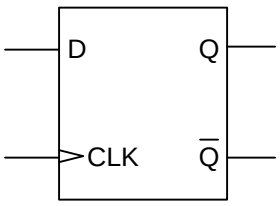
Flip-flops are sequential logic circuits that can store one or more bits. While their data inputs can change constantly, their outputs will change only when a "clock edge" occurs. A clock edge is defined as a change in state of the "Clock" input pin on the device. Usually, any device function will be triggered by the positive (0 to 1) clock edge.

There are several types of flip-flops, but the D-type and JK-type are the most common in TI's portfolio.

2.1.1 D-type Flip-Flop

The D-type flip-flop takes the D input and pushes its value to the Q output on the next clock edge. It also pushes the inverse of D to the $\overline{Q}$ output. D-type flip-flops can be used for temporary data storage; for example, 8 D-type flip-flops connected to the same clock line will be able to store one byte of data on each clock edge. The SN74AUC1G79 is an example of a TI 1-bit D-type flip-flop.

Symbol



Truth Table

D	CLK	Q	$\overline{Q}$
0	↑	1	0
1	↑	0	1
X	0	Q_0	$\overline{Q}_0$
X	1	Q_0	$\overline{Q}_0$

The D-type flip-flop passes the value of D to the Q output, and the inverse of D to the Q_0 output, when a clock edge occurs. Most devices function on the positive clock edge.

Functional Block Diagram

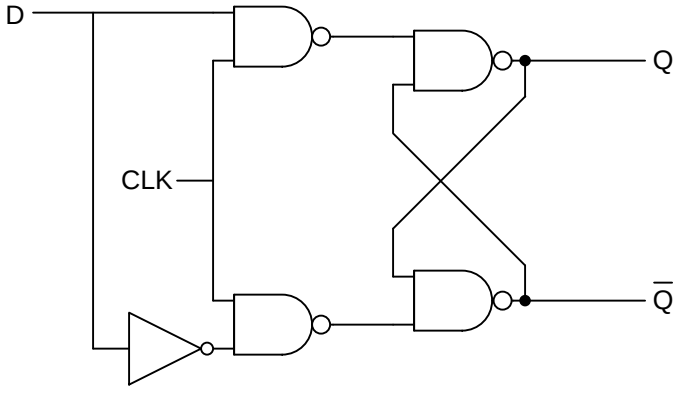
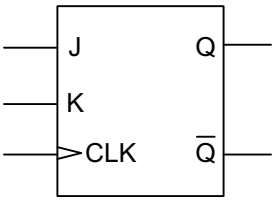


Figure 2. D-Type Flip-Flop

2.1.2 J-K Flip-Flop

The J-K flip-flop function is slightly more complicated than the D-type flip-flop. However, it can be converted to a D flip-flop by placing an inverter in front of the K input and tying the input of that inverter to the J input. The SN74LVC112A is an example of a TI dual J-K flip-flop that is triggered on the negative edge of the clock pulse.

Symbol



Truth Table

J	K	CLK	Q	$\overline{Q}$
0	0	↓	Q_0	$\overline{Q}_0$
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	$\overline{Q}_0$	Q_0
X	X	0	Q_0	$\overline{Q}_0$
X	X	1	Q_0	$\overline{Q}_0$

The Q output of the J-K flip-flop output takes the value of J if J and K are different. If J and K are both 0, the output stays the same. If J and K are both 1, the output toggles.

Functional Block Diagram

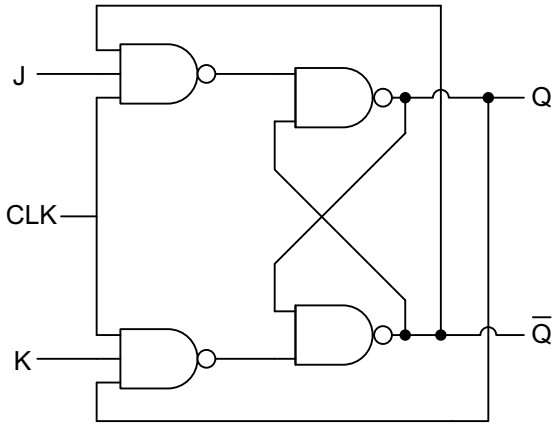


Figure 3. J-K Flip-Flop

2.2 Shift Registers

Shift registers are chains of flip-flops (usually D-type) that propagate data through the device after each valid clock edge. For example, for an 8-bit shift register, if the data input is a 1 and the clock is pulsed 8 times, then a 1 will be stored in all registers. If the input is 1 for 4 clock pulses, then 0 for another 4 clock pulses, then the final 4 bits of the shift register will be 1s and the first 4 bits of the shift register will be 0. These devices can be used in many different applications, including driving a string of flashing LEDs or scanning a keyboard for key press activity. The SN74LV164A is an example of a TI shift register.

2.3 Counters

Counters are devices that count in binary, starting with 0, 1, 10, 11, 100, and so on. Each time a clock edge occurs, the value stored inside increments by 1. There are also counters that start at the maximum value and decrement during each clock cycle. Some even have specific flags for when a count has been finished. Counters are generally used to divide the frequency of a clock signal. The SN74HC393 is an example of a dual 4-bit binary counter from TI.

3 What are 1 and 0 in the Real World?

So far in this document, we have discussed inputs and outputs of logic circuits as being "high" (1) or "low" (0). But what does this mean exactly?

In reality, different families of discrete logic ICs treat "high" and "low" differently. For example, some devices will register 0.7 V at the input as a "high", while on other devices, 0.7 V is not enough to reach the switching threshold and is still considered a "low".

The application report Understanding and Interpreting Standard-Logic Data Sheets has lots of useful information on every specification in logic datasheets, but we will discuss the relevant specifications for input and output voltage levels here. The most common input/output level standards are CMOS and TTL, which can have different voltage levels and are described by the levels in Figure 4.

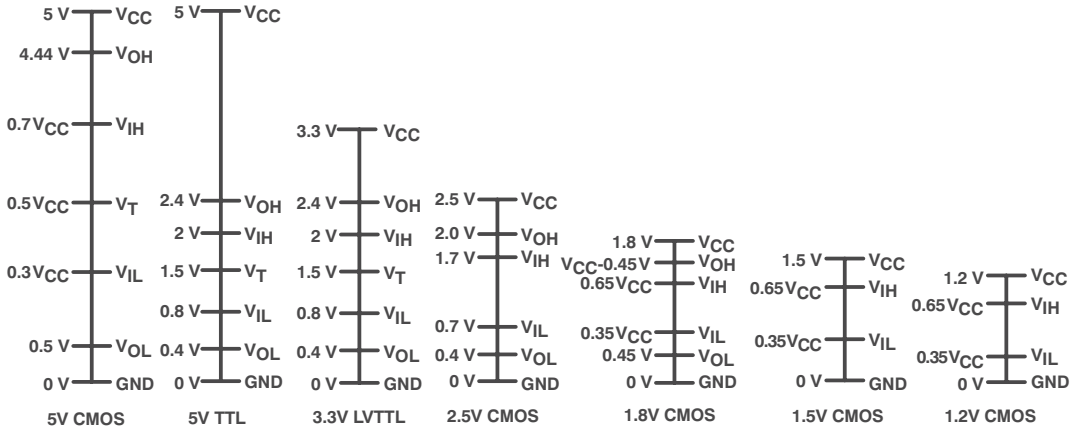


Figure 4. Common Switching Input and Output Levels

- V_{CC}: The supply voltage of the device
- V_{OH}: The minimum allowed "high" output voltage for a device using that particular logic level standard. For example, a 5-V CMOS device only has a valid output "high" if that output is at least 4.44 V.
- V_{IH}: The minimum allowed input voltage for an input to be considered "high"
- V_T: The actual point where the switching occurs from low to high. This is typically not specified in TI datasheets. In reality, there is some variance here, and therefore TI specifies V_{IH} and V_{IL} as maximum and minimum margins for this switching threshold to occur.
- VIL: The maximum allowed input voltage for an input to be considered "low"
- VOL: The maximum allowed "low" output voltage for a device using that particular logic level standard. For example, a 5-V CMOS device only has a valid output "low" if the output is 0.5 V or less.

Therefore, when designing a system, it is critical that the designer should choose parts whose outputs are compatible with the receiver's inputs. For example, 5-V CMOS outputs are compatible with 5-V TTL inputs because the V_{IL} for 5-V CMOS is 4.44 V, which is greater than the 2-V V_{IH} required for a 5-V TTL input to be considered "high". In addition, the 0.5-V V_{OL} for 5-V CMOS is less than the minimum 0.8-V V_{IL} of the 5-V TTL standard. However, a 5-V TTL output should not go into a 5-V CMOS input because the 5-V TTL V_{OL} is allowed to be as low as 2.4 V, which is not high enough to guarantee a "high" on the CMOS device; the V_{IH} for 5-V CMOS is 0.7 × 5 V = 3.5 V.

3.1 Output Current, V_{OH}, and V_{OL}

Most logic circuits can be thought of as having the same types of output characteristics. That is, for any logic circuit, the output section of the device (regarding its performance with voltage, current, and speed) behaves similarly to a buffer in the same logic family.

TI datasheets usually specify V_{OH} and V_{OL} at different values of V_{CC} and different input/output current values. When a logic circuit outputs a "high", current is flowing out (I_{OH}) of the device into a load. That load can be a resistor, LED, other logic circuit, or any other type of circuit element. However, the more current that flows out of the device, the lower its output voltage will be. This is due to voltage drops within the output stage of the device itself. TI datasheets recommend a safe operating current that does not drop the V_{OH} below the standard that the device falls under (5-V TTL, 1.8-V CMOS, and so forth). At extremely small output current values, most logic circuits will output a voltage equal to or very close to V_{CC}. See Figure 5.

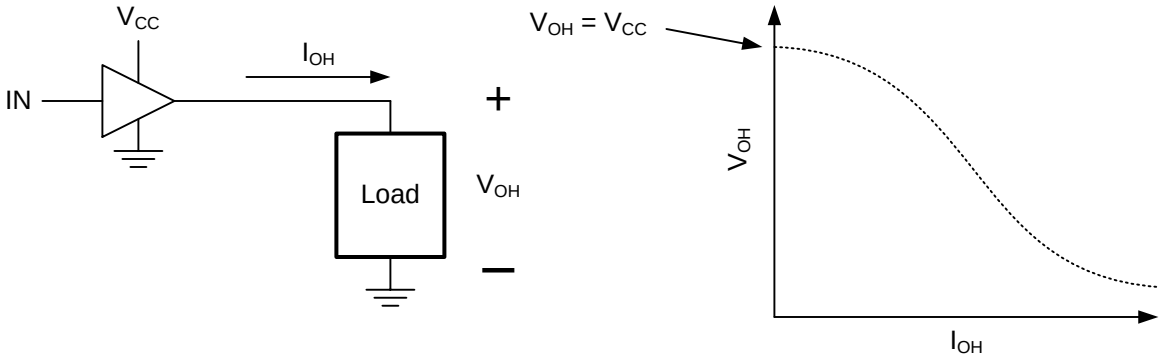


Figure 5. Typical V_{OH}/I_{OH} Relationship for Logic Circuits

Similarly, when the device outputs a "low", current flows into the device. In this case, more current flowing into the device can increase the V_{OL}, which should ideally be 0 V at low currents.

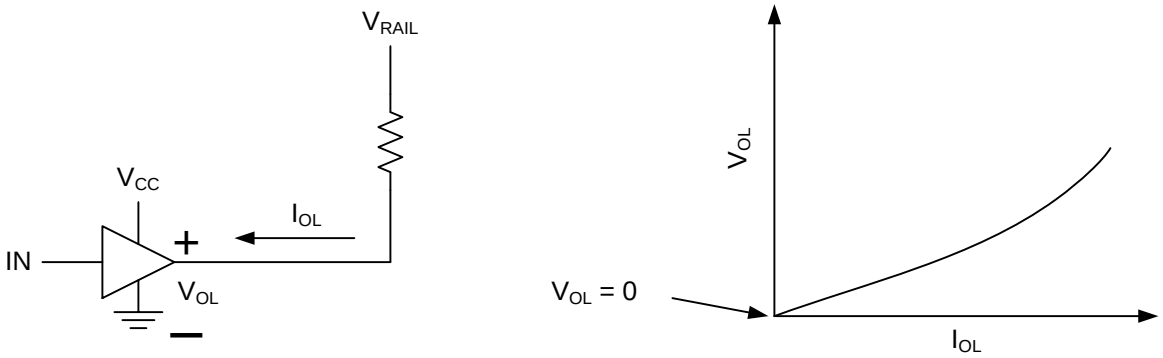


Figure 6. Typical V_{OL}/I_{OL} Relationship for Logic Circuits

Most logic circuits have "push-pull" outputs, meaning that they can provide current and sink current. Some logic circuits have "open-collector" or "open-drain" outputs, which means that they can only sink current and rely on an external pullup resistor to provide the "high" logic level. For an "open-collector" or "open-drain" device, there are no V_{OH} or I_{OH} specifications.

4 Logic Families

You may notice different nomenclature in TI part numbers. For example, TI produces many different types of single-bit buffers, including the SN74AUC1G34 and SN74LVC1G34. We classify these devices as being from two different "families". While they perform the same function, their specifications may be different. For example, the AUC device is characterized to operate at 0.8-V V_{CC}, but the LVC device is not. Additionally, the LVC device is characterized to provide up to 24 mA of output current while retaining its valid CMOS output levels, while the AUC device cannot provide as much current. Family selection is important when considering which logic circuit you pick for your design. A list of families and a short description of each can be found in Understanding and Interpreting Standard-Logic Data Sheets.

5 Additional Technical Reading

This document is intended to give a brief overview of TI logic and introduce the reader to specific devices and documentation. TI has a wide variety of application reports targeted at different applications and issues engineers may encounter. The following is a brief list of application reports. The full list of logic documents is found here.

- Understanding and Interpreting Standard-Logic Data Sheets is the most comprehensive overview of datasheet parameters and specifications for TI logic circuits.
- Voltage-Level Translation with the LSF Family explains how to use TI's LSF0x0x family of devices to translate between different voltage levels in applications where different logic signaling standards are used.
- Power-Up Behavior of Clocked Devices describes dangers of assuming certain output states when using flip-flops and registers - and what to do about it.
- Use of the CMOS Unbuffered Inverter in Oscillator Circuits describes a low-cost way to generate a clock signal.
- Power-up 3-State Circuits in TI Standard Logic Devices describes levels of isolation in TI logic circuits. This is especially useful in systems where not all devices are powered on at the same time.
- Implications of Slow or Floating CMOS Inputs describes the unwanted effects of leaving a logic input floating (unconnected) and elaborates on the "Input Transition Rise or Fall Rate" specification required of many devices.
- Implications of Slow or Floating CMOS Inputs describes the equations used to calculate the typical power consumption of a logic circuit in your design.
- Design Considerations for Logic Products contains a collection of application reports targeted at TI's legacy logic, including proper PCB layout, characterization information, and application-specific design circuits.
- How to Select Little Logic describes selection and design guidelines for TI's Little Logic circuits. Little Logic includes TI's smallest-package, 1-to-3 gate parts.

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