FET Configurations for the bq76200 High-Side N-Channel FET Driver

Taylor Vogt
Battery Management Solutions – Monitoring and Protection

ABSTRACT
The bq76200 is a low-power, high-side, N-Channel MOSFET driver that can be utilized in a variety of FET configurations to assist the user’s battery protection system from faults such as a cell’s undervoltage and overvoltage or a short circuit. The following material is aimed to portray various applications of the bq76200 with several different configurations of FETs, pack voltages, and cell counts that will represent the driver’s functionality under each setup. These configurations were chosen to portray the optimal functionality of the part as well as to define the parameters of applicability in order to present examples where a setup may need debugging.

Contents
1 Introduction ................................................................. 2
2 Test Configurations Table .................................................. 2
3 Main Test Setup ............................................................... 4
4 Test Data ........................................................................ 5
5 Pre-Discharge ................................................................. 29
6 VDDCP Capacitance Reference Table ...................................... 33
7 Data Conclusions .............................................................. 34
8 References ..................................................................... 34

List of Figures
1 Main Test Setup Schematic .............................................. 4
2 CHG and DSG FETs Arranged in Series ................................. 5
3 1xDFET DSG Turn-Off After UV ........................................ 6
4 1xCFET CHG Turn-Off After OV ........................................ 6
5 1x DFET DSG Fall After SC ................................................ 7
6 DSG FET With Added Cgd .................................................. 8
7 DSG Fall After SC Without Added Cgd ................................. 8
8 DSG Fall After SC With Added Cgd ...................................... 9
9 2xCFET/2xDFET Schematic ............................................. 10
10 2xDFET DSG Fall After Undervoltage of a Cell ...................... 11
11 2xCFET CHG Fall After Overvoltage of a Cell ...................... 11
12 2xDFET DSG Fall After Short Circuit Occurs ....................... 12
13 4xCFETs and 4xDFETs in Parallel .................................... 13
14 4xCFETs and 4xDFETs in Series ....................................... 14
15 4xDFET DSG Turn-Off After UV ....................................... 14
16 4xCFET CHG Turn-Off After OV ....................................... 15
17 4xDFET DSG Turn-Off After SC ....................................... 15
18 4xCFETs and 8xDFETs in Parallel ..................................... 16
19 4xCFETs and 12xDFETs in Parallel ................................... 18
20 8xCFET/8xDFET Schematic ............................................ 20
1 Introduction

The bq76200 high-side FET driver can be used in battery protection systems in order to provide switching between normal operating modes and fault conditions. Faults such as a cell’s undervoltage and overvoltage and short circuit were simulated across the following set of FET and pack voltage configurations in order to portray the switching times of the CHG and DSG signals, which when becoming high, allow the battery access to charging and discharging, respectfully.

2 Test Configurations Table

Table 1 contains the test configurations data.

<table>
<thead>
<tr>
<th>Name of Setup</th>
<th>Companion Devices</th>
<th>Pack Configurations</th>
<th>CHG FETs</th>
<th>DSG FETs</th>
<th>FET Arrangement</th>
</tr>
</thead>
<tbody>
<tr>
<td>940 - 1x FETs</td>
<td>bq76940 + bq78350</td>
<td>48 V, 36 V</td>
<td>1x</td>
<td>1x</td>
<td>Series</td>
</tr>
<tr>
<td>940 - 2x FETs</td>
<td>bq76940 + bq78350</td>
<td>48 V, 36 V</td>
<td>2x</td>
<td>2x</td>
<td>Series</td>
</tr>
<tr>
<td>940 - 4x FETs</td>
<td>bq76940 + bq78350</td>
<td>48 V, 36 V</td>
<td>4x</td>
<td>4x</td>
<td>Series</td>
</tr>
</tbody>
</table>
## Table 1. Test Configurations (continued)

<table>
<thead>
<tr>
<th>Name of Setup</th>
<th>Companion Devices</th>
<th>Pack Configurations</th>
<th>CHG FETs</th>
<th>DSG FETs</th>
<th>FET Arrangement</th>
</tr>
</thead>
<tbody>
<tr>
<td>940 - 8x FETs</td>
<td>bq76940 + bq78350</td>
<td>48 V, 36 V</td>
<td>8x</td>
<td>8x</td>
<td>Series</td>
</tr>
<tr>
<td>940 - 12x FETs</td>
<td>bq76940 + bq78350</td>
<td>48 V, 36 V</td>
<td>12x</td>
<td>12x</td>
<td>Series</td>
</tr>
<tr>
<td>940 - 4:8x FETs</td>
<td>bq76940 + bq78350</td>
<td>48 V, 36 V</td>
<td>4x</td>
<td>8x</td>
<td>Parallel</td>
</tr>
<tr>
<td>940 - 4:12x FETs</td>
<td>bq76940 + bq78350</td>
<td>48 V, 36 V</td>
<td>4x</td>
<td>12x</td>
<td>Parallel</td>
</tr>
<tr>
<td>940 - Parallel FETs</td>
<td>bq76940 + bq78350</td>
<td>48 V, 36 V</td>
<td>4x</td>
<td>4x</td>
<td>Parallel</td>
</tr>
<tr>
<td>930 - 1x FETs</td>
<td>bq76930 + bq78350</td>
<td>36 V, 24 V</td>
<td>1x</td>
<td>1x</td>
<td>Series</td>
</tr>
<tr>
<td>930 - 8x FETs</td>
<td>bq76930 + bq78350</td>
<td>36 V, 24 V</td>
<td>8x</td>
<td>8x</td>
<td>Series</td>
</tr>
<tr>
<td>930 - 4:8x FETs</td>
<td>bq76930 + bq78350</td>
<td>36 V, 24 V</td>
<td>4x</td>
<td>8x</td>
<td>Parallel</td>
</tr>
<tr>
<td>930 - Parallel FETs</td>
<td>bq76930 + bq78350</td>
<td>36 V, 24 V</td>
<td>4x</td>
<td>4x</td>
<td>Parallel</td>
</tr>
<tr>
<td>920 - 1x FETs</td>
<td>bq76920 + bq78350</td>
<td>14.4 V, 18 V</td>
<td>1x</td>
<td>1x</td>
<td>Series</td>
</tr>
<tr>
<td>920 - 8x FETs</td>
<td>bq76920 + bq78350</td>
<td>14.4 V, 18 V</td>
<td>8x</td>
<td>8x</td>
<td>Series</td>
</tr>
<tr>
<td>920 - 4:8x FETs</td>
<td>bq76920 + bq78350</td>
<td>14.4 V, 18 V</td>
<td>4x</td>
<td>8x</td>
<td>Parallel</td>
</tr>
<tr>
<td>920 - Parallel FETs</td>
<td>bq76920 + bq78350</td>
<td>14.4 V, 18 V</td>
<td>4x</td>
<td>4x</td>
<td>Parallel</td>
</tr>
<tr>
<td>940 - Predischarge</td>
<td>bq76940 + bq78350</td>
<td>48 V</td>
<td>8x</td>
<td>8x</td>
<td>Series</td>
</tr>
<tr>
<td>920 - Predischarge</td>
<td>bq76920 + bq78350</td>
<td>18 V</td>
<td>8x</td>
<td>8x</td>
<td>Series</td>
</tr>
<tr>
<td>940 - Max Cells</td>
<td>bq76940 + bq78350</td>
<td>63 V (&quot;54 V&quot;)</td>
<td>8x</td>
<td>8x</td>
<td>Series</td>
</tr>
<tr>
<td>920 - Min Cells</td>
<td>bq76920 + bq78350</td>
<td>10.8 V</td>
<td>2x</td>
<td>2x</td>
<td>Series</td>
</tr>
</tbody>
</table>

- bq76930 and bq76940 Evaluation Module User’s Guide (SLVU925)
- bq76920 EVM User’s Guide (SLVU924)
- bq78350 Technical Reference Manual (SLUUAN7)

**NOTE:** The pack voltages were chosen so that the cells would perform at a nominal voltage of approximately 3.6 V and the corresponding FETs were chosen to best represent an ideal application.

- CSD19536KCS N-channel MOSFETs used for tests:
  - Approximately 9.24 nF $C_L$, $V_{ds}$: 100 V, Current: 150 A

**NOTE:** Several of the tests were performed using the IRFB3207ZPBF FETs which produced similar results.
Main Test Setup

Figure 1. Main Test Setup Schematic
4 Test Data

The following set of data represents the functionality of the bq76200 under various FET configurations and PACK voltages when driving FETs after an undervoltage, overvoltage or short circuit. Due to the increasing voltage difference/AFE among tests only slightly delaying FET switching times, each table of FET configurations will be represented by one set of data that provides a reference for the others.

4.1 1xCFET/1xDFET

FET Arrangement: 1 charge FET (1xCFET), 1 discharge FET (1xDFET) in series

Table 2. 1xFET Configurations

<table>
<thead>
<tr>
<th>AFE</th>
<th># CHG FETs</th>
<th># DSG FETs</th>
<th>PACK Voltage</th>
<th># of Cells</th>
<th>FET Arrangement</th>
<th>VDDCP Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>bq76920</td>
<td>1x</td>
<td>1x</td>
<td>14.4 V, 18 V</td>
<td>4, 5</td>
<td>Series</td>
<td>0.47 µF</td>
</tr>
<tr>
<td>bq76930</td>
<td>1x</td>
<td>1x</td>
<td>24 V, 36 V</td>
<td>6, 10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bq76940</td>
<td>1x</td>
<td>1x</td>
<td>36 V, 48 V</td>
<td>10, 13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4.1.1 Series Configuration

The CHG and DSG FETs are commonly arranged in series in order to support the PCHG feature and to reduce modifications to their design. In this arrangement the FETs will share a common charge path to PACK+ and the user will not need to add extra discharge capacitors for the one path. The following schematic details an ideal setup and construction when utilizing the series FET configuration.

Figure 2. CHG and DSG FETs Arranged in Series

Test: 36 V, 1xFETs, 10 cells, Undervoltage of a cell with a load of 1 A
**Figure 3. 1xDFET DSG Turn-Off After UV**

**Test:** 36 V, 1xFETs, 10 cells, Overvoltage of a cell when charging at 21 V (4.2 V per cell)

**Figure 4. 1xCFET CHG Turn-Off After OV**

**Test:** Short circuit
When using a minimal number of FETs (1–2) under increased battery pack voltages, that is, 48 V, and a short circuit occurs, the CSD19536KCS FETs Cgd capacitance requires an increase of approximately 220 pF in order to provide feedback to keep the gate on as it switches. Otherwise, the FET will jump on and off without being able to recover which eventually results in recovery or shorting of the FET depending on the amount of FETs used and their respective Cgd capacitance. Figure 7 shows the same configuration with 1xFET until it shorts and after the Cgd capacitance was increased, Figure 8 shows the elimination of the gate oscillation without sacrificing switching times.

However, when performing the same tests using the IRFB3207ZPBF FETs, the issue did not occur due to its lower input capacitance of about 6920 pF at 50 V compared to the CSD19536KCS 12000 pF at 50 V. Refer to your FET manufacturer’s data sheet to determine ideal use.

The following schematic displays the Cgd capacitance addition.
Figure 6. DSG FET With Added Cgd

Figure 7. DSG Fall After SC Without Added Cgd
Figure 8. DSG Fall After SC With Added Cgd
4.2 2xCFET/2xDFET

**FET Arrangement:** 2 charge FETs (2xCFET), 2 discharge FETs (2xDFET) in series.

### Table 3. 2xFET Configurations

<table>
<thead>
<tr>
<th>AFE</th>
<th># CHG FETs</th>
<th># DSG FETs</th>
<th>PACK Voltage</th>
<th># of Cells</th>
<th>FET Arrangement</th>
<th>VDDCP Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>bq76920</td>
<td>2x</td>
<td>2x</td>
<td>10.8 V, 14.4 V, 18 V</td>
<td>3, 4, 5</td>
<td>Series</td>
<td>1 µF</td>
</tr>
<tr>
<td>bq76930</td>
<td></td>
<td></td>
<td>24 V, 36 V</td>
<td>6, 10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bq76940</td>
<td></td>
<td></td>
<td>36 V, 48 V</td>
<td>10, 13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 9. 2xCFET/2xDFET Schematic**

**NOTE:** For configurations with multiple CHG or DSG FETs in parallel, 600-Ω ferrite beads were placed each FET gate in order to prevent parasitic oscillations.

**Test:** 10.8 V, 2xFETs, 3 cell, Undervoltage with a 2-A load.
Figure 10. 2xDFET DSG Fall After Undervoltage of a Cell

**Test:** 10.8 V, 3 cell, Overvoltage of a cell when charging at 12.6 V (4.2 V a cell)

Figure 11. 2xCFET CHG Fall After Overvoltage of a Cell

**Test:** 10.8 V, 2xFETs, 3 cell, short circuit
Figure 12. 2xDFET DSG Fall After Short Circuit Occurs
4.3 4xCFET/4xDFET

FET Arrangement: 4 charge FETs (4xCFET), 4 discharge FETs (4xDFET)

<table>
<thead>
<tr>
<th>AFE</th>
<th># CHG FETs</th>
<th># DSG FETs</th>
<th>PACK Voltage</th>
<th># of Cells</th>
<th>FET Arrangement</th>
<th>VDDCP Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>bq76920</td>
<td>4x</td>
<td>4x</td>
<td>14.4 V, 18 V</td>
<td>4, 5</td>
<td>Parallel</td>
<td>2.2 µF</td>
</tr>
<tr>
<td>bq76930</td>
<td>24 V,36 V</td>
<td>6,10</td>
<td>Parallel</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bq76940</td>
<td>36 V, 48 V</td>
<td>10, 13</td>
<td>Series</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE: When using multiple CHG or DSG FETs in parallel with one another, refer to the VDDCP Capacitance Reference table in order to implement a VDDCP capacitance size necessary for the user’s application.

Parallel Configuration

The user may want to configure the CHG and DSG FETs in a parallel configuration in order to support separate charge paths for CHG and DSG. However, this creates a CHG PACK+ path separate from the PACK+ path for the DSG FETs that can manage the voltage level by the PACKDIV feature so the initial intention of the PCHG FET would only be useful for PDSG. Though, these separate CHG and DSG paths do allow the user to support applications with a differing number of CHG and DSG FETs. The following schematic details an ideal setup and construction when utilizing the parallel FET configuration.

Figure 13. 4xCFETs and 4xDFETs in Parallel
**Figure 14. 4xCFETs and 4xDFETs in Series**

**Test:** 36 V, 4xFETs, 10 cells, Undervoltage of a cell with a load of approximately 4 A.

**Figure 15. 4xDFET DSG Turn-Off After UV**
**Test:** 36 V, 4xFETs, 10 cell, Overvoltage of a cell when charging at 42 V (4.2 V per cell)

![Figure 16. 4xCFET CHG Turn-Off After OV](image1)

**Test:** 36 V, 4xFETs, 10 cell, Short circuit

![Figure 17. 4xDFET DSG Turn-Off After SC](image2)
4.4 4xCFET/8xD Fet

FET Arrangement: 4 charge FETs (4xCFET), 8 discharge FETs (8xD Fet) in parallel.

Table 5. 4x8xFET Configurations

<table>
<thead>
<tr>
<th>AFE</th>
<th># CHG FETs</th>
<th># DSG FETs</th>
<th>PACK Voltage</th>
<th># of Cells</th>
<th>FET Arrangement</th>
<th>VDDCP Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>bq76920</td>
<td>4x</td>
<td>8x</td>
<td>14.4 V, 18 V</td>
<td>4, 5</td>
<td>Parallel</td>
<td>2.2 µF</td>
</tr>
<tr>
<td>bq76930</td>
<td></td>
<td></td>
<td>24 V, 36 V</td>
<td>6, 10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bq76940</td>
<td></td>
<td></td>
<td>36 V, 48 V</td>
<td>10, 13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 18. 4xCFETs and 8xD Fet in Parallel
4.5 4xCFET/12xDFET

**FET Arrangement:** 4 charge FETs (4xCFET), 12 discharge FETs (12xDFET) in parallel.

**Table 6. 4x12xFET Configurations**

<table>
<thead>
<tr>
<th>AFE</th>
<th># CHG FETs</th>
<th># DSG FETs</th>
<th>PACK Voltage</th>
<th># of Cells</th>
<th>FET Arrangement</th>
<th>VDDCP Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>bq76940</td>
<td>4x</td>
<td>12x</td>
<td>36 V, 48 V</td>
<td>10, 13</td>
<td>Parallel</td>
<td>4.7 µF</td>
</tr>
</tbody>
</table>
Figure 19. 4xCFETs and 12xDFETs in Parallel
NOTE: The 4x8x and 4x12x parallel configurations show no substantial differences from the series test for the same number of FETs. This is expected as the parallel configuration simply allows differing CHG and DSG FET numbers. The following references to other figures display the functionality of these configurations.

4x8x UV test, refer to Figure 21
4x8x OV test, refer to Figure 16
4x8x SC test, refer to Figure 25
4x12x UV test, refer to Figure 32
4x12x OV test, refer to Figure 16
4x12x SC test, refer to Figure 34
### 4.6 8xCFET/8xDFET

**FET Arrangement:** 8 charge FETs (8xCFET), 8 discharge FETs (8xDFET) in series.

<table>
<thead>
<tr>
<th>AFE</th>
<th># CHG FETs</th>
<th># DSG FETs</th>
<th>PACK Voltage</th>
<th># of Cells</th>
<th>FET Arrangement</th>
<th>VDDCP Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>bq76920</td>
<td>8x</td>
<td>8x</td>
<td>14.4 V, 18 V</td>
<td>4, 5</td>
<td>Series</td>
<td>4.7 µF</td>
</tr>
<tr>
<td>bq76930</td>
<td>8x</td>
<td>8x</td>
<td>24 V, 36 V</td>
<td>6, 10</td>
<td>Series</td>
<td></td>
</tr>
<tr>
<td>bq76940</td>
<td></td>
<td></td>
<td>36 V, 48 V, 54 V</td>
<td>10, 13, 15</td>
<td>Series</td>
<td></td>
</tr>
<tr>
<td>bq76920</td>
<td></td>
<td></td>
<td>48 V</td>
<td>13</td>
<td>Pre-Discharge</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>18 V</td>
<td>5</td>
<td>Pre-Discharge</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 20. 8xCFET/8xDFET Schematic**

**Test:** 48 V, 8xFETs, 13 cells, Undervoltage of a cell with a load of approximately 8 A
Figure 21. 8xDFET DSG Turn-Off After UV

Figure 22. 8xDFET DSG Turn-On After UV Recovery

NOTE: The longer delays in the PACK current recovery from an undervoltage or overvoltage is a result of an instrument response time of the Kikusui PLZ1004W Electronic Load. PACK eventually rises approximately 5ms later in this setup, and will rise quickly as expected when referenced through a resistor.

Test: 48 V, 8xFETs, 10 cell, Overvoltage of a cell when charging at 54.6 V (4.2 V per cell)
Figure 23. 8xCFET CHG Turn-Off After OV

Figure 24. 8xCFET CHG Turn-On After OV Recovery

Test: 48 V, 8xFETs, 13 cell, Short circuit
Figure 25. 8xDFET DSG Turn-Off After SC

NOTE: The following tests are displayed to show the differences between the switching times across consistent FET amounts, but a changed PACK voltage. The change is fairly minimal as opposed to increasing FETs which has a much more profound delay.

Test: 54 V, 8xFETs, 15 cells, Undervoltage of a cell with a load of approximately 8A

Figure 26. 8xDFET DSG Turn-Off After UV
Figure 27. 8xFET DSG Turn-On After UV Recovery

Test: 54 V, 8xFETs, 15 cell, Overvoltage of a cell when charging at 63 V (4.2 V per cell)

Figure 28. 8xCFET CHG Turn-Off After OV
Figure 29. 8xCFET CHG Turn-On After OV Recovery

**Test:** 54 V, 8xFETs, 15 cell, Short circuit

![Graph showing CHG Turn-On After OV Recovery](image)

Figure 30. 8xDFET DSG Turn-Off After SC

![Graph showing DSG Turn-Off After SC](image)
4.7 12xFET/12xFET

**FET Arrangement:** 12 charge FETs (12xCFET), 12 discharge FETs (12xDFET) in series.

### Table 8. 12xFET Configurations

<table>
<thead>
<tr>
<th>AFE</th>
<th># CHG FETs</th>
<th># DSG FETs</th>
<th>PACK Voltage</th>
<th># of Cells</th>
<th>FET Arrangement</th>
<th>VDDCP Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>bq76940</td>
<td>12x</td>
<td>12x</td>
<td>36 V, 48 V</td>
<td>10, 13</td>
<td>Series</td>
<td>4.7 µF</td>
</tr>
</tbody>
</table>

**Figure 31. 12xCFET/12xDFET Schematic**

**Test:** 48 V, 12xFETs, 13 cells, Undervoltage of a cell with a load of approximately 10 A
**Figure 32. 12xDFET DSG Turn-Off After UV**

**Test:** 48 V, 12xFETs, 13 cell, Overvoltage of a cell when charging at 54.6 V (4.2 V per cell)

**Figure 33. 12xCFET CHG Turn-Off After OV**

**Test:** 48 V, 12xFETs, 13 cell, Short circuit
Figure 34. 12xDFET DSG Turn-Off After SC
5 Pre-Discharge

Table 9. Pre-Discharge Configurations

<table>
<thead>
<tr>
<th>AFE</th>
<th># CHG FETs</th>
<th># DSG FETs</th>
<th>PACK Voltage</th>
<th># of Cells</th>
<th>FET Arrangement</th>
<th>VDDCP Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>bq76940</td>
<td>8x</td>
<td>8x</td>
<td>48 V</td>
<td>13</td>
<td>Series</td>
<td>4.7 µF</td>
</tr>
<tr>
<td>bq76920</td>
<td></td>
<td></td>
<td>18 V</td>
<td>5</td>
<td>Series</td>
<td></td>
</tr>
</tbody>
</table>

When attempting to connect the battery in systems where the load has an extremely high capacitance, the battery may short circuit and attempt to recover, resulting in DSG failing to switch on and PACK spiking to a low voltage which slowly dissipates in the load resistance and repeats the cycle. Figure 37 portrays this behavior when the bq76200 attempts to switch DSG on. After some time, PACK may slowly increase its initial voltage spike to a point where DSG may turn on but that is situationally unreliable.

In order to avoid this problem, consider using a pre-discharge FET in order to slowly push PACK and DSG into their normal operating voltage. The following schematic displays the use of the PDSG FET and how it can be implemented within an 8xFET configuration in systems where the bq76200 PCHG function is not needed for battery precharge. Figure 39 shows PDSG turn on and the effect it has on resolving the PACK and DSG turn on.

![Figure 35. Battery with High Capacitive Load](image-url)
Figure 36. Pre-Discharge Schematic
NOTE: The oscilloscope could not capture the rapid jump of DSG_EN and pack current which occurs exactly as the PACK begins a new cycle of dissipating. Figure 38 shows the spike zoomed in.
Problem resolved when PDSG_EN is turned on causing the PDSG FET to slowly ramp up PACK+ to turn on DSG

**Figure 39. DSG Spike and Current Spike Problem Resolved**

Using the pre-discharge feature, program the microcontroller to enable PDSG through the PCHG_EN pin. This is beneficial when using a high-capacitive load that essentially shorts DSG_EN and PACK which then attempt to recover in a cycle.
Due to the rising load capacitance as we increase the total number of FETs, the bq76200 requires an increase in the charge pump capacitor across the VDDCP and BATT terminals. If the capacitor is not increased as FETs are added, at some threshold the FETs will not comply and VDDCP will begin to cycle between slightly on and off states as there is not enough power to switch the FETs. Table 10 represents a reference for certain FET configurations and the recommended VDDCP capacitance size for each total FET amount.

Once more than approximately 4 total FETs are used, the charge pump capacitor must be increased from the base 470 nF capacitor at a ratio of roughly 23.5 charge pump capacitance (C_{VDDCP}) to total FET input capacitance (C_L). These tests were done with the TI CSD19536KCS FET which carries an input capacitance of about 9.25 nF. Subsequently, C_L was calculated by rounding the individual FET capacitance up to 10 nF to support applications with potentially higher FET capacitances. Note that as the charge pump capacitance increases, the longer the charge pump turn on time.

Table 10. VDDCP Capacitance Reference

<table>
<thead>
<tr>
<th>Total # of DSG and CHG FETs</th>
<th>C_C (nF) (Total FET Capacitance)</th>
<th>C_{VDDCP} (nF) (Theoretical Minimum Charge Pump Capacitance)</th>
<th>C_{VDDCP} (nF) (Actual Used Capacitance)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>20</td>
<td>470</td>
<td>470</td>
</tr>
<tr>
<td>4</td>
<td>40</td>
<td>940</td>
<td>1000</td>
</tr>
<tr>
<td>8</td>
<td>80</td>
<td>1880</td>
<td>2200</td>
</tr>
<tr>
<td>12</td>
<td>120</td>
<td>2820</td>
<td>2200</td>
</tr>
<tr>
<td>16</td>
<td>160</td>
<td>3760</td>
<td>4700</td>
</tr>
<tr>
<td>24</td>
<td>240</td>
<td>5640</td>
<td>4700</td>
</tr>
</tbody>
</table>

NOTE: The VDDCP capacitance fault may not occur in every application with more than approximately 4 FETs, for example, tests were successfully completed using the 470 nF with 4xFETs and using the 1000 nF with 8xFETs. Other capacitances used in the test did not meet the theoretical minimum. However, it may not work consistently, and therefore it is more reliable to follow the theoretical minimum value in Table 10 to guide your VDDCP capacitance selection. The recommended minimum VDDCP capacitor C_{CP} = 470 nF.

Figure 40. Example DSG Cycling With Inadequate VDDCP Capacitance
7 Data Conclusions

• Testing with the same number of CHG/DSG FETs using a parallel or series configuration produces similar results.
• In multiple FET configurations, it is important to include a ferrite bead/gate resistance at each FET gate.
• As FETs are increased, refer to Table 10 to determine an suitable capacitor.
• FET switching time is significantly delayed as FETs are increased, and less affected as the voltage increases.
• In higher power applications and minimal FET amounts, it may be useful to add Cgd capacitance to the FETs to provide feedback to the gate.
• The CHG FETs seem to recover slower than the DSG FETs.

8 References

1. bq76200 High Voltage Battery Pack Front-End Charge/Discharge High-Side NFET Driver (SLUSC16)

Revision History

<table>
<thead>
<tr>
<th>Changes from Original (November 2015) to A Revision</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed Q1 type, C5 value 2.2 to 470 nF, and FETs to FET in CHG and DSG FETs Arranged in Series schematic.</td>
<td>5</td>
</tr>
<tr>
<td>• Modified CHG and DSG FETs Arranged in Series schematic by adding C8 220 pF, moved wire, removed yellow box in the DSG FET with Added Cgd schematic.</td>
<td>8</td>
</tr>
<tr>
<td>• Changed the Q1 and C5 values in the 2xCFET/2xDFET Schematic.</td>
<td>10</td>
</tr>
<tr>
<td>• Changed Q1 in the 4xCFETs and 4xDFETs in Series schematic.</td>
<td>14</td>
</tr>
<tr>
<td>• Changed the Q1 and C5 value in the 8xCFET/8xDFET Schematic.</td>
<td>20</td>
</tr>
<tr>
<td>• Changed the Q1 and C5 value in the 12xCFET/12xDFET Schematic.</td>
<td>26</td>
</tr>
<tr>
<td>• Changed the Q1 and C5 value in the Pre-Discharge Schematic.</td>
<td>30</td>
</tr>
</tbody>
</table>

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
**IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

**Products**

- **Audio**
  - www.ti.com/audio
- **Amplifiers**
  - amplifier.ti.com
- **Data Converters**
  - dataconverter.ti.com
- **DLP® Products**
  - www.dlp.com
- **DSP**
  - dsp.ti.com
- **Clocks and Timers**
  - www.ti.com/clocks
- **Interface**
  - interface.ti.com
- **Logic**
  - logic.ti.com
- **Power Mgmt**
  - power.ti.com
- **Microcontrollers**
  - microcontroller.ti.com
- **RFID**
  - www.ti-rfid.com
- **OMAP Applications Processors**
  - www.ti.com/omap
- **Wireless Connectivity**
  - www.ti.com/wirelessconnectivity

**Applications**

- **Automotive and Transportation**
  - www.ti.com/automotive
- **Communications and Telecom**
  - www.ti.com/communications
- **Computers and Peripherals**
  - www.ti.com/computers
- **Consumer Electronics**
  - www.ti.com/consumer-apps
- **Energy and Lighting**
  - www.ti.com/energy
- **Industrial**
  - www.ti.com/industrial
- **Medical**
  - www.ti.com/medical
- **Security**
  - www.ti.com/security
- **Space, Avionics and Defense**
  - www.ti.com/space-avionics-defense
- **Video and Imaging**
  - www.ti.com/video
- **TI E2E Community**
  - e2e.ti.com

---

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated