ABSTRACT

In some applications, it may be desired to have a constant dv/dt ramp on the output of the TPS2471x to ensure a constant inrush current. This is often accomplished by adding a capacitor to the gate. This application note describes several considerations that must be taken into account when using this approach.

1 Circuit Overview and Considerations

Fundamentally, the dv/dt control is implemented by adding a capacitor from gate to ground as shown below. The gate pin sources a limited current so the gate pin slowly ramps up. Thus $V_{OUT}$ will slowly ramp and follow the gate. If the load is capacitive the current will be constant and proportional to the dv/dt of $V_{OUT}$.

![Figure 1. Operation of Power Limit Engine](image1)

![Figure 2. Typical Waveforms when Using Soft Start](image2)
Before switching to this method it’s important to take into account some of the drawbacks and limitations of this approach.

- There should not be any series resistance between $C_{SS}$ and the Gate pin. Adding this resistance would lead to undesired behavior during hot short tests.
- This approach results in a slower short circuit response because now the Hot Swap needs to discharge $C_{SS}$, which can be a lot bigger than the $C_{GS}$ of the FET.
- This usually requires a larger timer than a typical power limit based start-up approach. Hence the FET is stressed more during a start into short or a hot short test condition.
- The gate sourcing current will vary depending on the difference between $V_{(SNS,CL)}$ (target current limit or power limit voltage) and the actual $V_{(SNS)}$. This has to be taken into account when working on such designs.

2 Recommended Design Procedure

With the above limitations in mind, if soft start is still desired the following procedure can be used. Note that more detailed design procedure can be performed with a spreadsheet, but this provides a simpler approach that will ensure a robust design.

- First pick a soft start capacitor that will provide the desired typical output slew rate. Suppose a 1 V/ms ramp rate was desired. Then the $C_{SS}$ can be computed to 30 nF (30 µA/(1 V/ms)).
- Then the inrush current should be computed, which would depend on the output cap. If the output capacitor is 1,000 µF, the inrush current will be 1 A (1 V/ms x 1000 µF).
- Next the power limit must be set sufficiently large to ensure that there is sufficient gate current throughout the start-up process. In general, it is recommended to compute the $V_{(SNS,PLIM,MIN)}$ using Equation 1. The 6 mV is the recommended over-drive to ensure 20 µA of sourcing current over process and temperature. Assuming a 1-mΩ sense resistor, $V_{(SNS,PLIM,MIN)}$ of 7 mV is computed.

$$V_{(SNS,PLIM,MIN)} = 6 \text{ mV} + I_{\text{INR}} \times R_{\text{SNS}} = 7 \text{ mV} \tag{1}$$

- Based on this, the lowest value the current should be regulated to is 7 A (7 mV/ 1 mΩ). For a $V_{(IN,MAX)}$ of 14 V, this would imply that the power limit should be set to at least 7 A x 14 V = 98 W.
- Next, it is important to compute how long the timer will run. Note that the timer runs while $V_{GS}$ is less than 5.9 V. In addition to $C_{SS}$, the $C_{GS}$ of the MOSFET needs to be charged as well. Continuing with the example above and assuming a $C_{GS}$ of 10 nF, a conservative value of the timer run time can be computed as follows;

$$t_{\text{TIMER, RUN}} = \frac{(V_{(IN,MAX)} + 5.9 \text{ V}) \times C_{SS} + 5.9 \text{ V} \times C_{GS}}{20 \mu A} = \frac{(14 \text{ V} + 5.9 \text{ V}) \times 30 \text{ nF} + 5.9 \text{ V} \times 5 \text{ nF}}{20 \mu A} = 31.3 \text{ ms} \tag{2}$$

- Finally the timer should be set to have some margin compared to timer runs. 25% margin is recommended. In this case, a timer of at least 39 ms would be recommended.

3 References

*TPS2471x 2.5V to 18V Positive Voltage Power-Limiting Hot-Swap Controllers (SLVSAL2)*
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