ABSTRACT
As aerospace technology continues to develop, the industry has seen a dramatic increase in the lifetime of satellites. With this increase, the operational lifetime of many satellites now surpasses that of the telecom standards they were developed around. Because of this, the need for re-programmability in space applications has also risen [1]. Microsemi® is one company that addresses this need with their SRAM based FPGA, the RTG4™. Modern FPGAs tend to operate at lower voltages and higher currents than their predecessors, and the RTG4 is no exception. FPGA power supply requirements have become more demanding and features such as soft-start and sequencing are required to avoid large inrush currents that could potentially create problems in the regulators upstream. This report demonstrates how TI's space qualified power portfolio can be used to power RTG4 based designs.

Contents
1 RTG4 Electrical Specifications ........................................................................................................... 2
2 RTG4 Power-Up and Power-Down Requirements .............................................................................. 3
3 Demonstrating Space Rated TI Solutions .......................................................................................... 5
4 Conclusion ........................................................................................................................................ 10
5 References ....................................................................................................................................... 11
6 Additional Resources .......................................................................................................................... 11

List of Figures
1 RTG4 Development Board Power Distribution .................................................................................. 4
2 RTG4 Development Board Start-up Sequence ................................................................................... 4
3 RTG4 Modified Development Board Connected to TI Evaluation Modules ......................................... 5
4 RTG4 Modified Development Board Power Distribution Using TI Space Qualified Components ....... 6
5 RTG4 Modified Development Board Power Sequence ...................................................................... 7
6 RTG4 Modified Development Board Fulfilling the First Power-Up Requirement ............................. 7
7 RTG4 Modified Development Board Fulfilling the Second Power-Up Requirement ...................... 8
8 Recommended Grounds-Up RTG4 Power Distribution ................................................................. 9
9 Recommended Grounds-Up RTG4 Power-Up Sequencing. The SD_Vxx Signals Can Be Used for Power-Down Sequences as Needed ............................................................... 9

List of Tables
1 RTG4 Electrical Specifications ........................................................................................................... 2
RTG4 Electrical Specifications

Trademarks

RTG4 is a trademark of Microsemi Corporation. Microsemi is a registered trademark of Microsemi Corporation. All other trademarks are the property of their respective owners.

1 RTG4 Electrical Specifications

All specifications for the RTG4 are taken from Microsemi datasheet (Rev. 4) and application reports [2].

Table 1. RTG4 Electrical Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>DC FPGA core supply voltage. Must always power this pin.</td>
<td>1.14</td>
<td>1.2</td>
<td>1.26</td>
<td>V</td>
</tr>
<tr>
<td>VPP</td>
<td>Power supply for charge pumps (for normal operation and programming). Must always power this pin.</td>
<td>3.15</td>
<td>3.3</td>
<td>3.45</td>
<td>V</td>
</tr>
<tr>
<td>VDDPLL</td>
<td>Power for eight corner PLLs, PLLs in SERDES PCIe/PCS blocks, and FDDR PLL.</td>
<td>3.15</td>
<td>3.3</td>
<td>3.45</td>
<td>V</td>
</tr>
<tr>
<td>SERDES_x_Lyz_VDDAIO</td>
<td>Tx/Rx analog I/O voltage. Low voltage power for lane-y and Lane-z of SERDES_x. It is a +1.2-V SERDES PMA supply.</td>
<td>1.14</td>
<td>1.2</td>
<td>1.26</td>
<td>V</td>
</tr>
<tr>
<td>SERDES_x_Lyz_VDDAPLL</td>
<td>Analog power for SERDES_x PLL lanes yz. It is a +2.5-V SERDES internal PLL supply.</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>SERDES_VDDI</td>
<td>Power for SERDES reference clock receiver 1.8-V supply. Must always power this pin.</td>
<td>1.71</td>
<td>1.8</td>
<td>1.89</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power for SERDES reference clock receiver 2.5-V supply. Must always power this pin.</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Power for SERDES reference clock receiver 3.3-V supply. Must always power this pin.</td>
<td>3.15</td>
<td>3.3</td>
<td>3.45</td>
<td></td>
</tr>
<tr>
<td>SERDES_VREF</td>
<td>Reference voltage for SERDES receiver reference clocks.</td>
<td>0.49 × SERDES_VDDI</td>
<td>0.5 × SERDES_VDDI</td>
<td>0.51 × SERDES_VDDI</td>
<td>V</td>
</tr>
</tbody>
</table>
Table 1. RTG4 Electrical Specifications (continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDIx</td>
<td>1.2-V DC supply voltage for FPGA I/O banks.</td>
<td>1.14</td>
<td>1.2</td>
<td>1.26</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>1.5-V DC supply voltage for FPGA I/O banks.</td>
<td>1.425</td>
<td>1.5</td>
<td>1.575</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.8-V DC supply voltage for FPGA and JTAG I/O banks.</td>
<td>1.71</td>
<td>1.8</td>
<td>1.89</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.5-V DC supply voltage for FPGA and JTAG I/O banks.</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.3-V DC supply voltage for FPGA and JTAG I/O banks.</td>
<td>3.15</td>
<td>3.3</td>
<td>3.45</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DC supply voltage for LVDS25 differential I/O banks.</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DC supply voltage for LVDS33 differential I/O banks.</td>
<td>3.15</td>
<td>3.3</td>
<td>3.45</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DC supply voltage for BLVDS, MLVDS, Mini-LVDS, RSDS differential I/O banks.</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DC supply voltage for LVPECL differential I/O banks.</td>
<td>3.15</td>
<td>3.3</td>
<td>3.45</td>
<td></td>
</tr>
</tbody>
</table>

2 RTG4 Power-Up and Power-Down Requirements

The power-up requirements are based on the VDDPLL and the SERDES_x_Lyz_VDDAIO voltage rails. The only way to not have any power-up sequencing requirements are to hold the RTG4 in reset (by asserting DEVRST_N) until the VDDPLL supply reaches its minimum recommended level and to have the SERDES_x_Lyz_VDDAIO supplies tied to VDD. If this cannot be done however, then the RTG4 voltage rails need to be properly sequenced. In this case, the following requirements apply:

1. VDDPLL must not be the last supply to ramp up and must reach its minimum recommended level before the last supply (VDD or VDDIx) starts ramping up.
2. VDD core and SERDES IO must be powered up in parallel.

There is no power-down requirement if an external 1-kΩ pull-down resistor is used for each critical output that cannot tolerate an output glitch during power-down or DEVRST_N assertion.

Microsemi has a development kit intended to demonstrate the capabilities of the RTG4 and expedite software development. The power distribution for this development board is shown in Figure 1. In this design, Microsemi uses a reset supervisor that holds the FPGA in reset for approximately 150 ms after the 3.3-V, 10-A regulator comes up. This allows sufficient time for all rails to reach regulation before the device begins operation bypassing the need for a power-up sequence. The oscilloscope plot in Figure 2 shows the main rails on startup while the device is held in reset. All of the voltage rails come up at the same time and reach their recommended operating points before the reset supervisor releases the active low reset.
Figure 1. RTG4 Development Board Power Distribution

Figure 2. RTG4 Development Board Start-up Sequence
3 Demonstrating Space Rated TI Solutions

3.1 Setup

To demonstrate the applicability of TI's space portfolio to this design, an RTG4 development kit was modified such that the voltage rails associated with power-up requirements were replaced with Evaluation Modules (EVM) of four space qualified power devices (TPS50601SPEVM-S, TPS50601SPEVM-D and TPS7H1101SPEVM). To demonstrate successful functionality under heavy load, the RTG4 was flashed with a high current design that resulted in a core current consumption of approximately 5 A at 1.2 V. The test setup can be seen in Figure 3.

![Figure 3. RTG4 Modified Development Board Connected to TI Evaluation Modules](image)

The reset supervisor on the development board was then removed and the voltage rails were sequenced using the power good and enable pins of each device as shown in Figure 5. The 12-V input source to the development board was changed to a 6-V source to satisfy the input requirements of the TI space power devices. The power tree for the modified development board is shown in Figure 4. The new components are shown in orange.
Figure 4. RTG4 Modified Development Board Power Distribution Using TI Space Qualified Components
Figure 5. RTG4 Modified Development Board Power Sequence

The rise times of all devices were configured to be at least 1 ms to avoid inrush currents. The core rail, VDD, is ratiometrically sequenced with the SERDES IO rail to ensure both voltage rails rise at the same time as required by the RTG4.

3.2 Results

The oscilloscope plots in Figure 6 and Figure 7 show the start-up behavior of each of these voltage rails while connected to the RTG4 development kit fulfilling the 2 requirements discussed in Section 2.
As shown in Figure 6 and Figure 7, both power sequencing requirements have been met and a clean monotonic power-up behavior is observed. Once the voltage rails come up, the RTG4 begins executing its software and the core starts to draw approximately 5-A of current. The software is the SERDES EPCS demo software (DG0624) provided by Microsemi.

### 3.3 Suggested Grounds-Up Implementation

The solution presented in Figure 3, Figure 4 and Figure 5 was based on modifications to the RTG4 development board. In a new RTG4 design, TI recommends a power distribution as the one shown in Figure 8. In this case, an isolated DC-DC converter using TI's portfolio of UC18xx-SP controllers is used to generate the 5-V input voltage to the switching and linear point of load regulators. The recommended power-up sequence for this power distribution is shown in Figure 9. Since the RTG4 supports DDR memories, a DDR termination regulator will be needed as part of the power distribution as shown in Figure 1. For such device, the TPS7H3301-SP has been included in this grounds-up recommended power distribution. The TPS7H3301-SP is TI's radiation hardened double data rate (DDR) 3-A termination regulator that supports all standard DDR memory configurations and incorporates a built-in reference voltage buffer, eliminating the need for an additional supply to produce the DDR reference. In addition, as it is a linear device, it provides significant area savings and simplicity when compared to switching devices that require inductor and more components for the device to operate. For more information, please refer to the TPS7H3301-SP product page. Notice the 1.5-V input voltage to the TPS7H3301-SP shown in Figure 8 is the high current supply providing the output current for the DDR termination voltage.
Figure 8. Recommended Grounds-Up RTG4 Power Distribution

Figure 9. Recommended Grounds-Up RTG4 Power-Up Sequencing. The SD_Vxx Signals Can Be Used for Power-Down Sequences as Needed.

This implementation ensures all power-up sequencing requirements are met as well as providing board area savings as TI offers the smallest, thermally enhanced radiation hardened DC-DC converter and LDO packages in the industry (TPS7H1101A-SP: 11.00 mm × 9.60 mm, TPS50601-SP: 12.70 mm × 7.38 mm).
Conclusion

The TPS50601-SP, TPS7H1101A-SP and TPS7H3301-SP are TI's flagship radiation tolerant power devices with features such as soft-start, power good, and tracking that make them particularly well suited for powering modern FPGA applications. This report has demonstrated how to implement these features with the RTG4 to achieve successful operation. Similar configurations can also be applied to other FPGAs to satisfy their specific power requirements.
5 References

   http://www.esa.int/Our_Activities/Space_Engineering_Technology/Microelectronics/The_use_of_reprogrammable_FPGAs_in_space

(2) Microsemi Documentation:
   a. UG0617: RTG4 FPGA Development Kit User Guide
   b. DS0131: RTG4 FPGA Datasheet
   c. AC439: Board Design Guidelines for RTG4 FPGA Application Note
   d. RTG4 Power Estimator

6 Additional Resources

• TPS50601-SP Datasheet (SLVSD45)
• TPS7H1101-SP Datasheet (SLVSD81)
• Advanced Topics in Powering FPGAs (SNVA592)
• Power Supply Design Considerations for Modern FPGAs (SNOA864)
IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT. AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include, without limitation, TI's standard terms for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated