

SOT23 Package Thermal Consideration

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ABSTRACT

Thermal design is very important for small outline transistor (SOT) packages. This paper compares the thermal performance of flip-chip on lead (FCOL) SOT23 packages with conventional wire-bond SOT23 packages. The results show that FCOL packages have better thermal-dissipation capabilities. Present SOT23 package PCB layout guides and summary of the FCOL SOT23 package thermal test results are based on the TI EVM.

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1 Introduction

More DC/DCs are using the SOT23 package, because the smaller size and lower cost. SOT23 package has 5-, 6-, and 8-pin versions, it can also be used for switches and LDO products. The SOT23 package does not have a thermal pad and the package size is much smaller than traditional TSSOP, so optimizing the thermal performance both in the IC design phase and the PCB layout design phase is required.

Wire bond and FCOL are two different technologies, which connect the die with the package. To get a better PCB design, it is important to know the difference about those two bonding structures. This paper shows the comparison using two bump methods, the results show FCOL bump technology can largely improve the power-dissipation capability of the SOT23 package. TI's monolithic product line has the TPS560200 device, which is a standard banding wire SOT23 package, the thermal resistance in the JEDEC standard is 167°C/W, while the TPS563200 device, which is the FCOL SOT23 package, the thermal resistance in the JEDEC standard is 87.9°C/W.

Finally, this paper introduces a general rule for SOT23 package layout and gives an example of TI suggested layout. Based on the TI EVM board, comparing the thermal performance of banding wire and FCOL SOT23 devices, the results show the FCOL SOT23 package can largely improve the thermal results and the customer can achieve a good thermal performance with optimized PCB layout.

2 Banding Wire SOT23 Package Introduction

Wire bonding is the method of making interconnections between an integrated circuit (IC) and its packaging during semiconductor device fabrication. Wire bonding is generally considered the most cost-effective and flexible interconnect technology and is used to assemble the vast majority of semiconductor packages.

From [Figure 1](#) and [Figure 2](#), the die fastens on the middle of the lead frame with glue and connects with the pin out using banding wire. The banding wire is copper or gold, the length is from several hundred μm to several mm and the diameter is typically 15 to 35 μm . The total $R_{\text{DS(on)}}$ is the $R_{\text{DS(on)}}$ of the die plus the banding wire $R_{\text{DS(on)}}$. For a high-current converter, the $R_{\text{DS(on)}}$ of the banding wire significantly increases the total $R_{\text{DS(on)}}$ of the device, meaning to keep the total $R_{\text{DS(on)}}$ smaller, you must increase the die size to decrease the die $R_{\text{DS(on)}}$. The banding wire will also increase the parasitic inductance between Vin, SW pin to Vin, and the SW pad on the die. It will decrease the SW ringing slew rate because of higher parasitic inductance, which is bad for efficiency.

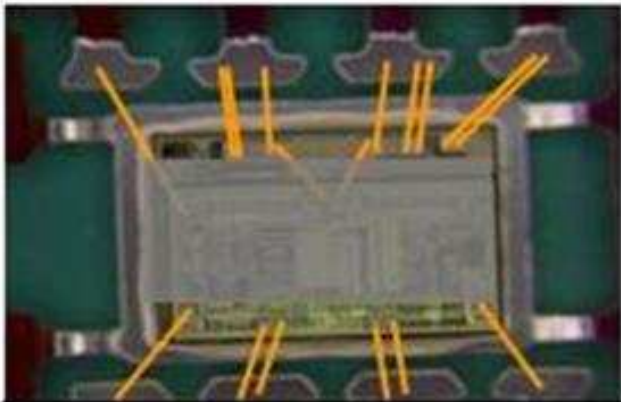


Figure 1. Bonding Wire Package Top View

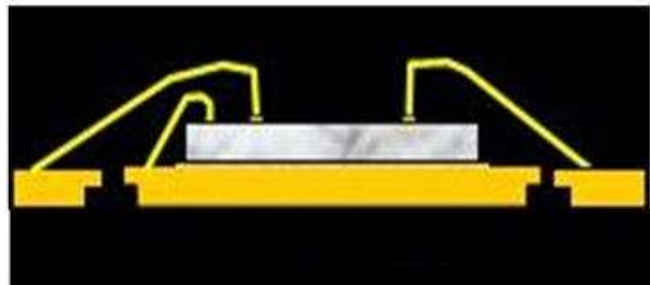
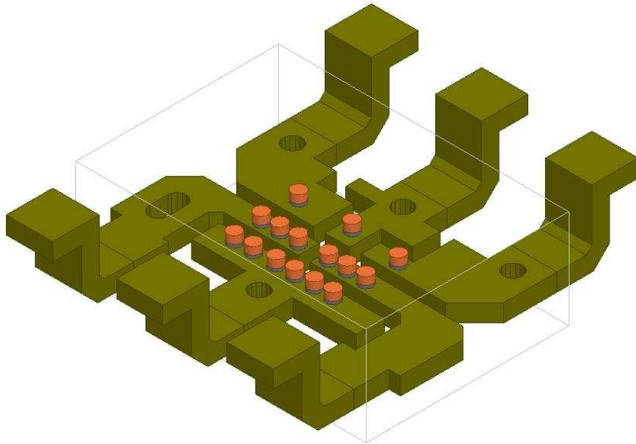
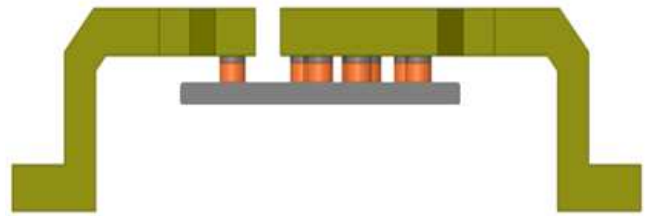


Figure 2. Bonding Wire Package Cross-Sectional View

The banding wire heats itself due to the larger $R_{\text{DS(on)}}$. Also the thermal needs of the die transfer to the external pin through the banding wire and then dissipation on the PCB board. A thermal pad at the bottom of the lead frame helps dissipate heat. The SOT23 package is very small and does not have thermal pad at bottom, so the thermal dissipation through the pin is very important for the total package temperature, it determines the total package thermal dissipation. Wire-bond is a long thin wire, is difficult to transfer heat from the die to the pin and makes the SOT23 package temperature higher.

3 FCOL SOT23 Package Introduction

From [Figure 3](#) and [Figure 4](#), the top of the die metal connects the lead frame with a copper post, the length is about 60–100 μm and the diameter is 50–125 μm . Wire bonding for the conventional packages typically requires more space due to the height and length of the wires. With FCOL, the copper bumps are located above the die and do not require additional space, thus enabling smaller overall package sizes. The TPS56x201 and TPS56x200 series implement FCOL package technology.


Figure 3. FCOL SOT23 Package Bottom View

Figure 4. FCOL SOT23 Package Cross-Sectional View

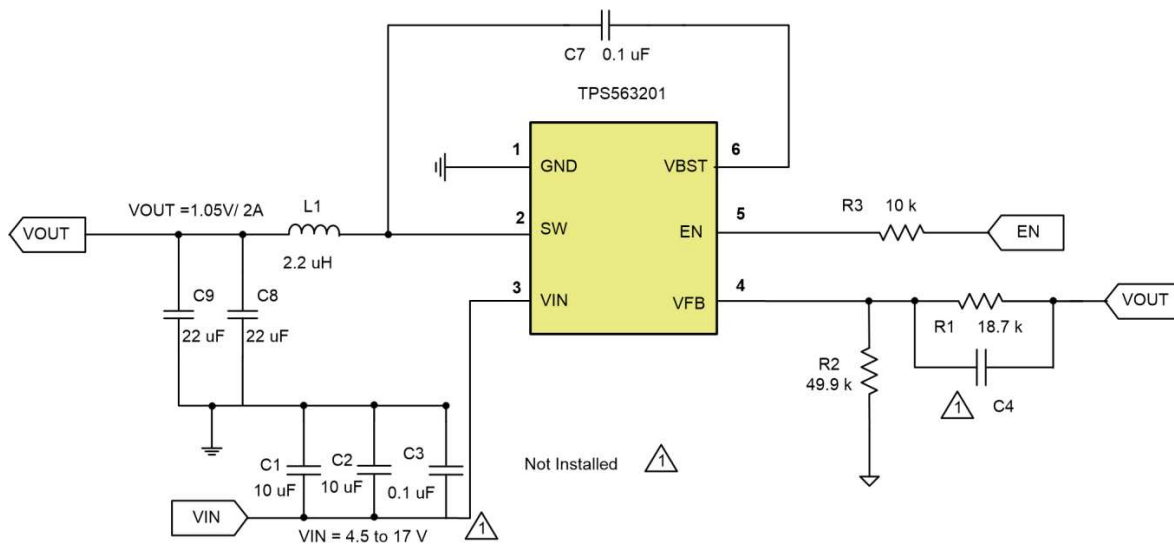
Flip Chip (FC) is not a specific package (like [SOIC](#)), or even a package type (like [BGA](#)). Flip chip describes the method of electrically connecting the die to the package carrier. The package carrier, either substrate or leadframe, then provides the connection from the die to the exterior of the package. Using flip-chip interconnect offers a number of possible advantages:

- Reduced signal inductance - Because the interconnect is **much** shorter in length (0.1 mm versus 1–5 mm), the inductance of the signal path is greatly reduced. This is a key factor in high-speed communication and switching devices
- Reduced power and ground inductance - By using flip-chip interconnect, power can be brought directly into the core of the die, rather than having to be routed to the edges. This greatly decreases the noise of the core power, improving performance of the silicon
- Higher signal density - The entire surface of the die can be used for interconnect, rather than just the edges. This is similar to the comparison between QFP and BGA packages. Because flip chip can connect over the surface of the die, it can support vastly larger numbers of interconnects on the same die size
- Die shrink - For pad limited die (die where size is determined by the edge space required for bond pads), the size of the die can be reduced, saving silicon cost
- Reduced package footprint - In some cases, the total package size can be reduced using flip chip. This can be achieved by either reducing the die to package edge requirements, since no extra space is required for wires, or in utilizing higher density
- Substrate technology, which allows for reduced package pitch

The copper post of the FCOL has a bigger diameter and shorter length, compared to wire bonding, so the $R_{DS(on)}$ of the copper post is smaller and the total $R_{DS(on)}$ of the device is smaller. The copper post also decreases the parasitic inductance from package to die, it can help the design achieve fast SW rising or falling slew rate, which is much better for efficiency. Higher efficiency will make the total power loss smaller and also the copper post is better for thermal dissipation than wire-bond.

4 SOT23 Package Layout Guideline

From the analysis, the FCOL SOT23 part has a better thermal performance than the banding wire version, it helps the SOT23 package achieve good performance. The thermal performance of the package depends on the die size and copper post, so when doing IC design, it is very important to design an optimized lead frame and try to add more copper post at the ground side for better thermal dissipation. It will largely help the die to dissipate the thermal to the PCB board. However, the SOT23 package is very small and does not have a thermal pad; therefore, the design must optimize PCB design to achieve good thermal dissipation.



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Figure 5. TPS563201 Application Schematics

A 4-layer PCB is helpful for thermal dissipation, TI's SOT23 solution can support a 2-layer application, TI's EVMs use a 2-layer PCB. The typical application circuit of the TPS563201 device is shown in [Figure 5](#) and a layout image is provided in [Figure 6](#) and [Figure 7](#).

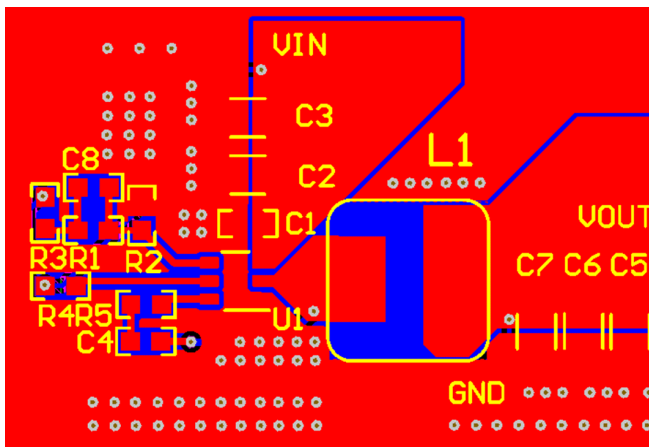


Figure 6. Top PCB Layout

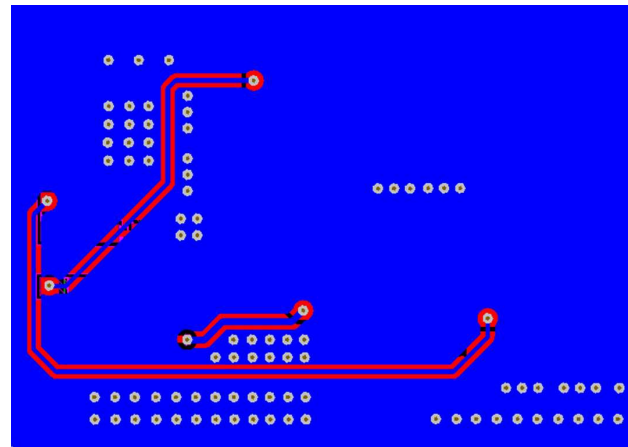


Figure 7. Bottom PCB Layout

The layout in [Figure 6](#) and [Figure 7](#) is just for reference. In some PCB designs, the top and bottom layer may not have so much space. In those cases, IC pins can be connected with vias to copper planes in the inner layers. It is important to realize that in FCOL packages, all IC pins are potential heat conductors and good a thermal connection to PCB copper planes can enhance the thermal cooling effect.

For real applications, space may not be available for better layout, and a trade off is needed: The following list, provides the layout priority:

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas provide better heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.

5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. The voltage feedback loop should be placed away from the high-voltage switching trace, and would preferably have a ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

For a 4-layer PCB, put your signal wire at layer 2 or layer 3, make sure the bottom layer GND does not separate by the line, this will increase thermal dissipation. Also, add more GND via to make all GND in each layer connect together. TI suggests pouring GND polygon for the top layer and the bottom layer.

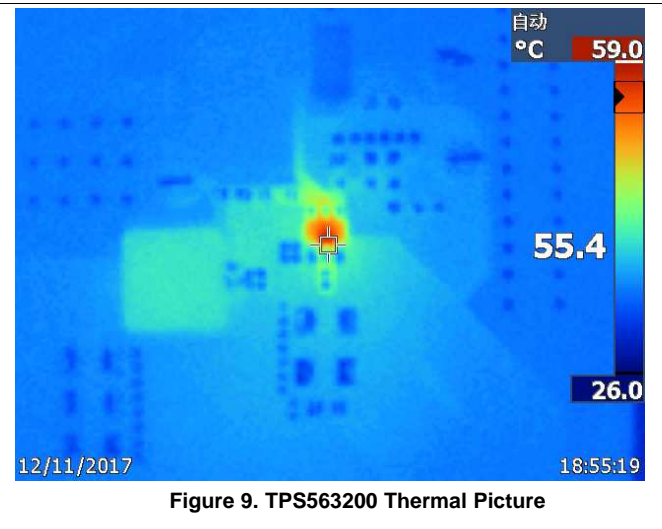
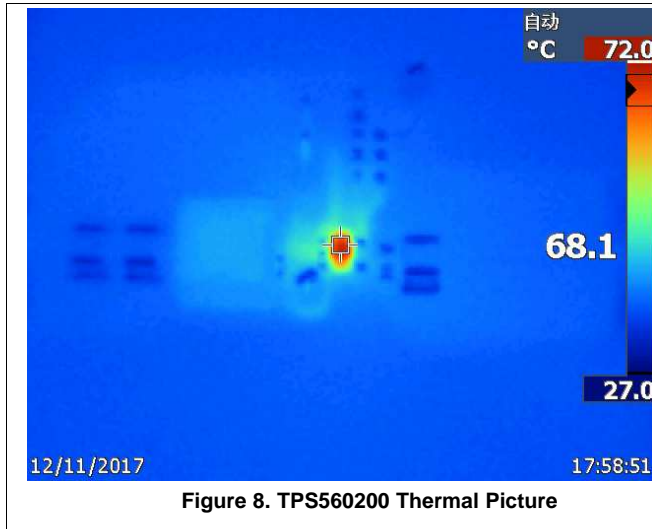
5 Thermal Test

Table 1 shows thermal simulation result based on the JEDEC standard, from the result, observe the TPS563201 device, FCOL, the θ_{JA} based on the JEDEC standard is 92.6 versus 166.8, the TPS560200 banding wire. Because the TPS560200 is 500 mA DC/DC, power loss on the die is much smaller than the TPS563201 device, so the final thermal performance can be acceptable by using banding wire.

Table 1. Thermal Simulation Results Comparison

Thermal Metric		TPS563201	TPS560200	Unit
		SOT	SOT	
θ_{JA}	Junction-to-ambient thermal resistance	92.6	166.8	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	48.5	100	
θ_{JB}	Junction-to-board thermal resistance	15.5	75.5	
θ_{JT}	Junction-to-top characterization parameter	2.5	29.2	
θ_{JB}	Junction-to-board characterization parameter	15.5	3.7	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance			

Figure 8 and **Figure 9** show two thermal scans, **Figure 8** is a standard wire-bond SOT23-6 package, while **Figure 9** shows an FCOL SOT23-6. Both ICs were mounted on a TI evaluation board with the same device power dissipation of around 0.6 W. The layout was optimized for good thermal performance based on guidelines mentioned in [Section 4](#). The wire bond SOT23-6 clearly shows a large hotspot, and the scan also shows that the pins on the left side of the package are hotter than the pins on the right side. This is because the GND pin is located on the left side. The FCOL package hotspot is from 15° to 20° cooler than the wire bond, and shows heat conduction from all pins.



Based on the results in [Figure 8](#) and [Figure 9](#), the thermal resistance from junction to ambient of an FCOL SOT23-6 package in a highly optimized 2-layer PCB layout can go as low as 53°C/W. In layouts where there is less space available, the cooling properties may be a bit less, but values of 60°C/W to 70°C/W are definitely achievable. This makes it possible to dissipate around 0.85 W under 60°C ambient conditions. If using a 4-layer board, the thermal resistance should be even lower than the 2-layer board, better thermal performance can be achieved if using a 4-layer PCB.

After testing a 2 A–5 A DC/DC with the same EVM layout, the following thermal resistance based on EVM layout was achieved ([Table 2](#)). With the die size and copper post area increasing, the thermal resistance is decreasing. Also increase the efficiency of full loading to get the same thermal performance for high-current DC/DC. From the test result the TPS563201, TPS564201, and TPS565201 have the same thermal performance at full loading conditions.

Table 2. SOT23 Product Thermal Test Result

	TPS563201	TPS564201	TPS565201
EVM board	2-layer board 60-mm x 60-mm	2-layer board 60-mm x 60-mm	2-layer board 60-mm x 60-mm
Efficiency (1.05 V, full loading)	72%	77.5%	77.8%
Case temperature(°C)	85	73	82
EVM θ_{JA} (°C/W)	59.5	56	53

6 Summary

FCOL packages have some electrical and thermal advantages. In FCOL packages, each pin has a good thermal connection to the silicon die. The PCB layout can be optimized to let each pin conduct more heat from die to PCB, which can lower the overall thermal resistance from Junction to Ambient. This allows more power to be dissipated in the FCOL package when compared to same package with wire bond connections.

Even FCOL of SOT23 can help for thermal dissipation, but the designer still needs to consider good PCB design to get better thermal performance. TI's EVMs provides a good example for the customer to do layout for an SOT23 package. Also, TI's *WEBENCH*[®] online tool can help do simulations for efficiency and for thermal results of your design. A full solution with the SOT23 package, covers from 0.5- to 5-A applications, is pin-to-pin compatible and easy to design.

Table 3. TI SOT23 Package Product Table

Device Name	Input Voltage (V)	Load Current (A)	Control Mode	Eco-Mode at Light Load	Comments
TPS560200	4.5–17	0.5	DCAP2	Yes	
TPS561201	4.5–17	1	DCAP2	Yes	
TPS561208	4.5–17	1	DCAP2	No	
TPS562200, TPS562201	4.5–17	2	DCAP2	Yes	
TPS562209, TPS562208	4.5–17	2	DCAP2	No	
TPS563200, TPS563201	4.5–17	3	DCAP2	Yes	
TPS563209, TPS563208	4.5–17	3	DCAP2	No	
TPS562210, TPS563210	4.5–17	2	DCAP2	Yes	SOT238, with SS, PG
TPS562219, TPS563219	4.5–17	3	DCAP2	No	SOT238, with SS, PG
TPS564201	4.5–17	4	DCAP2	Yes	
TPS564208	4.5–17	4	DCAP2	No	
TPS565201	4.5–17	5	DCAP2	Yes	
TPS565208	4.5–17	5	DCAP2	No	
TPS54302	4.5–28	3	Peak Current	Yes	
TPS54202	4.5–28	2	Peak Current	Yes	

7 References

1. Texas Instruments, [Semiconductor and IC Package Thermal Metrics](#)
2. Texas Instruments, [Optimized Layout for the TPS565201 EVM](#)
3. Texas Instruments, [TPS565201 4.5-V to 17-V Input, 5-A Synchronous Step-Down Voltage Regulator in SOT-23](#)
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