**Understanding the Start-up Behavior of the TPS61178x**

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**ABSTRACT**

This application report details the start-up behavior of the TPS61178x device. It also characterizes the start-up timing and proposes a method to reduce the start-up inrush current. The proposed method is confirmed by bench test measurements.

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1 Introduction

For the conventional synchronous boost converter, the output voltage follows the input voltage when the converter is disabled. This behavior increases power loss due to the leakage current flowing through the feedback divider and the post-load. The TPS61178x device is a 20-V, 10-A boost converter that integrates a circuitry to drive an external P-FET to isolate the output side from the input side. Figure 1 shows a typical schematic of the TPS61178x. Because the output voltage drops to zero after the TPS61178x shuts down, the leakage current in the output also decreases to zero. The start-up circuitry of TPS61178x is designed to prevent the power supply from overloading when output voltage increases from zero to the setting value.

![Figure 1. Typical Schematic of TPS61178x](image-url)

2 Start-up Behavior Description

The start-up procedure of the TPS61178x device is divided into precharge phase and soft-start phase. The precharge phase is the period when the output voltage (VOUT2) increases from zero to 10% higher than $V_{IN} \times (1.1 \times V_{IN})$; the soft-start phase is the period from $1.1 \times V_{IN}$ to the setting output voltage.

Figure 2 shows the start-up waveform measured in TPS61178x evaluation module (EVM) at 7.2-V input voltage. In the waveform, CH1 is VOUT2 (after P-FET) shown in Figure 1; CH2 is the TPS61178x VOUT pin (before P-FET); CH3 is the EN pin voltage; and CH4 is the input current of the boost converter. The behavior of the waveform is explained as follows:

- Before $t_0$, the EN pin is logic low, and the TPS61178x shuts down. The voltage at the VOUT pin is $(V_{IN} - V_D)$, where $V_D$ is the body diode voltage. The DISDRV pin is in high impedance to turn off the external P-FET.

- At $t_0$, the EN pin becomes logic high. After a short delay, the TPS61178x starts switching and boosts the voltage at the VOUT pin to $1.1 \times V_{IN}$. At the same time, the DISDRV pin discharges to ground with a typical 55-µA current source, as shown in Figure 3. The gate-to-source voltage $V_{GS}$ of the P-FET decreases. The slew rate is determined by Equation 1, where $I_{GATE}$ is typical 55 µA; $\tau$ is $R_{GATE} \times C_{GATE}$.

$$V_{GS} = -I_{GATE} \times R_{GATE} \left(1 - e^{-\frac{1}{\tau}}\right)$$  

(1)

- At $t_1$, the $V_{GS}$ becomes lower than the threshold voltage of the P-FET. The P-FET turns on, and charges the output capacitor to $1.1 \times V_{IN}$. 
• At \( t_2 \), the precharge phase finishes and the device enters soft-start phase. The period from \( t_2 \) to \( t_3 \) is called precharge phase, which is approximately 2.6 ms. After \( t_2 \), the rising rate of the FB pin voltage is internally controlled by Equation 2, where \( V_{\text{REF}} \) is typical 1.198 V and \( t_{\text{startup}} \) is typical 3.2 ms

\[
V_{\text{FBSS}} = \frac{V_{\text{REF}}}{t_{\text{startup}}}
\]  

(2)

• At \( t_3 \), the FB voltage reaches 1.198 V, and the soft-start phase finishes. The period from \( t_2 \) to \( t_3 \) can be calculated by Equation 3, where \( V_{\text{OSET}} \) is the setting output voltage.

\[
t_{\text{boost SS}} = t_{\text{startup}} \times \left(1 - \frac{1.1 \times V_{\text{IN}} \times R_{\text{DOWN}}}{\left(R_{\text{UP}} + R_{\text{DOWN}}\right) \times V_{\text{REF}}}\right) = t_{\text{startup}} \times \frac{V_{\text{OSET}} - 1.1 \times V_{\text{IN}}}{V_{\text{OSET}}}
\]  

(3)

Figure 2. Start-up Waveform of the TPS61178 EVM at \( V_{\text{IN}} = 7.2 \) V

Figure 3. P-FET Driving Circuitry

The \( R_{\text{GATE}} \) in Figure 3 is used to clamp the \( V_{\text{GS}} \) not higher than \(-I_{\text{GATE}} \times R_{\text{GATE}}\). Make sure the \(|V_{\text{GS}}|\) is high enough to drive the P-FET while lower than the maximum voltage rating. In the TPS61178x EVM, the \( R_{\text{GATE}} \) is 100 k\( \Omega \) to get \(-5.5 \) V for the CSD25404Q3.

In the precharge phase, an inrush current charges the output capacitor when the P-FET turns on. Increasing the \( C_{\text{GATE}} \) can reduce the charging current because the \( V_{\text{GS}} \) slope rate becomes slower. However, the P-FET must effectively turn on before the precharge phase finishes, otherwise the output voltage will be out of control as the FB pin voltage comes from VOUT2. Taking CSD25404Q3 as example, this MOSFET effectively turns on at \( V_{\text{GS}} = -1.5 \) V from its “Transfer Characteristics”. Therefore, the \( V_{\text{GS}} \) should be lower than \(-1.5 \) V before the precharge phase finishes. Because the minimum precharge time is 1.8 ms, the maximum \( C_{\text{GATE}} \) can be calculated by Equation 4.
Start-up Behavior Description

\[ C_{\text{GATE\_MAX}} = \frac{t_{\text{PRE\_CHARGE}}}{-\ln\left(1 + \frac{V_{\text{GS}}}{I_{\text{GATE}} \times R_{\text{GATE}}}\right) \times R_{\text{GATE}}} = \frac{1.8 \text{ m}}{-\ln\left(1 - \frac{1.5}{55 \mu \times 100 \text{ k}}\right) \times 100 \text{ k}} = 56 \text{ nF} \]  

As showed in Figure 4, the inrush current during the precharge phase reduces to 2 A if the \( C_{\text{GATE}} \) increases from 22 nF to 47 nF, and the P-FET fully turns on within 1.8 ms.

Figure 4. Start-up Waveform at \( C_{\text{GATE}} = 47 \text{ nF} \)

To increase \( C_{\text{GATE}} \) further, add a resistor in series with \( C_{\text{GATE}} \), as shown in Figure 5. When the TPS61178x is enabled and the voltage of \( C_{\text{GATE}} \) is zero, the \( V_{\text{GS}} \) is defined by Equation 5. As the minimum threshold voltage of the CSD25404Q3 is 0.65 V, the \( R_{\text{G\_A}} \) is set to approximately 13.4 kΩ to void the P-FET turning on at the beginning.

Figure 5. Method to Reduce the Start-up Current

\[ V_{\text{GS}} = -I_{\text{GATE}} \frac{R_{\text{GATE}} \times R_{\text{G\_A}}}{R_{\text{GATE}} + R_{\text{G\_A}}} \]  

(5)
After adding \( R_{G_A} \), the \( V_{GS} \) is defined by Equation 6 after the TPS61178x is enabled, where \( \tau \) is \((R_{G_A} + R_{GATE}) \times C_{GATE}\). The maximum value of \( C_{GATE} \) can be calculated by Equation 7.

\[
V_{GS} = -I_{GATE} \times R_{GATE} \left( 1 - e^{-\frac{1}{\tau}} \right) - I_{GATE} \times R_{GATE} \times e^{-\frac{1}{\tau}} \times \frac{R_{G_A}}{R_{GATE} + R_{G_A}}
\]

(6)

\[
C_{GATE\_MAX} = \frac{t_{PRE\_CHARGE}}{-\ln \left( \frac{V_{GS} + I_{GATE} \times R_{GATE}}{I_{GATE} \times R_{GATE}} \times \frac{R_{GATE} + R_{G_A}}{R_{GATE}} \right) \times \left( R_{GATE} + R_{G_A} \right)}
\]

= \frac{1.8 \text{ ms}}{-\ln \left( \frac{-1.5 + 55 \mu \times 100 \text{ k}}{55 \mu \times 100 \text{ k}} \times \frac{100 \text{ k} + 13.4 \text{ k}}{100 \text{ k}} \right) \times (100 \text{ k} \times 13.4 \text{ k})} = 82 \text{ nF}
\]

(7)

Selecting the \( R_{G_A} \) to be 13.4k and \( C_{GATE} \) to be 68 nF, the start-up waveform is shown in Figure 6. The input inrush current reduces to 1.5 A, and the P-FET fully turns on within 1.8 ms after the EN pin becomes logic high.

![Figure 6. Start-up Waveform With Proposed Method](image)

3 Summary

This application report described the soft-start timing and behavior of the TPS61178x device. Theoretic analysis and bench tests show that the input inrush current during start-up is determined by the driver circuitry of the external P-FET. Suitable selection of the circuitry components can help reduce the inrush current.
### Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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<td>• Changed &quot;1n&quot; to &quot;ln&quot; in <strong>Equation 4</strong>..................</td>
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<td>• Changed &quot;1n&quot; to &quot;ln&quot; in <strong>Equation 7</strong>..................</td>
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