

# Reduce Motor Drive BOM and PCB Area with TI Smart Gate Drive

James Lockridge, Analog Motor Drive



## Introduction

In an ideal world, gate drivers would connect directly to MOSFET gates and the motor drive system would operate perfectly. However, the real world creates a variety of issues for motor drive designers that cause them to add extra external components between a gate driver's outputs and the external power-stage FETs. The example in Figure 1 shows that each external power MOSFET may need up to four additional components for a designer to mitigate possible FET gate drive issues. For a three-phase driver, a designer might use up to twenty-four external components between the gate driver IC and triple half-bridge FETs.

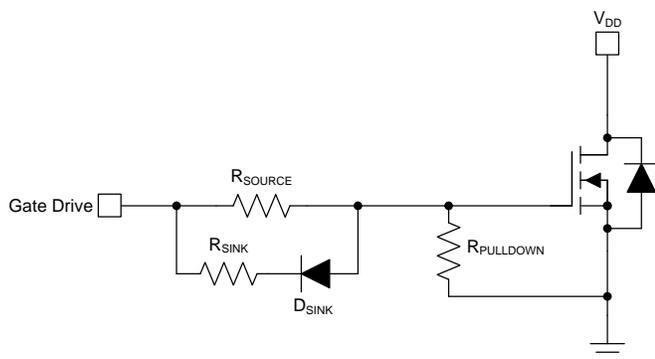


Figure 1. Additional components between gate driver and MOSFET

The main reasons designers add these components are to improve radiated electromagnetic interference (EMI) performance, protect the gate driver and FETs, and eliminate unintentional FET turn-on from switching transients. Adding these components to the gate driver increases board area and bill of materials (BOM) cost in motor drive designs. TI's Smart Gate Drive features eliminate the need for these external components while helping designers meet their EMI, robustness, and performance goals.

## How Smart Gate Drive eliminates components

The  $R_{SOURCE}$  and  $R_{SINK}$  resistors limit the gate current of the FET as it switches. By reducing the gate current, the FET gate capacitance takes longer to charge and discharge. This slows the slew rate of the FET as it switches. While  $R_{SOURCE}$  is sufficient to limit the turn-off

slew rate for some designs, sometimes designers require a larger sinking current to turn off the FET faster and keep it turned off during transients on the switching node. The diode  $D_{SINK}$  puts the two resistors in parallel during turn-off for a larger sinking current.

Although FETs dissipate less power when they switch quickly, fast edges cause ringing in the parasitic inductances (traces, bond wires, leads) and capacitances ( $C_{GD}$ ,  $C_{GS}$ ,  $C_{DS}$ ) in and around the FET (Figure 2). This ringing from the parasitic components contributes to EMI and causes voltage overshoot and undershoot transients on the switching node. These transients can damage the FET and gate driver by violating minimum and maximum voltage ratings.

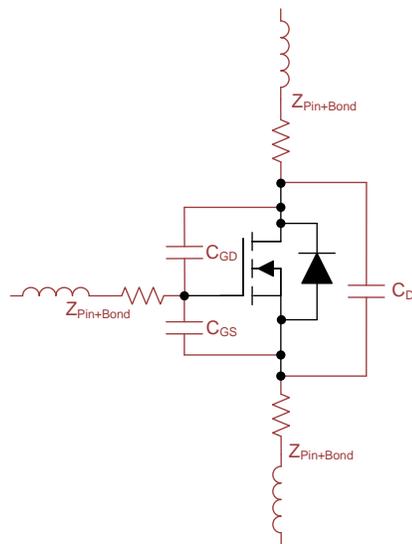


Figure 2. Some of the parasitic inductances and capacitances around a FET.

The Smart Gate Drive feature in TI motor drivers allows designers to select the gate drive source and sink currents without adding components to the gate-drive output. Figure 3 shows an example of how to select gate-drive currents using a single pin. Other devices use a serial interface to select the gate-drive currents. By configuring the gate-drive currents, designers can eliminate  $R_{SOURCE}$ ,  $R_{SINK}$ , and  $D_{SINK}$ . This can save the BOM cost and PCB area of up to *eighteen components* between the gate driver and the power-stage MOSFETs.

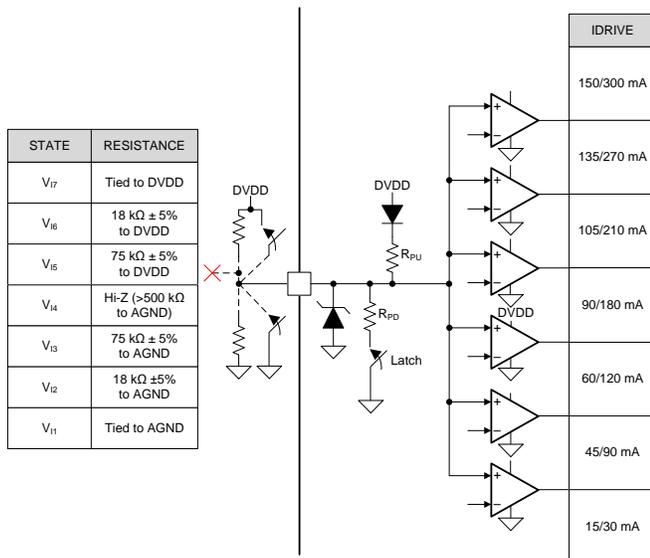


Figure 3. DRV8304H IDRIVE settings. See [DRV8304 Product Folder](#) for more information.

Additionally, Smart Gate Drive eliminates the R<sub>PULLDOWN</sub> resistor by integrating it into the gate driver. This resistor helps to hold the FET gates low so they do not turn on from system noise coupling when the H-bridge FETs are disabled. By integrating the resistor, Smart Gate Drive can eliminate *six more components*.

### Printed circuit board layout example

Figure 4 (a) shows a layout with components between the driver and the FETs. Figure 4 (b) shows how eliminating those components with Smart Gate Drive saves board space. Even though the components are small, their reference designators, traces, and geometry of the design require additional board area. The resistors and diodes in the Figure 4 example are 0402 packages (40 mil x 20 mil), but only use about 7% of the total area between the gate driver and the FETs. In this particular board example, Smart Gate Drive saves a total board area of about 180 mm<sup>2</sup> (0.28 in<sup>2</sup>).

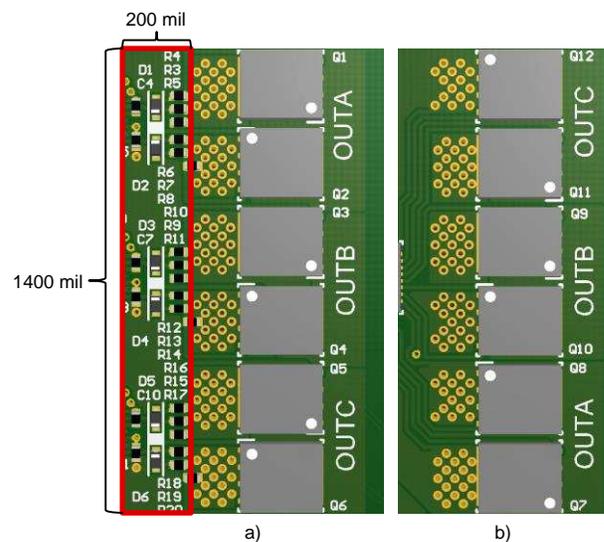


Figure 4. Example gate drive layouts for a three-phase driver.

### Conclusion

With Smart Gate Drive, TI motor drivers bring the ideal world closer to reality. Smart Gate Drive addresses FET driving concerns while reducing a motor drive system's bill of materials (BOM) and PCB area by around *twenty-four components*. For more details, see the [Understanding IDRIVE and TDRIVE in TI Smart Gate Drivers application report](#).

Table 1. Device Recommendations

Device	Description
DRV832x	60-V Three-Phase Smart Gate Driver with Three Current Shunt Amplifiers and Buck Regulator
DRV835x	100-V Three-Phase Smart Gate Driver with Three Current Shunt Amplifiers and Buck Regulator
DRV8305	45-V Three Phase Gate Driver with Three Current Shunt Amplifiers and LDO Regulator
DRV8304	38-V Three-Phase Smart Gate Driver with Three Current Shunt Amplifiers

### Related Documentation

- [Understanding IDRIVE and TDRIVE in TI Smart Gate Drivers](#)
- [Field Oriented Control \(FOC\) Made Easy for Brushless DC \(BLDC\) Motors Using TI Smart Gate Drivers](#)

## IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2018, Texas Instruments Incorporated