Examples of Applications with the Pulse Width Modulator TL5001

Author: Ingrid Kohl

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1. Introduction

Switched-mode techniques are used more and more nowadays for the design of power supplies. Switch mode power supplies have considerably higher efficiency when compared to designs employing linear regulators, and can be used for higher output powers. The rectified input voltage in a switching regulator is chopped by means of a switch. The LC network after the switch smoothes this voltage, resulting in a DC voltage at the output. This voltage is controlled by a regulator, such that the end result is a regulated output voltage (see figure 1.1)

**Figure 1.1: Block diagram of a Switched Mode Power Supply**

As a result of the high switching frequencies which are involved, very small components can be used. This allows the construction of compact and low-cost power supplies. However, the high frequency switching signals also potentially create interference, and this can only be avoided with careful attention to the design and layout of the circuit.

The configurations of the components which are external to the regulator allow the design of various types of switching regulators. In the following section a step-down converter will be described, in which the output voltage is lower than the input.
2. Step-Down Converters

The circuit diagram of a step-down converter is shown in figure 2.1.

![Schematic diagram of a Step-Down Converter](image)

The actual voltage converter is made up of a switch (in this case, the transistor Q), the inductor L, the diode D, and the capacitor C. If the switch is closed (transistor Q conducting), current flows via the inductor L to the load. When the switch is open (transistor Q not conducting), the polarity of the voltage across the inductor is reversed, and the current flows via the free-wheeling diode D to the load. The switching transistor is controlled by the output of the regulator.

During the switch-on time $t_{on}$ (transistor Q conducting), the voltage across the inductor can be calculated as follows:

$$V_{in} - V_{DS} - V_{out} = -L \frac{\Delta I}{t_{on}}; \quad \left( V_{in} - V_{DS} - V_{out} \right) t_{on} = -L \cdot \Delta I$$

(1)

$V_D$ is the forward voltage of the diode.

$V_{DS}$ is the Drain-Source voltage of the switching transistor, but this will be neglected below.

If the switch is open (transistor Q non-conducting), the voltage across the inductor will be:

$$V_{out} + V_D = -L \frac{\Delta I}{t_{off}}; \quad \left( V_{out} + V_D \right) t_{off} = -L \cdot \Delta I$$

(2)

The result of equations (1) and (2) is:

$$\frac{V_{out} + V_D}{V_{in} - V_{out}} = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T} = D$$

(3)

This shows that the output voltage $V_{out}$ can be adjusted by means of the pulse duty ratio $D$. 
2.1 The inductor as an energy store

In this circuit the inductor functions as a store of energy. During the time period $t_{on}$, the current in the inductor rises linearly, up to a value of $I_{L_{\text{max}}}$. During the time period $t_{off}$, the current through the inductor falls again, but retains its direction of flow. A distinction must be made between the two different operating modes: continuous and discontinuous operation (see figure 2.2a and b).

![Figure 2.2: Inductor current, with continuous and discontinuous operation](image)

With continuous operation, the current in the inductor does not fall to zero. The change of current in the inductor can be expressed as follows:

$$\Delta I = \frac{1}{L} \left( V_{\text{in}} - V_{\text{out}} \right) t_{on} = \frac{1}{L} \left( V_{\text{out}} + V_D \right) t_{off}$$

The changeover from continuous to discontinuous operation occurs when the curve of the current $I_{\text{out}_{\text{min}}}$ in figure 2.2a just touches the zero line. Solving expression (3) for $t_{on}$ and inserting into (4) gives the minimum output current for continuous operation as follows:

$$I_{\text{out}_{\text{min}}} = \frac{\Delta I}{2} = \frac{T}{2L} \cdot \left( V_{\text{in}} - V_{\text{out}} \right) \cdot \frac{V_{\text{out}} + V_D}{V_{\text{in}} + V_D}$$

If the output current sinks further, the flow of current in the inductor will be interrupted. In order to avoid this, the pulse duty ratio must be changed; otherwise the output voltage will rise. Since the pulse duty ratio is limited to a finite switch-on time of the switching transistor, the inductance of the inductor should be chosen to insure that the current in the inductor is not interrupted at the minimum rated current.
The important factors to be considered when designing the inductor are the minimum and maximum load current, the switching frequency, and the voltage drop across the inductor.

\[ L = \frac{D}{f \cdot \Delta t} (V_{in} - V_{out}) \]  

(6)

2.2 The free-wheeling diode

The diode in a switching regulator is used as a free-wheeling diode, maintaining the inductor current, when the switching transistor is turned off. The changeover from the conducting to the blocking state is of great significance with switching regulators, due to the increasing switching losses with increasing frequency. When the transistor is switched on, the diode continues conducting until the reverse recovery time has passed. During this time period, the power dissipation is very high. For this reason fast recovery diodes are needed, which should in particular have a very rapid turn off time.

For applications of this kind, Schottky or epitaxial diodes are appropriate.

Schottky diodes are particularly suitable, because of their low forward voltages and the fast switching times which result from their use of metallic boundaries within the semiconductor. Since they have a low breakdown voltage, Schottky diodes can only be used for low output voltages.

Epitaxial diodes have very fast reverse recovery time, and as a result of their high breakdown voltage can also be used for higher output voltages. Their forward voltage is, however, higher than that of Schottky diodes.

2.2.1 Switching behavior of a diode

![Figure 2.3: Switching behavior of a diode](image)

*Figure 2.3: Switching behavior of a diode*
When changing over from the conducting into the blocking state, the current in the diode falls with a slope of $-\frac{dI_F}{dt}$. This slope depends on the turn-on speed of the switching transistor. As soon as the current has reached the maximum reverse current $I_{RM}$, it rises again at $\frac{dI_R}{dt}$. The current collapses during this period. If the edge is very steep, the collapse of the current takes place very fast, and together with the inductance in the circuit results in high-frequency oscillations. To prevent this from happening, fast soft-recovery diodes can be used which - as a result of their soft switch-off characteristics - avoid the generation of high-frequency interference. Another way of damping these oscillations is to connect a RC network in parallel with the diode.

### 2.3 The switching transistor

The transistor operates as a switch: either blocking or fully conducting. In this mode of operation, the power dissipation in the transistor is very low, and occurs almost exclusively during the changeover from the conducting into the blocking state. To allow the use of high switching frequencies, in switching regulators a transistor is needed which can be switched on and off very fast.

With bipolar transistors, both types of charge carriers are needed to carry current. During the changeover from the conducting to the blocking state, the charge carriers in the base region must first be removed, resulting in relatively long switch-off times.

In contrast, MOS field-effect transistors use only one type of charge carrier in the conduction of current. Resulting in significantly shorter switching times. The switching time of a MOSFET depends primarily on the Gate-Drain (Miller) capacitance, and which must be charged and discharged during each switching cycle. In order to ensure that this happens very quickly (in a few ns), the gate of the transistor must be controlled by a driver circuit, which provides the current needed to charge and discharge the capacitance, reducing the switching time.

### 2.4 Output capacitance

The function of the output filter capacitor is to smooth the output voltage, and to stabilize it against sudden changes in the load.

A large capacitance results in a reduction of the ripple at the output.

The value of this capacitance can be calculated from the following expression:

$$C_{\text{Filter}} = \frac{Q}{V_{\text{Ripple}}}$$  \hspace{1cm} (7)

The value $V_{\text{Ripple}}$ is the maximum change of the output voltage, and $Q$ is the charge transferred from the capacitor $C_{\text{Filter}}$ to the load during one cycle.

The capacitor will be charged provided that the current in the inductor is larger than the load current $I_{\text{out}}$. The area shaded in figure 2.4 corresponds to the change of the charge $Q$ in the capacitor $C_{\text{Filter}}$. 
The series resistance $R_{ESR}$ and the series inductance $R_{ESL}$ of the filter capacitor should be as small as possible, in order not to increase the ripple on the output voltage. For this reason, a capacitor should be used which has a very low loss resistance, and which also has the necessary high capacitance.

As a result of their wound aluminum foil construction, aluminum electrolytic capacitors have a very high series inductance. To reduce this, several capacitors are connected in parallel at the output. As a result of these precautions, the loss resistance $R_{ESR}$ will also be reduced, resulting in a low level of output ripple. The use of tantalum electrolytic capacitors has the additional advantage that they have both a very low series inductance and also a particularly low series resistance.

3. The Driver Circuit for the Switching Transistor

The open-collector output stage of integrated driver circuits for switching regulators used with a pull-up resistor (see figure 3.1a) is not able to deliver the currents needed to charge and discharge the Miller capacitance of the switching transistor. An external driver circuit (see figure 3.1b) should be used. This provides the current needed to charge and discharge the input capacitance of the switching transistor, reducing switching time and increasing efficiency.
The principle of operation of this circuit can be described as follows.

When the output transistor $Q_{out}$ is in a conducting state, the transistor $Q_1$ will be driven into conduction, and the Gate-Source voltage of the MOSFET raised correspondingly. The voltage at node 3 will be $V_c = V_{CC} - V_{D1}$, and $V_{BE(Q1)}$ at node 2. In this state, the transistor $Q_2$ will be non-conducting.

If the output transistor $Q_{out}$ becomes non-conducting, then the transistor $Q_1$ will also be at a high resistance. The voltage at node 2 increases. Since the voltage across the capacitor can not be changed instantaneously, the voltage at the nodes 2 and 4 will also rise. The transistor $Q_2$ will conduct. As a result of this kind of feedback (Bootstrap), the transistor $Q_2$ will be driven very quickly into full conduction.

The difference in the slope of the edges of the rate of rise of the gate voltage $V_{GATE}$ is shown in figure 3.1, with and without a driver circuit.
4. Drain-Source Voltage Limiting

With MOS transistors the maximum Gate-Source voltage is usually 20 V. With circuits such as that shown in figure 3.1, the Gate-Source voltage of the switching transistor in the conducting state is about the same as the input voltage $V_{CC}$. When using an input voltage $V_{CC} > 20$ V an additional circuit must therefore be used to limit the Gate-Source voltage to the maximum permissible value.

The circuit shown in figure 4.1 limits the Gate-Source voltage of the MOSFET to a value which is below the maximum permissible voltage.
The Zener diode $Z_1$ determines the maximum Gate-Source voltage at the MOSFET. The Zener voltage $V_Z$ of the diode $Z_1$ is chosen to be high enough to ensure that the MOSFET is driven sufficiently hard to attain the desired on-resistance $R_{DSon}$. The transistor $J_1$ operates as a current source. If the transistor $Q_{out}$ is switched on, and the transistor $J_1$ thus conducting, then the voltage $V_{CC} - V_{Z1} - V_{D4} + V_{BE(Q2)}$ will appear at node 1. If the transistor is non-conducting, then the voltage at node 1 will again rise to that of the supply voltage $V_{CC}$.

Figure 4.1: Limiting the Gate-Source voltage
5. Pulse Width Modulation

As mentioned above, in a switching regulator the transistor operates as a switch. Pulse width modulation is the method used to control this switching transistor, the on and off time of which is controlled as a function of the output voltage (see figure 5.1).

![Schematic diagram of a pulse width modulator](image)

**Figure 5.1:** Schematic diagram of a pulse width modulator

The output voltage $V_{out}$ which is to be regulated is divided by a resistive divider network $R_1/R_2$, and compared with the internal reference voltage in the error amplifier. The difference between the required and the actual value is amplified, and compared in the pulse width modulator with the oscillator signal (see figure 5.1). The output signal of the pulse width modulator is a square-wave pulse, of constant frequency and variable pulse duty ratio. If the amplitude of the output signal of the error amplifier is greater than that of the oscillator signal, then there will be a High signal at the output of the pulse width modulator; if it is less, there will be a Low signal (see figure 5.2).

![Principle of Pulse Width Modulation](image)

**Figure 5.2:** Principle of Pulse Width Modulation

6. Circuit Description of the TL5001

The TL5001 includes all of the function necessary in the design of a reliable switching regulator.
The actual value of the output voltage of the switching regulator is fed back to the input FB (Feedback) of the device, and compared with the internally generated reference voltage $V_{\text{ref1}}$ in the error amplifier. If the voltage at the input FB (Feedback) is below the reference voltage, then the error amplifier output voltage will be pulled in the direction of the supply voltage of the amplifier; in the opposite case, it will be pulled towards the negative supply voltage (GND). This output signal is now compared in the PWM/DTC comparator with the sawtooth signal of the oscillator OSC and the voltage at the DTC input. If the oscillator signal level is lower than the two other voltages, then the output signal of this comparator will become High; in the opposite case, it will become Low. With a High signal, the output transistor $Q_{\text{OUT}}$ will become conducting, and the output OUT will be pulled to ground potential. By means of a constant voltage at the DTC input, which must lie between the minimum and maximum value of the oscillator output voltage, the pulse duty ratio can be limited to a specific value.

If an overload (e.g. a short circuit) occurs at the output of the switching regulator, the output voltage will fall very rapidly, together with the voltage at the input FB. The output signal of the error amplifier will exceed 1.5 V, and generate a Low level at the output of the SCP1.
Circuit Design Calculations with the TL5001

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7. Circuit Design Calculations with the TL5001

The design of a regulator circuit with the following characteristics is discussed below.

<table>
<thead>
<tr>
<th>Input voltage $V_{in}$</th>
<th>Output voltage $V_{out}$</th>
<th>Output current $I_{out}$</th>
<th>Switching frequency $f$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>200 kHz</td>
</tr>
</tbody>
</table>

The description of the individual components which follows is made assuming the circuit in figure 7.6.

7.1 Pulse duty ratio

The output voltage is derived from the average value of the input voltage, as a result of being switched on and off with a pulse duty ratio of $D$.

$$V_{out} = D \cdot V_{in}$$  \hspace{1cm} (10)

For an input voltage in the range of 24 - 40 V, the pulse duty ratio will be:

$$D_{max} = \frac{V_{out} + V_D}{V_{in \ min}} = \frac{5 \ V + 0.7 \ V}{24 \ V} = 24\% \quad ; \quad D_{min} = \frac{V_{out} + V_D}{V_{in \ max}} = \frac{5 \ V + 0.7 \ V}{40 \ V} = 14\%;$$

$V_D$ = Forward voltage of the diode
The switch on-time $t_{on}$ of the switching transistor can be derived from the pulse duty ratio and the chosen switching frequency.

$$
t_{on\ max} = \frac{D_{\ max}}{f} = \frac{0.24}{200 \ kHz} = 1.2 \ \mu s \\
t_{on\ min} = \frac{D_{\ min}}{f} = \frac{0.14}{200 \ kHz} = 0.7 \ \mu s
$$

### 7.2 Inductance

The inductance must be chosen to be sufficiently large to ensure that the regulator operates continuously over the required range of load current. The circuit should be designed such that continuous operation down to 10% of the maximum output current $I_{out\ max}$ is assured.

The minimum alternating current $\Delta I_{\ min}$ in the inductor (see figure 2.4) will therefore be as follows:

$$
\Delta I_{\ min} = 2 \cdot 0.1 \cdot I_{out\ max} = 1A
$$

For the pulse duty ratio, the larger of the values calculated above should be used. This then results in the following value for the inductance:

$$
L = \frac{(V_{in} - V_{out}) D_{\ max}}{\Delta I_{\ min} \cdot f} = \frac{(24 \ V - 5 \ V) \cdot 0.24}{1A \cdot 200 \ kHz} = 22 \ \mu H
$$

### 7.3 Output capacitance

The ripple voltage across the output capacitance is determined by the size of the filter capacitor. This ripple voltage superimposed on the output should be < 1 % of the DC output voltage.

The maximum permissible ripple voltage $V_{\ Ripple}$ at the output is:

$$
V_{\ Ripple} = V_{out} \cdot 0.01 = 5 \ V \cdot 0.01 = 50 \ mV
$$

According to Formula (9), the following value results (assuming ESR=0):

$$
C_{out} = \frac{Q}{V_{\ Ripple}} = \frac{\Delta I}{8 \cdot f \cdot V_{\ Ripple}} = \frac{2A}{8 \cdot 200 \ kHz \cdot 50 \ mV} = 25 \ \mu F
$$

In addition, account must be taken of the series resistance $R_{ESR}$ of the capacitor. This increases the alternating voltage superimposed on the output. Since the series resistance of an electrolytic capacitor depends on the voltage rating and the capacitance, a capacitor is recommended having a voltage rating which is double the required output voltage, and a capacitance which is about ten times the calculated value.

In this case, a capacitor with a capacitance of 220 $\mu F$ has been chosen.

### 7.4 Potential divider at the output

In order to regulate the output voltage, it is first divided down to 1 V with a resistive divider network, and then compared in the error amplifier of the pulse width modulator with the internal reference voltage $V_{ref1}$. 
\[
\frac{V_{\text{out}}}{V_{\text{ref1}}} = \frac{R_6 + R_7}{R_7}
\]

In this application, the output voltage is 5 V. The maximum resistance is determined by the input current of the error amplifier. With the TL5001, this is 160 nA. If the error resulting from this current should be \( \leq 1\% \), then the lateral current in the resistive divider network must be at least 100 times more than the input current of the error amplifier. In this case, a lateral current of about 0.5 mA has been chosen. The values of the resistors which then result are as follows:

\[
R_6 = 7.5 \, \text{k}\Omega \\
R_7 = 1.87 \, \text{k}\Omega
\]

The resistors must be of close tolerance (1 %), in order that the required value of the output voltage can be achieved.

### 7.5 Calculation of the oscillator frequency

The frequency of the oscillator is determined by a resistor \( R_t \) at the output \( R_T \). The oscillator frequency can be varied over a range of 40 kHz to 400 kHz. The necessary values of resistance can be read from figure 7.1. For a frequency of 200 kHz, a resistance value of \( R_t = 47 \, \text{k}\Omega \) is chosen.

![Figure 7.1: Oscillator frequency as a function of resistor \( R_t \)](image)

### 7.6 Overload protection

As mentioned above, the pulse width modulator TL5001 has built-in overload protection, which is activated when there is an overload at the output.
If an overload (e.g. a short circuit) is applied to the output of the switching regulator, the output voltage will collapse. The output signal of the error amplifier (see figure 6.1) will become High. As a result, the output of the SCP comparator 1 will be pulled to Low. The transistor Q2 will turn off, and the voltage across the resistive divider network $R_1/R_2$ will rise toward 2.5 V. The capacitor $C_{SCP}$ connected to pin 5 [SCP] will charge up until the voltage at the SCP comparator 2 reaches a value of 1 V. The output of this comparator will become High, and switch off the output via an inverter.

The voltage at the capacitor $C_{SCP}$ rises with an exponential function to:

$$V_{SCP} = 0.185 \text{ V} \cdot V_{ref3} \left(1 - e^{-t/\tau}\right); \quad V_{ref3} = 2.5 \text{ V} - 0.185 \text{ V} = 2.32 \text{ V}$$

$$\Rightarrow V_{SCP} = 0.185 \text{ V} \cdot 2.315 \text{ V} \left(1 - e^{-t/\tau}\right)$$  \hspace{1cm} (12)

The time constant $\tau$ with which the capacitor is charged depends on the capacitor $C_{SCP}$ and the resistor $R_{SCP}$:

$$\tau = R_{SCP} \cdot C_{SCP}$$

If this formula is inserted in (12) and solved for $C_{SCP}$, the value of the timing capacitor can be obtained which must be connected to pin 5, as a function of the desired time delay $t_{SCP}$.

$$C_{SCP} = 12.46 \times t_{SCP}$$

When finally determining the time delay $t_{SCP}$, care must be taken that it is longer than the initiation time of the circuit, otherwise the overload protection will be prematurely activated, and the voltage regulator will not operate.

In this circuit a delay time $t_{SCP} = 50$ ms was chosen, which corresponds to a capacitance of $C = 0.68 \mu\text{F}$ in figure 7.6.

### 7.7 Dead Time Control (DTC)

The pulse duty ratio can be limited by means of the dead time control. This makes it possible to prevent the switching transistor from being switched on during the complete cycle. This is achieved by the use of a resistor connected between Pin 6 and ground. A constant current $I_{DT}$ (figure 6.1) at Pin 6 generates a voltage drop across the resistor $R_{DT}$, which compared by the PWM/DTC comparator with the oscillator signal and the voltage at the output of the error amplifier. The use of the dead time control is however not absolutely necessary with a step-down converter, in contrast to step-up converters and flyback regulators.

In this circuit, the maximum pulse duty ratio $D$ is 24%. For the pulse duty ratio of the dead time control, a sufficiently large value can be chosen, in order to ensure that the performance of the regulator is not adversely affected by limitation of the pulse duty ratio. In this case, the maximum pulse duty ratio is 50%.
As described in Section 6, the pulse duty ratio is 0% when the voltage $V_{DT} \leq 0.7 \text{ V}$, and 100% when the voltage $V_{DT} \geq 1.3 \text{ V}$ or more. The voltage $V_{DT}$, which must be dropped across resistor $R_{DT}$ in order to achieve a dead time of 50%, can be determined from figure 7.2 (normal operation).

$$V_{DT} = D \left( V_{OSC_{\text{max}}} - V_{OSC_{\text{min}}} \right) + V_{OSC_{\text{min}}} = 0.5 \cdot (1.35 \text{ V} - 0.7 \text{ V}) + 0.7 \text{ V} = 1.025 \text{ V}$$

The voltage $V_{DT}$ is generated by the voltage drop caused by the current $I_{DT}$ (figure 5.1) flowing in the external resistor $R_{DT}$. The same current also flows in the resistor $R_t$ at the oscillator input RT. The external resistance $R_{DT}$ can be calculated with the formula:

$$R_{DT} = \left( R_t + 1.25 \text{ k}\Omega \right) \frac{V_{DT}}{1 \text{ V}}$$

In addition to limiting the pulse duty ratio, the DTC input can also be used to implement a soft start of the circuit. At the moment of switching on, the output voltage will not have reached its nominal value. The control amplifier attempts to balance this differential voltage as fast as possible. The result is that the pulse duty ratio immediately reaches its maximum value, leading to a very high current, and therefore a possible overload of the circuit. To prevent this, a capacitor $C_{DT}$ is connected in parallel with the resistor $R_{DT}$ to the input 6 (DTC). As a result, when switching on, the supply voltage $V_{DT}$ increases slowly and the pulse duty ratio rises with a time delay $\tau = R_{DT} \cdot C_{DT}$ (see figure 7.2). In this way, the current when switching on is limited. In order to prevent the overload circuit from operating when switching the regulator on, and the appearance of an apparent overload (output voltage = 0 V), the time constant $\tau_{DT}$ should be chosen to be about 10 times larger than the time constant $\tau_{SCP}$.

In this case, a time constant of 5 ms will be assumed. The resulting capacitance is:
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7.8 Compensating network

There is a LC network at the output of the switching regulator, which behaves like a second-order low pass filter. A second-order low pass filter has the property that the phase shift is 180°. If this signal is now applied to the inverting input of the error amplifier, unstable behavior will result. Compensation is added to the error amplifier to delay the phase reversal until the close loop gain is below 0 dB. In order to design the negative feedback loop correctly, the pole points and zero points of the output circuit must first be calculated.

The transfer function of the output circuit at low frequencies is as follows:

\[ F(s) = \frac{V_{out}}{V_{in}} = \frac{1}{s^2LC + 1} \quad (s = 2\pi) \]

The result of this is a double pole at:

\[ f_1 = \frac{1}{2\pi \sqrt{LC_{out}}} = \frac{1}{2\pi \sqrt{28 \mu H \cdot 220 \mu F}} = 2.027 \text{ kHz} \]

At higher frequencies, the influence of the series resistance \( R_{ESR} \) of the output capacitor \( C_{out} \) becomes apparent. This results in a zero at:

\[ f_2 = \frac{1}{2\pi R_{ESR} C_{out}} = \frac{1}{2\pi \cdot 0.035 \Omega \cdot 220 \mu F} = 20.7 \text{ kHz} \]

The total amplification of this configuration without negative feedback is determined by the maximum change of the output voltage of the circuit, which results from a change of the output voltage of the error amplifier.

The output voltage of the error amplifier will be assumed to be between 0.6 V and 1.4 V, this being slightly above or below the maximum and minimum values of control voltage. The pulse duty ratio of the oscillator is adjusted over a range of 0 and 100 %, by means of an input voltage of 0.7 to 1.3 V. If the minimum voltage of 0.6 V appears at the output of the error amplifier, the pulse duty ratio will be 0 %, and the output voltage of the regulator will fall to 0 V. At the maximum voltage, the pulse duty ratio will be increased to 100 %, and the input voltage will be switched directly to the regulator output. The amplification \( A \) can then be calculated as follows:

\[ A = \frac{\Delta V_{out_{max}}}{\Delta V_{Comp}} = \frac{20 \text{ V} - 0 \text{ V}}{1.4 \text{ V} - 0.6 \text{ V}} = 25 \Rightarrow A \text{ dB} = 20 \cdot \log 25 = 28 \text{ dB} \quad (13) \]

The Bode diagram for the uncompensated control loop is sketched in figure 7.3.
Figure 7.3: Amplification and frequency characteristics of the output circuit

The complex pole pair provides a 180° phase shift at \( f_1 \). The zero from the ESR can be seen at the frequency \( f_2 \).

The simplest solution would be to choose the amplification such that the critical frequency is less than 0 dB. This could be implemented with a simple integrator having a reduction of amplification of 20dB / decade. The disadvantage of this method is that, at a low degree of amplification, the output transient response is very poor. For this reason, the frequency at which the amplification is unity should be as high as possible.

A better solution is to arrange the negative feedback as shown in figure 7.4. This compensation network has 3 pole points and two zero points, which can be fixed by means of the correct calculation of the values for the individual components.
The Bode diagram for this compensation network is shown in figure 7.5.

The behavior of this feedback arrangement can be described as follows. The first pole of the feedback is at a frequency of 0. The transfer function is determined by the resistor $R_5$ and the capacitor $C_4$; $C_3$ can be neglected, since $C_4 \gg C_3$.

$$\frac{1}{s \cdot R_5 \cdot C_4} = 0$$

The reduction of the amplification of an integrator is 20 dB/decade, and the phase shift is -90°.
In order to compensate the phase shift of 180° due to the pole of the LC network, the compensating network must have a double zero at this frequency $f_1$. This means that the amplification must rise at 20dB/decade from the frequency $f_1$. The phase shift in this region is $+90°$, corresponding to the behavior of a differentiator. At the zero points of the transfer function, the behavior of the circuit will change from that of an integrator (-20 dB/decade), to that of a differentiator (+20 dB/decade). This means that the resistance $R_3$ in the feedback loop will be larger than the impedance of the capacitor $C_4$, and the impedance of the capacitor $C_7$ will be larger than $R_6$.

The zero of the transfer function is therefore:

$$s \cdot R_3 \cdot C_4 + 1 = 0 \quad \text{and} \quad s \cdot R_5 \cdot C_7 + 1 = 0$$

The next step is that the zero, which results from the series resistance $R_{ESR}$ of the output capacitor at the frequency $f_2$, must be compensated with a pole. From this pole, the amplification falls at a rate of 20dB/decade. There is therefore a constant amplification and a phase shift of 0° in the frequency range of $f_2$ to $f_3$. The pole is then attained when the resistance $R_8$ becomes larger than the resistance of the capacitor $C_7$. The pole then becomes:

$$s \cdot R_7 \cdot C_7 + 1 = 0$$

Finally, a pole is introduced at the frequency $f_3$, which lies between the previous pole and the oscillator frequency, in order to reduce the amplification at higher frequencies. The pole point is active when the resistance of the capacitor $C_3$ exceeds the resistance $R_3$. This pole is defined as follows:

$$s \cdot R_3 \cdot C_3 + 1 = 0$$

In order to correctly calculate the values for the resistors and capacitors, it must now be established that the total amplification is 0 dB at a frequency of $f_2$.

The amplification of the circuit at the frequency $f_2$ (20 kHz) without feedback is -12 dB. This requires the amplification of the compensating network to be +12 dB at this frequency. At the frequency $f_1$, the amplification will be 20 dB lower than at $f_2$ (see figure 7.5): in other words, it will be -8 dB. $C_4$ can be calculated from this as follows.

$$\frac{1}{2\pi \cdot f R_5 \cdot C_4} = 10^{\left(-8 \text{ dB}\right)} \Rightarrow C_4 = \frac{1}{0.398 \cdot 2\pi \cdot 2 \text{ kHz} \cdot 7.5 \text{ kΩ}} = 27 \text{ nF}$$

In the next step, $R_3$ can be calculated from the zero at 2 kHz:

$$s \cdot R_3 \cdot C_4 + 1 = 0 \Rightarrow R_3 = \frac{1}{2\pi \cdot f_1 \cdot C_4} = \frac{1}{2\pi \cdot 2 \text{ kHz}_1 \cdot 27 \text{ nF}} = 2.9 \text{ kΩ}$$

Calculations are now given for the values of all the remaining components in the compensating network.

$$s \cdot R_3 \cdot C_3 + 1 = 0 \Rightarrow C_3 = \frac{1}{2\pi \cdot f_3 \cdot R_3} = \frac{1}{2\pi \cdot 100 \text{ kHz}_1 \cdot 3 \text{ kΩ}} = 531 \text{ pF}$$
\begin{align*}
\text{s} \cdot R_5 \cdot C_7 + 1 &= 0 \quad \Rightarrow \quad C_7 = \frac{1}{2\pi \cdot 2 \text{ kHz} \cdot R_5} = \frac{1}{2\pi \cdot 2 \text{ kHz} \cdot 7.5 \text{ k}\Omega} = 10 \text{ nF} \\
\text{s} \cdot R_7 \cdot C_7 + 1 &= 0 \quad \Rightarrow \quad R_7 = \frac{1}{2\pi \cdot 20 \text{ kHz} \cdot C_7} = \frac{1}{2\pi \cdot 20 \text{ kHz} \cdot 10 \text{ nF}} = 795 \Omega
\end{align*}

Since the values which result above are not available in the commonly used range of component tolerances, the following standard values were used:

- \( R_3 = 3 \text{ k}\Omega \)
- \( R_7 = 820 \Omega \)
- \( C_3 = 470 \text{ pF} \)
- \( C_4 = 27 \text{ nF} \)
- \( C_7 = 10 \text{ nF} \)

### 7.9 Complete circuit diagram

The complete circuit diagram which results is shown in figure 7.6.
Figure 7.6: Complete circuit diagram of the voltage regulator
### 7.10 List of components

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Component</th>
<th>Value</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>TL5001</td>
<td></td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>R1</td>
<td>Carbon Film Resistor</td>
<td>10 kΩ</td>
<td></td>
</tr>
<tr>
<td>R2</td>
<td>Carbon Film Resistor</td>
<td>2.2 kΩ</td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>Carbon Film Resistor</td>
<td>3 kΩ</td>
<td></td>
</tr>
<tr>
<td>RDT</td>
<td>Carbon Film Resistor</td>
<td>43 kΩ</td>
<td></td>
</tr>
<tr>
<td>R4</td>
<td>Carbon Film Resistor</td>
<td>43 kΩ</td>
<td></td>
</tr>
<tr>
<td>R5</td>
<td>Carbon Film Resistor</td>
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<td></td>
</tr>
<tr>
<td>R6</td>
<td>Carbon Film Resistor</td>
<td>1.87 kΩ (1%)</td>
<td></td>
</tr>
<tr>
<td>R7</td>
<td>Carbon Film Resistor</td>
<td>820 Ω</td>
<td></td>
</tr>
<tr>
<td>R8</td>
<td>Carbon Film Resistor</td>
<td>100 Ω</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>Electrolytic Capacitor</td>
<td>100 µF</td>
<td>63 V</td>
</tr>
<tr>
<td>C2</td>
<td>Ceramic capacitor</td>
<td>100 nF</td>
<td>63 V</td>
</tr>
<tr>
<td>C3</td>
<td>Ceramic capacitor</td>
<td>470 pF</td>
<td></td>
</tr>
<tr>
<td>C4</td>
<td>Ceramic capacitor</td>
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<tr>
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<td>Tantalum electrolytic capacitor</td>
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</tr>
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<td>C6</td>
<td>Ceramic capacitor</td>
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</tr>
<tr>
<td>CDT</td>
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<tr>
<td>C8</td>
<td>Ceramic capacitor</td>
<td>100 nF</td>
<td></td>
</tr>
<tr>
<td>Cout</td>
<td>Tantalum electrolytic capacitor</td>
<td>4 x 47 µF</td>
<td>10 V</td>
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<tr>
<td>D1 - D4</td>
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<td></td>
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<tr>
<td>DZ</td>
<td>Zener Diode</td>
<td>22 V</td>
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<td>BYP100</td>
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<tr>
<td>L</td>
<td>Inductor</td>
<td>35 µH A6161-X002-80</td>
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</tr>
</tbody>
</table>
8. Efficiency

The efficiency $\eta$ is defined as the ratio of the output to the input power. With switching regulators, the efficiency is primarily determined by the characteristics of the external components.

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}}$$

8.1 Losses in the switching transistor

The losses in the switching transistor depend partly on the energy dissipated while the transistor is being switched, and partly on the voltage drop between Source and Drain while the transistor is switched on. Since the transistor is either switched off or in a saturated state, the last mentioned part is very small.

The losses which result while the transistor is being switched can be calculated from the current that is consumed during switching, and from both the duration of the switching process and the frequency. The static losses when switched on are determined by the resistance $R_{\text{DSon}}$ between Source and Drain. The power dissipation of the transistor is therefore made up of the sum of the switching and the static losses.

$$P_{\text{Trans}} = P_{\text{stat}} + P_{\text{dyn}} = \left(\frac{t_{\text{off}}}{t_{\text{on}} + t_{\text{off}}}\right) \cdot R_{\text{DSon}} + Q_{\text{gate}} \cdot V_{\text{GS}} \cdot f$$

8.2 Losses in the diode

The voltage drop across the diode in a conducting state is mostly responsible for the losses in the diode. The losses as a result of the diode can be calculated as the product of the forward voltage and the load current taken from the output.

$$P_{\text{Diode}} = V_{D} \cdot I_{\text{out}} \cdot \frac{t_{\text{off}}}{t_{\text{on}} + t_{\text{off}}}$$

The switching losses which occur at the change over from a conducting into a non conducting state are so small in comparison with the losses during the conducting phase, that they can be ignored.

8.3 Losses in the inductor

The inductor is an additional factor influencing the efficiency of the switching regulator. The losses in the inductor result from the resistance $R_{\text{Cu}}$ of the windings (copper losses).

$$P_{\text{Inductor}} = \left(\frac{t_{\text{out}}}{2}\right)^2 \cdot R_{\text{Cu}}$$

8.4 Overall losses in the circuit

The overall power dissipation in the circuit is the sum of the losses mentioned above in the individual components.
The overall efficiency which results is:

\[ \eta = \frac{P_0}{P_0 + P_{Total}} \]

9. Layout Guidelines

The mechanical construction of the circuit is just as important as the calculation of the component values for the switching regulator. When designing the layout of the printed circuit board for the regulator, care must be taken that the high frequency switching signals do not generate interference, either in the circuit or in the environment outside.

The metallization which conducts these high frequency switching signals on the circuit board should be kept as short as possible, such that interference can be neither emitted to the outside world nor coupled into the circuit. This will also reduce the inductance of the connections. As a result of the very short switching times the current is changing very rapidly, such that even low values of inductance in the connections can result in considerable voltage drops.

The ground lines of the power section and of the integrated circuit should be run separately, so that the high currents in the output circuit can not influence the regulating circuitry. Both ground lines must however be connected together at a single point, such that different potentials for the two grounds can not occur.

A capacitor of about 0.1 - 1 μF should be connected between the Source pin of the switching transistor and ground, which is able to carry the necessary current when switching occurs. Also in this case it is important to keep the wiring short, and to site the capacitor as close as possible to the Source pin.

The residual ripple in the output voltage results largely from the high inductance and the serial resistance \( R_{ESR} \) of the electrolytic capacitor. An improvement can be obtained here by connecting several smaller capacitances in parallel, as these will reduce both the inductance and the series resistance \( R_{ESR} \). The capacitors are connected in a star configuration to the grounding point and to the output voltage line.

The circuit arrangement described above can be seen in figure 9.1.
10. Additional applications Proposals

10.1 Step-Up Converter with the TL5001

It is also possible to design a step-up converter with the pulse width modulator TL5001. In a step-up converter, energy is stored in the inductor when the switching transistor is conducting. While this is happening, no energy is supplied to the output. In the non-conducting state, the...
energy stored in the inductor is passed via the diode to the output circuit. The result is that the output voltage is higher than the input voltage. In order to control the n-channel transistor, the output signal OUT from the integrated circuit must be inverted. In this example a special MOS driver TPS2816 is used, which inverts the signal and also supplies the current needed by the switching transistor in order to switch over.

![Figure 10.1: Step-Up Converter with the TL5001](image)

**Figure 10.1: Step-Up Converter with the TL5001**

### 10.2 Step-Down Converter for low output currents

If only low currents are needed at the output, then a switching transistor with a very low gate capacitance such as the TPS1101 can be used. In this case no external driver circuit is needed to charge and discharge the gate capacitance. A circuit proposal for a step-down converter of this type can be seen in figure 10.2.
Additional applications Proposals

Figure 10.2: Step-Down Converter for low output currents
11. Summary

This Application Report has explained the operation of the pulse width modulator TL5001, and given examples of several applications. This integrated circuit makes it a simple task to design various configurations of switching regulator.

Besides discussing the operation of this pulse width modulator, practical considerations which arise in the development and construction of switching regulators have also been covered.

The three examples of applications:

- a step-down converter,
- an step-up converter,
- and a down converter for low output currents,

demonstrate the use of the TL5001, and include practical proposals for constructing switching regulators.

12. References

Data Sheet TL5001 ...................................................................................................... SLVC084C
Applications report “Designing with the TL5001 PWM Controller” ..........................SLVA034A
Data Sheet TPS28xx ...............................................................................................SLVS132C
Power Supply Data Book....................................................................................... SLVD002
Internet: ............................................................................................................. http://www.ti.com