

Open Load Detection in Motor Drivers

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ABSTRACT

Better protection and better diagnostics is always the highest priority of any system board. The demand of various protection schemes to make the system robust and reliable is increasing day by day. Open load detection (OLD) is one of such protection scheme which determines the load's (motor or other loads) connectivity to the power-stage (for example external FET or integrated-FET motor driver). This article presents various types of open load detection (OLD) schemes / configurations, features and implementation in TI's motor drivers.

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1 Introduction

Open Load Detection (OLD) requirements are increasing to detect if any output terminals are disconnected from the motor (or other loads) to cater to safer and robust system. Open load detection can be done in three different ways depending upon the state of driving FETs (internal / external) as follows:

- **Passive Open Load Detection:** The passive open load detect also refers to the offline open load detect, where the detection of open load is carried before the driver is turned on. The state of all FETs remains in Hi-Z state, while a minimal amount of current flows through motor for short amount of time to test the motor connection. The diagnostic current is very small to avoid causing the motor rotation. The details of passive open load detection are presented in [Section 2](#)
- **Active Open Load Detection:** The active open load detection also refers to the online open load detection, where the detection of open load is carried during the driver / FET operation. This diagnostics features ensures that the load is always connected to the driver during the operation. While the motor is in operation, the FETs monitor the current flowing from one to another to ensure that motor is connected. The details of active open load detection are presented in [Section 3](#).
- **Pseudo-Active Open Load Detection:** In pseudo-active open load detection, the PWM-off time of the driver is utilized. In this scheme, the re-circulation current flowing into the body-diode of the FET is monitored to check the status of the motor connection to the driver. The details on the pseudo-active open load detection are presented in [Section 4](#).

Open load detection schemes are highly dependent on the type of load connection of the output terminals. The load connections can be classified into three configurations as explained in next section.

1.1 Load Connected to Supply

In this type of connection, the load (unidirectional motor or solenoid / relay load) is connected between the output (OUT1) and supply (VM) as shown in [Figure 1](#) (Passive OLD) and [Figure 2](#) (Active OLD). During the nominal operation, the load current flows (from VM to OUT1) when the low-side FET is turned ON and the high-side FET is turned off. The body diode of high-side FET's is utilized to re-circulate the current when the low-side FET turns OFF.

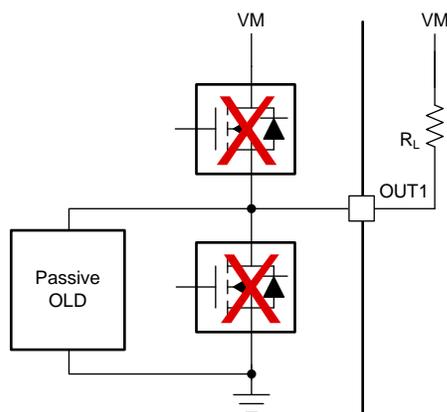


Figure 1. Passive Open Load Detection for Load Connected to Supply Voltage (VM)

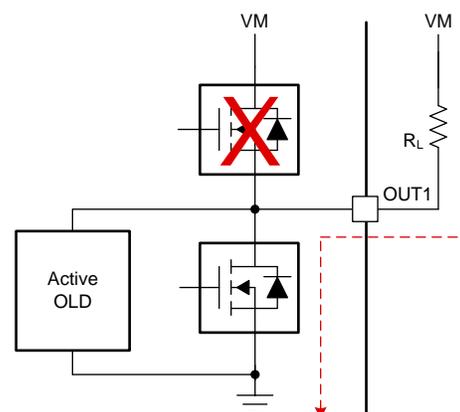


Figure 2. Active Open Load Detection for Load Connected to Supply Voltage (VM)

1.2 Load Connected to Ground (GND)

In this type of connection the load (unidirectional motor or solenoid / relay load) is connected between the output (OUT1) and ground (GND) as shown in [Figure 3](#) (Passive OLD) and [Figure 4](#) (Active OLD). During the nominal operation, the load current flows (from OUT1 to GND) when the high-side FET is turned ON and low-side FET's body diode is utilized to re-circulate the current when the high-side FET turns OFF.

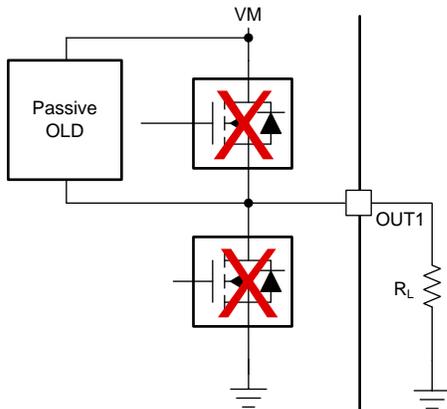


Figure 3. Passive Open Load Detection for Load Connected to Ground (GND)

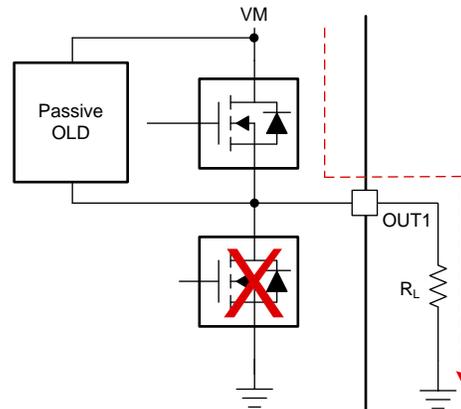


Figure 4. Active Open Load Detection for Load Connected to Ground (GND)

1.3 Motor Connected in Full Bridge Configuration

In this type of connection the load (bidirectional motor or solenoid / relay load) is connected between the two outputs (OUT1 and OUT2) as shown in Figure 5 (Passive OLD) and Figure 6 (Active OLD). This configuration is widely used for bidirectional control of motor. This configuration gives flexibility to change the direction of motor by opposing the polarity at OUT1 and OUT2. During nominal operation, the load current flows (between OUT1 and OUT2) when one of the half-bridge's high-side FET and other half-bridge's low-side FET is turned ON or vice versa.

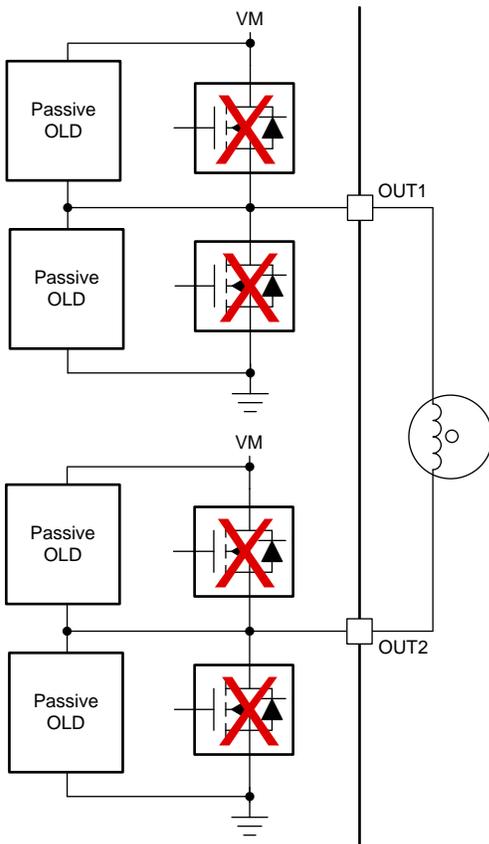


Figure 5. Passive Open Load Detection for Motor Connected in Full Bridge Configuration

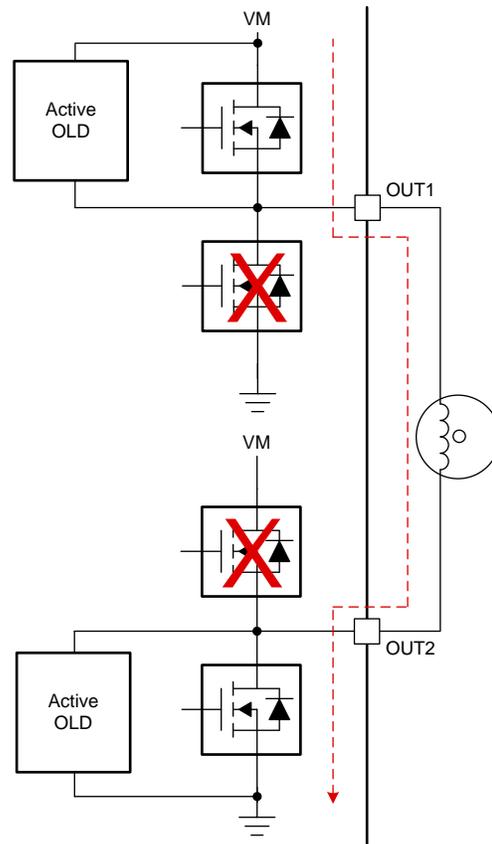


Figure 6. Active Open Load Detection for Motor Connected in Full Bridge Configuration

2 Passive Open Load Detection

The passive open load detection is also referred to the offline open load detection, where the detection of the open load is carried before the driver is turned on. This diagnostics feature ensures that the load is connected to the driver before switching it on. However, this scheme cannot detect if the motor terminal was disconnected from power-stage during the motor operation.

Figure 7 shows the circuit implementation of the passive open load detection. As shown in this figure, the high-side and low-side FETs of both half-bridges (OUT1 and OUT2) remain in Hi-Z state. Internal source / sink currents are allowed to flow to the load connected between the OUT1 and OUT2 half bridges during a set deglitch time, which is also limited by the motor's resistance. The diagnostic current is very low ($\sim 100 \mu\text{A}$) such that it doesn't rotate the motor in the open load detection time. If the motor (low-resistance path) is connected between OUT1 and OUT2, the diagnostics current is high and operate in saturation. However, if the motor is disconnected from the either of the OUT1 or OUT2 terminal, then the effective impedance becomes very high and current reduces to zero. This current variation is captured via the comparator trip connected on both high-side and low-side of the OLD circuit (as shown in Figure 7), which determines the state of load connection.

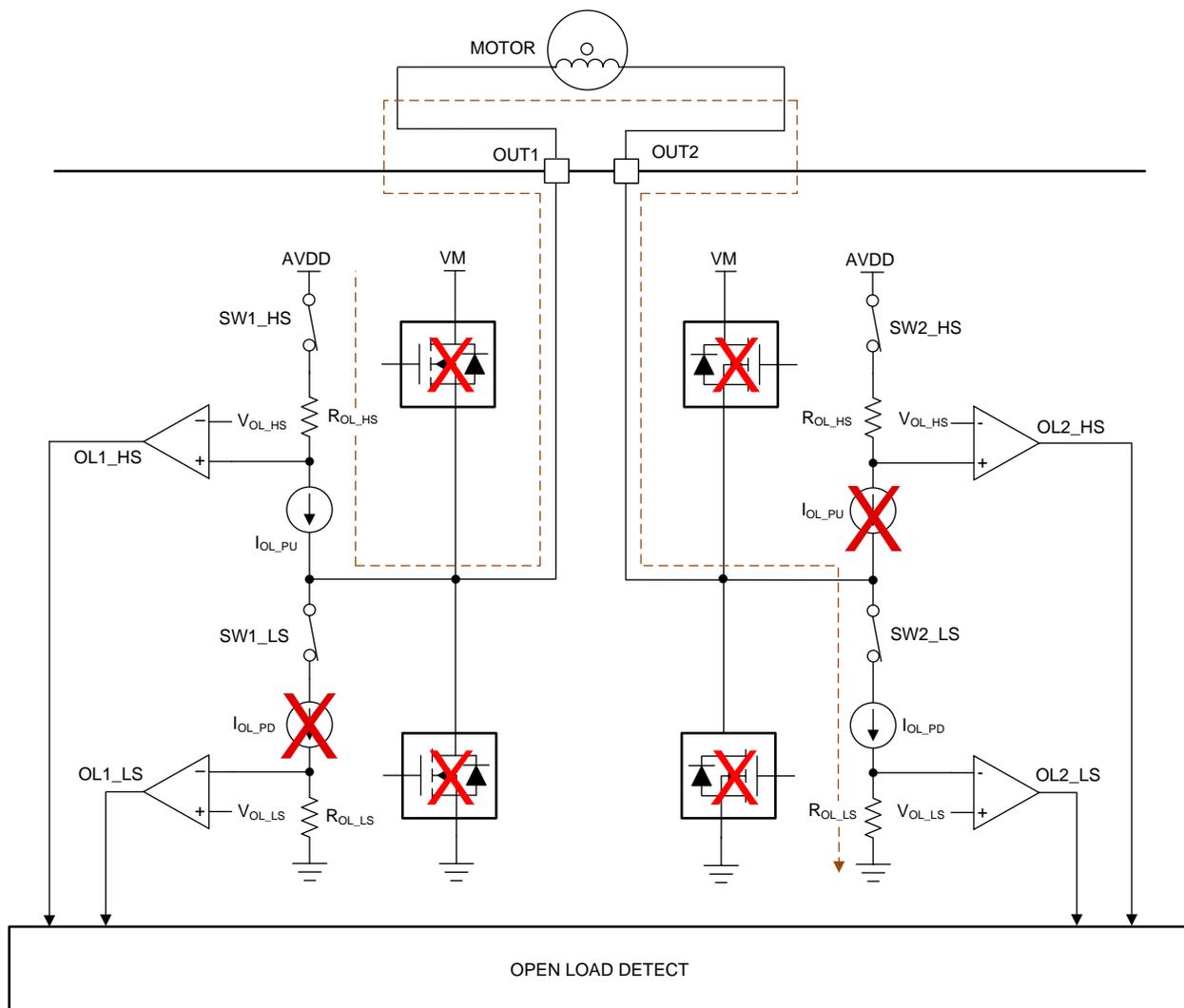


Figure 7. Passive Open Load Detection Circuit

2.1 Circuit Operation and Detection

This section presents the circuit implementation of the passive open load detection scheme of the [DRV8847](#) device. The full-bridge open load detection sequence consists of turning-on the high-side switch (SW1_HS) of half-bridge-1 and the low-side switch (SW2_LS) of half-bridge-2 together. Now, depending on the connection to the load, there can be three cases:

2.1.1 Full-Bridge Open

If no-load is connected between the OUT1 and OUT2 terminals, then no current flows from the internal regulator (AVDD). Now, the voltage-drop at the positive terminal of high side comparator of half-bridge-1 (OL1_HS) and the negative terminal of low side comparator of half-bridge-2 (OL2_LS) will be as follows:

High-side comparator of half-bridge-1 (OL1_HS)

Since no current is flowing from the internal regulator (AVDD), the voltage on OUT1 (which is also the positive terminal of OL1_HS comparator) is clamped to AVDD (for example 4.2-V). The comparator has positive input of OUT1 and negative input of V_{OL_HS} (which is fixed at 2.3-V). Since OUT1 is greater than V_{OL_HS} (2.3-V), the comparator output is set to a "1".

Low-side comparator of half-bridge-2 (OL2_LS)

For an open load condition, no current flows through the SW2_LS switch, which pulls down the negative terminal of OL2_LS comparator to 0-V (GND). This if compared with V_{OL_LS} (for example 1.2-V) sets the comparator output to "1". The comparator has negative input of OUT2 and positive input of V_{OL_LS} (which is fixed at 1.2-V). Since OUT2 is less than V_{OL_LS} (1.2-V), the comparator output is set to a "1".

Now, If both the comparator outputs (OL1_HS and OL2_LS) are high, it signifies an open load.

2.1.2 Full-Bridge Short

If there is short between the OUT1 and OUT2 terminals, then a short current (I_{SC}) will flows from the internal regulator (AVDD). It will depends on the high side resistor, R_{OL_HS} (12-k Ω) and low-side resistor, R_{OL_LS} (15-k Ω) resistor. The I_{SC} equation is as follows:

$$I_{SC} = \frac{V_{AVDD}}{15k\Omega + 12k\Omega} = \frac{V_{AVDD}}{27k\Omega} \quad (1)$$

Hence the short-current is calculated using [Equation 1](#) as,

$$I_{SC} = \frac{V_{AVDD}}{27k\Omega} = \frac{4.2V}{27k\Omega} = 155.56\mu A \quad (2)$$

Now, the voltage-drop at the positive terminal of high side comparator of half-bridge-1 (OL1_HS) and the negative terminal of low side comparator of half-bridge-2 (OL2_LS) will be as follows:

High side comparator of half-bridge-1 (OL1_HS)

Now, the pull up current of I_{SC} (155.56- μ A, short circuit current) is flowing from the internal regulator (AVDD), therefore the voltage at the positive terminal of OL1_HS comparator is calculated as,

$$V_{OL1_HS}(+) = V_{AVDD} - I_{SC} \times 12k\Omega \quad (3)$$

using [Equation 3](#), the $V_{OL1_HS}(+)$ is calculated as,

$$V_{OL1_HS}(+) = 4.2V - 155.56\mu A \times 12k\Omega = 2.33V \quad (4)$$

This voltage, if compared with V_{OL_HS} (2.3-V) sets the OL1_HS comparator output to "1".

Low side comparator of half-bridge-2 (OL2_LS)

The pull down current of I_{SC} (155.56- μ A) is flowing from the internal regulator (AVDD) to the SW2_LS switch. Therefore, the voltage at the negative terminal of OL2_LS comparator is calculated as,

$$V_{OL2_LS}(+) = I_{SC} \times 15k\Omega \quad (5)$$

Using [Equation 5](#), the V_{OL2_LS} is calculated as,

$$V_{OL2_LS}(+) = 155.56\mu A \times 15k\Omega = 2.33V \quad (6)$$

This voltage, if compared with V_{OL_LS} (1.2-V) reset the OL2_LS comparator output to "0".

Since, the OL1_HS comparator shows an output "1" and OL2_LS comparator shows an output "0", this case is considered as no-open load.

2.1.3 Load Connected in Full Bridge

The load current (I_L) for load (R_L) connected between the OUT1 and OUT2 terminals is calculated as,

$$I_{LOAD} = \frac{V_{AVDD}}{12k\Omega + R_L + 15k\Omega} = \frac{V_{AVDD}}{R_L + 27k\Omega} \quad (7)$$

Now, the voltage-drop at the positive terminal of high side comparator of half-bridge-1 (OL1_HS) and the negative terminal of low side comparator of half-bridge-2 (OL2_LS) will be as follows:

High side comparator of half-bridge-1 (OL1_HS)

If the voltage drop at positive terminal of OL1_HS comparator is higher than V_{OL_HS} (2.3-V), the comparator sets output to "1". Hence, the voltage required to trip the OL1_HS comparator is calculated as:

$$V_{OL_HS} < V_{AVDD} - I_{LOAD} \times 12k\Omega \quad (8)$$

By putting Equation 7 into Equation 8,

$$V_{OL_HS} < V_{AVDD} - \frac{V_{AVDD} \times 12k\Omega}{R_L + 27k\Omega} \quad (9)$$

By solving Equation 9, the load resistance (R_L) is expressed as,

$$R_L > \frac{V_{AVDD} \times 12k\Omega}{V_{AVDD} - V_{OL_HS}} - 27k\Omega \quad (10)$$

By putting the values of V_{AVDD} and V_{OL_HS} in Equation 10, the load resistance (R_L) is calculated as (-)10.2-k Ω . Since the value of the resistance is negative, the voltage at the positive terminal of OL1_HS comparator is always higher than V_{OL_HS} and the comparator output is always high ("1").

Low side comparator of half-bridge-2 (OL2_LS)

If the voltage at negative terminal of OL2_LS comparator is lower than V_{OL_LS} (1.2-V), the comparator sets to "1" showing as open load. Hence, the voltage required to trip the OL2_LS comparator is calculated as:

$$V_{OL_LS} > I_{LOAD} \times 15k\Omega \quad (11)$$

By putting Equation 7 to Equation 11,

$$V_{OL_LS} = \frac{V_{AVDD} \times 15k\Omega}{R_L + 27k\Omega} \quad (12)$$

By solving Equation 12, the load resistance (R_L) is expressed as,

$$R_L > \frac{V_{AVDD} \times 15k\Omega}{V_{OL_LS}} - 27k\Omega \quad (13)$$

By putting the values of V_{AVDD} and V_{OL_LS} in Equation 13, the load resistance (R_L) is calculated as 25.5-k Ω . Therefore, the output of OL2_HS comparator is set to 1, if the load resistance is greater than 25.5-k Ω .

Since the OL1_HS comparator always outputs "1", the open load status is solely dependent on the output of the OL2_HS comparator. If the OL2_HS comparator output is "1", then an open load is detected.

3 Active Open Load Detection

The active open load detection also refers to the online open load detection, where the detection of open load is carried during the driver / FET operation. This diagnostics features ensures that the load is always connected to the driver during the operation. However, it cannot detect if the motor terminal got disconnected from the power-stage before the motor operation.

Figure 8 shows the circuit implementation of the active open load detection. As shown in this figure, the high-side FET of the OUT1 channel and low-side FET of the OUT2 are in the operating state. The reference generator generates the equivalent reference voltage corresponding to the actual voltage drop in the main FET for comparing to the open load threshold. The main advantage of such an implementation is that it takes care of the measurement error due to the temperature and process variation. When the voltage drop in the main FET becomes lower than the reference voltage (as generated by the reference generator), the comparator trips, indicating that an open load event has occurred.

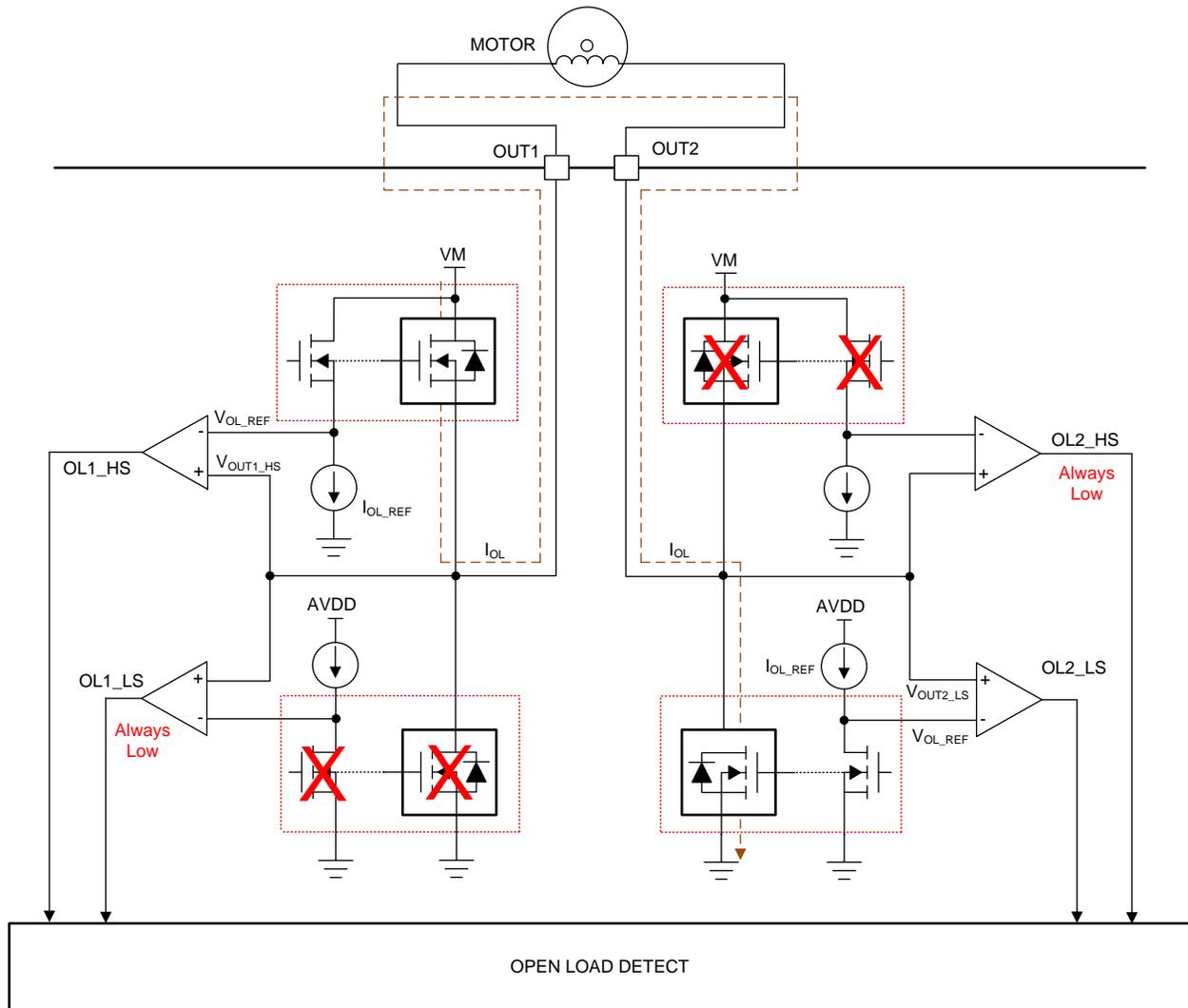


Figure 8. Active Open Load Detection Circuit

3.1 Circuit Operation and Detection

Figure 9 shows the operation of the active open load detection scheme. (Refer to DRV89XX-Q1 device family for more details). As shown in this figure, if any of the FETs are in operating condition (switched-ON) and the current flowing in the particular FET is lower than the open load current threshold (I_{OL}) for time magnitude larger than the open load deglitch time (t_{OLD}), then an open load condition is detected.

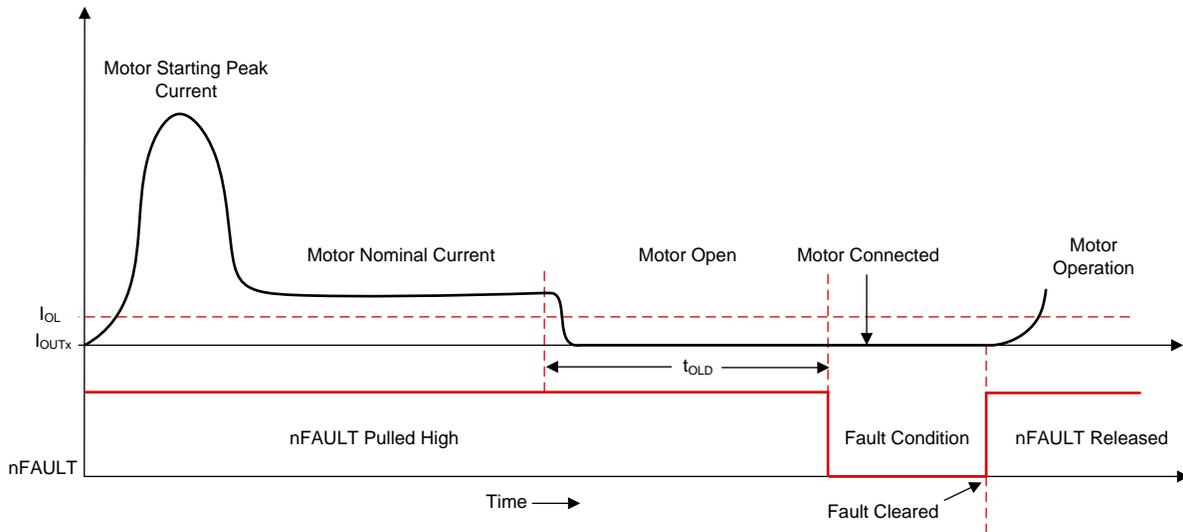


Figure 9. Active Open Load Detection Operation

As shown in Figure 8, the high-side comparator of OUT1 (OL1_HS) and the low-side comparator of OUT2 (OL2_LS) trips when the output voltages V_{OUT1_HS} and the V_{OUT2_LS} become equal to the comparator reference voltage (V_{OL_REF}),

$$\begin{aligned} V_{OL_REF} &= V_{OUT1_HS} \\ V_{OL_REF} &= V_{OUT2_LS} \end{aligned} \quad (14)$$

The reference voltage generated is determined by the pull-down current (I_{OL_REF}) and the on-state resistance of the sense-FET ($R_{DS(ON)_REF}$). Moreover, the voltage drop at the main power FET is determined by the main FET current (I_{OL}) and the on-state resistance of the main-FET ($R_{DS(ON)}$). Hence, by putting these values in Equation 14, this equation is modified as,

$$I_{OL_REF} \times R_{DS(ON)_REF} = I_{OL} \times R_{DS(ON)} \quad (15)$$

Hence, the main-FET current (I_{OL}) can be calculated as,

$$I_{OL} = I_{OL_REF} \times \left(\frac{R_{DS(ON)_REF}}{R_{DS(ON)}} \right) \quad (16)$$

Equation 16 determines that the open-load detection completely depends on the on-state resistance ratio of the sense-FET to main-FET.

Now, putting the values of on-state resistance ratio (450:1) and the reference generator pull-down current (20- μ A), the open load detection current (I_{OL}) is obtained as,

$$I_{OL} = (20 \times 10^{-6}) \times \left(\frac{450}{1} \right) = 9\text{mA} \quad (17)$$

Hence, if the main-FET current is lower than I_{OL} current (9-mA), an open-load event is registered.

4 Pseudo-Active Open Load Detection

In pseudo-active open load detection mode the open load detection is based on the voltage drop in high-side FET or body diode due to re-circulation current during high-side braking.

Figure 10 shows the circuit implementation of the pseudo-active open load detection. As shown in this figure, the high-side FETs of OUT1 and OUT2 channels are in operating state. The voltage drop across the conducting FET is compared with the fixed reference open load threshold voltage (V_{OLA}) to detect the open load detection event.

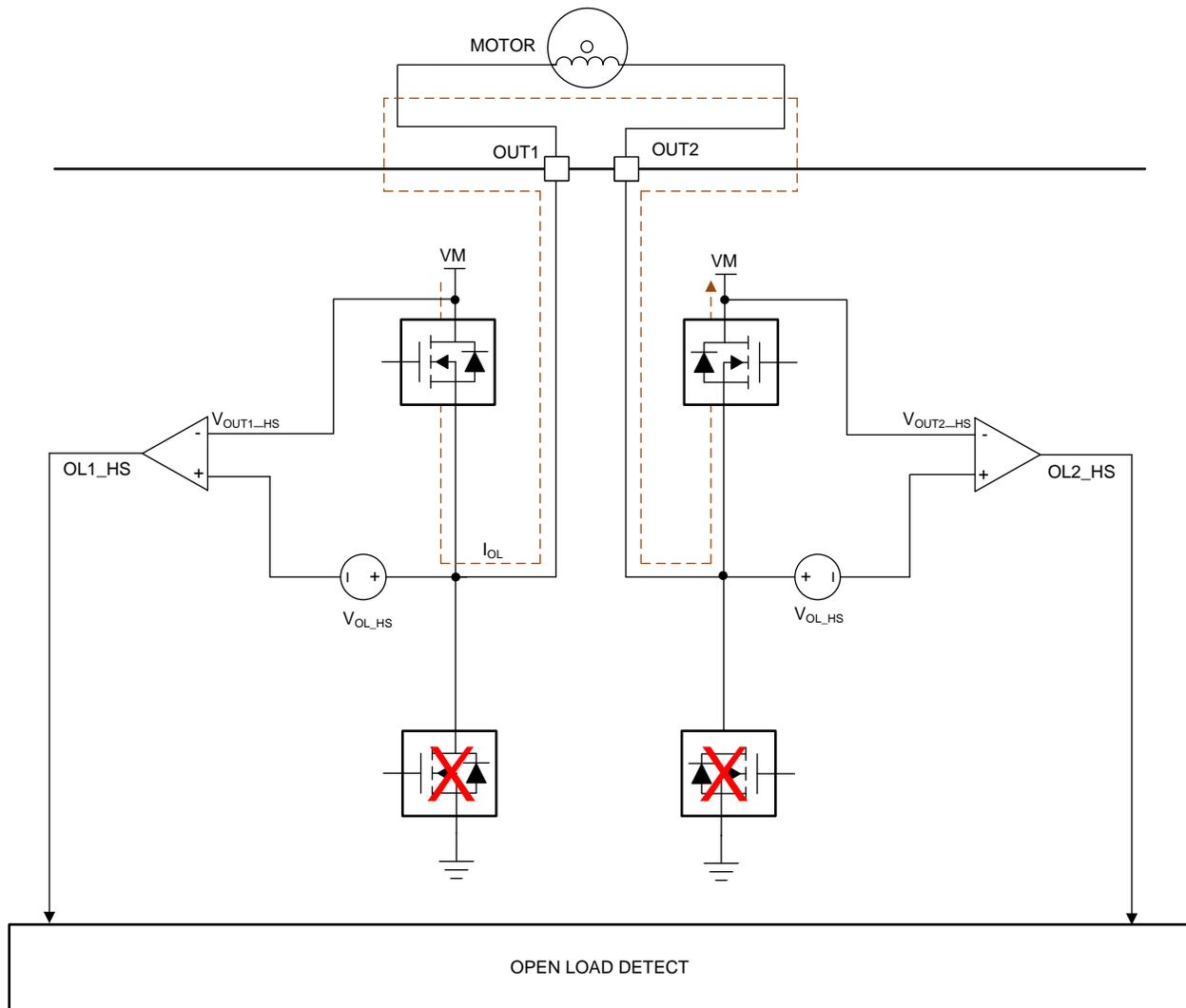


Figure 10. Pseudo-Active Open Load Detection Circuit

4.1 Circuit Operation and Detection

In pseudo-active open load detection, the body-diode voltage drop of the high-side FET during the current re-circulation (PWM OFF time) is monitored for the open load detection (Refer to [DRV8873-Q1](#) datasheet for further details). [Figure 11](#) and [Figure 12](#) shows the operation of the full-bridge with current re-circulation through body-diode (for open load detection) or high-side FET (for nominal operation in synchronous rectification) respectively. If the body-diode voltage drop is lower than the V_{OL_HS} threshold, an open load is detected. Below example shows the calculation of open load threshold's current in DRV8873-Q1 device.

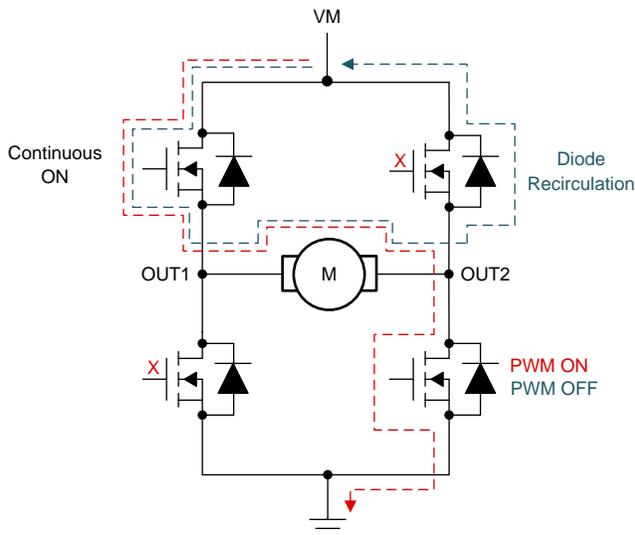


Figure 11. Reticulation Current flow through Body-Diode for Open Load Detection

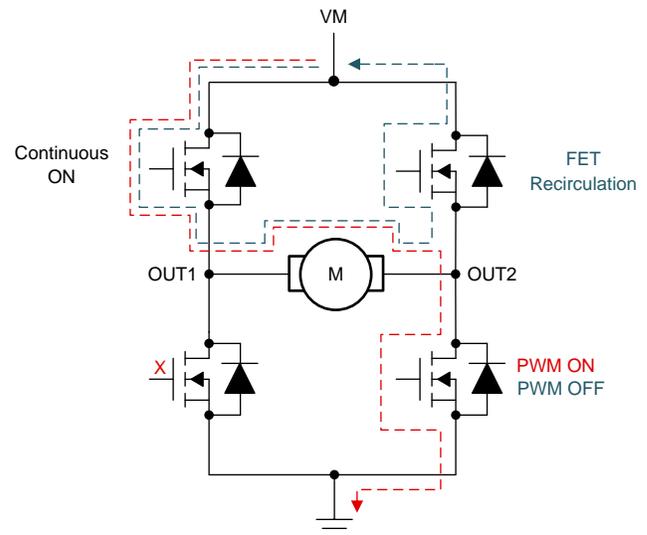


Figure 12. Nominal Operation of Braking through High-Side FET

The open load detect comparator (OL2_HS) is set if the voltage drop at OUT2 terminal (V_{OUT2_HS}) is lower than the open load threshold voltage (V_{OL_HS}) as,

$$V_{OL_HS} = V_{OUT2_HS} \tag{18}$$

For current re-circulation through body-diode, the voltage drop is dependent on the body-diode current (I_{OL}) of the high-side FET as shown in [Equation 19](#).

$$V_{OL_HS} = V_{OUT2_HS} = V_D(I_{OL}) \tag{19}$$

The open load detect comparator (OL2_HS) will trip if the voltage drop across body-diode (V_D) is lower than the open load threshold (V_{OL_HS}). For DRV8873-Q1, the typical voltage threshold value of the open load detect comparator is 300-mV.

5 Summary

This article has presented three types of open load detection schemes: passive, active and pseudo-active open load detection along with different load connections such as the load connected to supply, ground or connected in full-bridge configuration.

The passive open load detection scheme is suited for the applications which require to check the connectivity of the driver to the motor before powering the driver. In such applications, there can be hazard of the open wire connecting to other low-voltage circuitry (chances of damaging the low-voltage components) or power lines which can cause the overcurrent event.

The active and the pseudo-active open load detection scheme is suited for the application where the driver current is to be always monitored while the motor is running. The pseudo-active open load detection allows the open load detection only during the PWM-off time, which limits its operation for the continuous mode. Whereas, active open load detect can operate in both continuous and PWM operation.

6 References

- Texas Instruments, [DRV8847 Dual H-Bridge Motor Driver](#) Datasheet, August 2018.
- Texas Instruments, [DRV89xx-Q1 Automotive Multi-Channel Half-Bridge Driver](#) Datasheet, January 2019.
- Texas Instruments, [DRV8873-Q1 Automotive H-Bridge Motor Driver](#) Datasheet, August 2018.

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