Application Report

TPS55288 Layout Guideline

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ABSTRACT

The TPS55288 is a synchronous buck-boost converter optimized for converting battery voltage or adaptor voltage into power-supply rails. In addition to the schematic design and proper external components selection, board layout is also critical to the success of a buck-boost design. This application note details a guidance on how to route the TPS55288 buck-boost converter to achieve stable operation, and good thermal and low EMI performance.

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1 Introduction

The TPS55288 buck-boost converter is widely used in the USB Type-C™ PD applications, like industry PC, car charger, and dockings. The output power range can be from around 10 W to 100 W based on the different input voltage.

A well-planned PCB layout is fundamental to careful system design of any DC/DC or AC/DC power converter. An optimized layout leads to better EMI performance, better thermal performance, and good stability performance within a relatively smaller solution size. So an optimized layout means higher reliability, lower cost, and faster release time to market.

This application note gives out the TPS55288 buck-boost converter layout guideline. Under the guidance of this application note, the customers can achieve the above goals easily with a 4-layer PCB. The main content includes identification of the critical switching loops, power-stage component placement, power circuit, and signal circuit routing, AGND and PGND connection, power and GND copper plane design.

2 TPS55288 Layout Guide Line

2.1 Identification of the Critical Switching Loops

Figure 2-1 shows the TPS55288 four-switch buck-boost converter with power stage components, an integrated gate drivers and a VCC bias supply. Figure 2-1 also distinguishes by color the high current traces, high dI/dt critical loops, and the high dv/dt switching nodes.

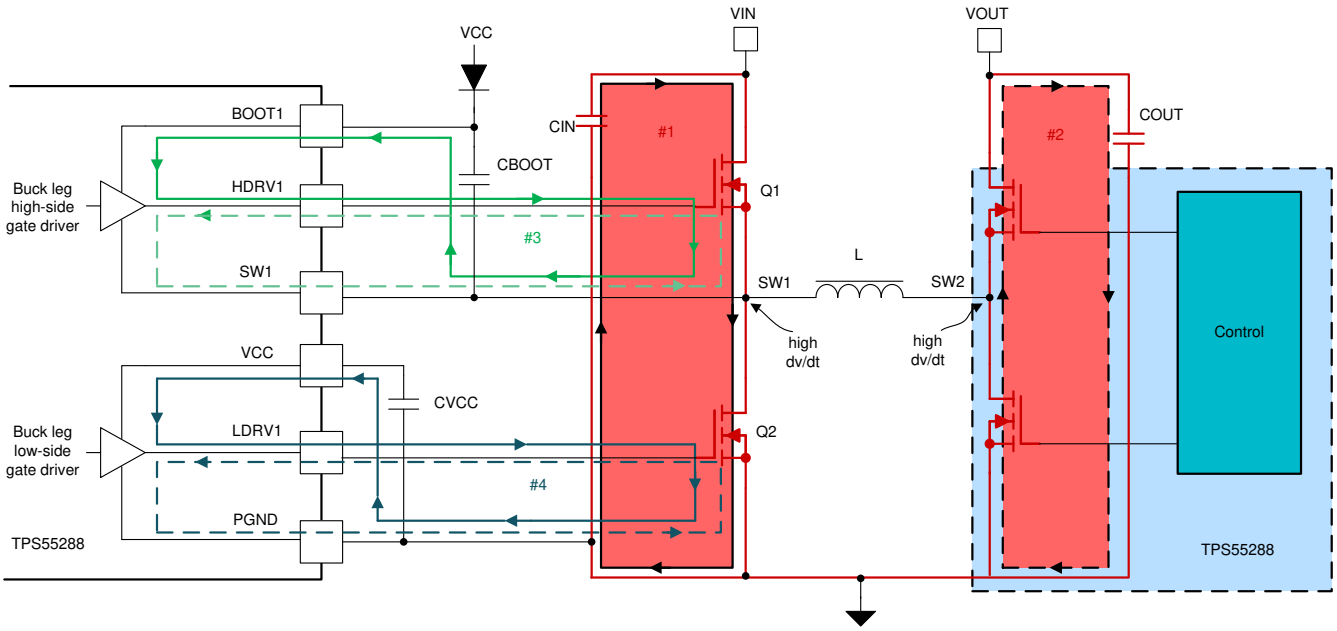

Figure 2-1. Buck-Boost Converter Schematic With Critical Loops

Loop 1 and loop 2, shaded in red, are the two critical high-frequency power loops for the buck-legs and the boost-legs. Long and thin traces in these two loops can cause excessive noise, overshoot, and ring on the switch node, and the ground bounce because of the parasitic inductance. During a MOSFET switching event, the slew rate of the commutating current can exceed 3–5 A/ns, so a 2-nH parasitic inductance can result in a voltage spike of 6 V. The pulsed rectangular current waveforms flowing in these critical loops are rich in harmonic content, so a big loop area can cause big radiated energy emanating from it, which causes an electromagnetic interference issue. So it is vital to minimize the trace length and the enclosed area of loop 1 and loop 2.

The current flowing in the main inductor is largely DC, with a superimposed triangular current ripple. The inductance inherently limits the current change rate. The parasitic inductance in series with the main inductor is benign. At the meanwhile, the area of the switching node SW1 and SW2 should be as small as possible. If the SW1 and SW2 are poured with big area copper planes, the high dv/dt noisy signal will couple into other traces nearby though capacitive coupling, which causes the electromagnetic interference issue.

Loop 3 and loop 4 in Figure 2-1 are gate loops for the buck-leg MOSFET. Loop 3 represents the high-side gate driver circuits of the MOSFET supplied by the bootstrap capacitor. Loop 4 represents the low side gate driver circuits of the MOSFET supplied by the VCC capacitor. The turn-on path and the turn- off path are denoted by the solid and the dashed lines, respectively. To charge and discharge the gate capacitance of the MOSFET during turn-on and turn-off transitions, an instantaneous current up to around 1-A peak flows briefly in the gate loop.

Placing the VCC decoupling capacitor very close to the VCC and PGND pins, placing the bootstrap capacitor very close to the SW and the boot pins can reduce the gate loop enclosed areas. Route the gate drive traces from the silicon to the MOSFET as short as possible, routing the gate drive and the return traces side by side can minimize the gate-loop inductance and the gate-loop area.

2.2 Power Component Placement

Figure 2-2 illustrates the placement of the power MOSFETs, input and output ceramic capacitors, main inductor, and the TPS55288 silicon on the top layer.

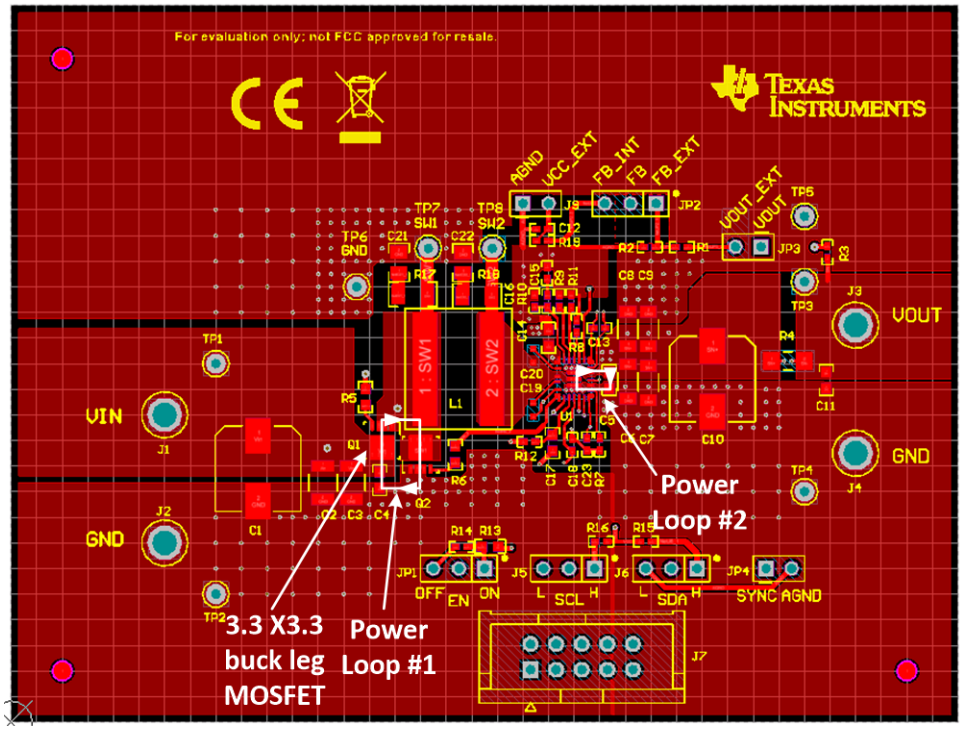

Figure 2-2. Power Stage Components Placement

Input capacitors are placed close to the buck-leg MOSFETs. Output capacitors are placed adjacent to the TPS55288's VOUT pin and PGND pin. A small enclosed area of the power loop 1 and power loop 2 can be achieved by proper placement.

The main inductor L1 is placed between the buck-leg MOSFETs and the TPS55288 silicon. The SW node is poured with small copper plane to reduce the capacitive coupling relating to the SW node high dv/dt transitions. A large SW node copper plane helps the thermal, but will cause severe radiated emissions.

2.3 Driver Circuit and Signal Circuit Routing

Figure 2-3 and Figure 2-4 show the gate drive traces running from the IC to the buck-leg MOSFETs. The drive traces are routed on layer 1 and 3. Kelvin – connecting the gate drive return traces directly to the respective MOSFET sources minimize common-source inductance. To minimize gate-loop area, gate and source traces are routed side by side as differential pairs. The return current for the low side MOSFET gate driver flows on the GND plane back to the PGND pin of the IC. The gate drive resistors should be placed close to the gate terminal of each MOSFET.

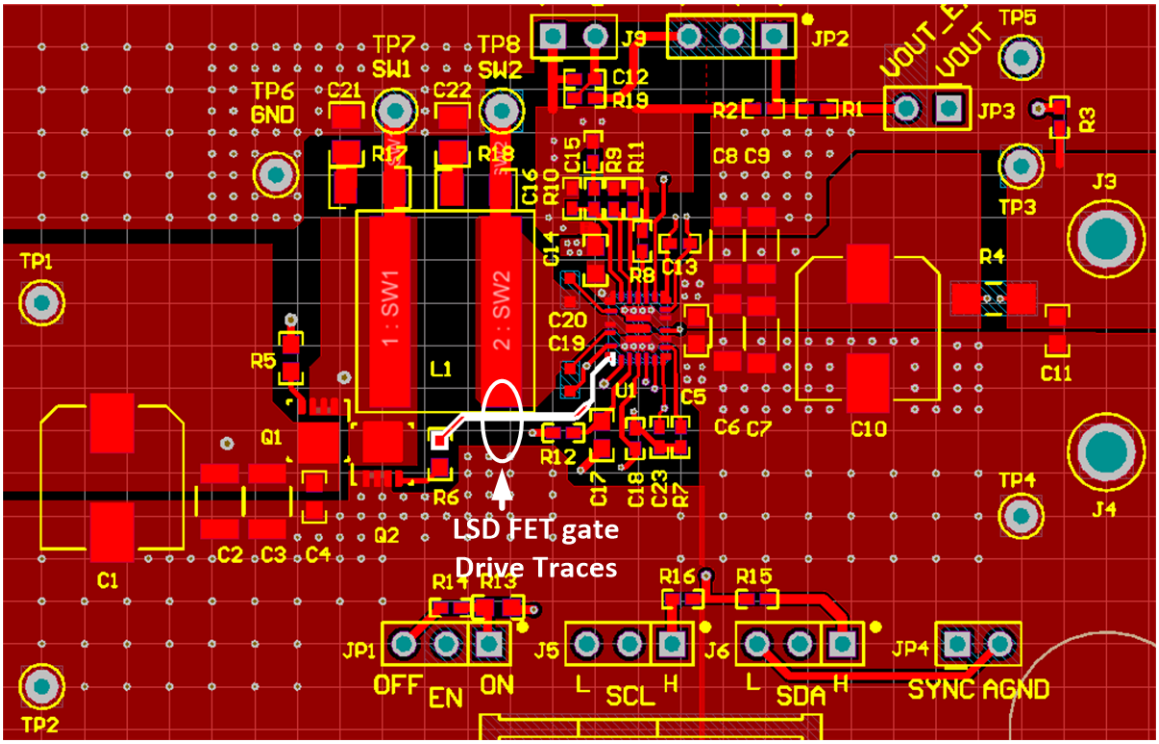

Figure 2-3. Low-Side-FET Drive Traces Routing

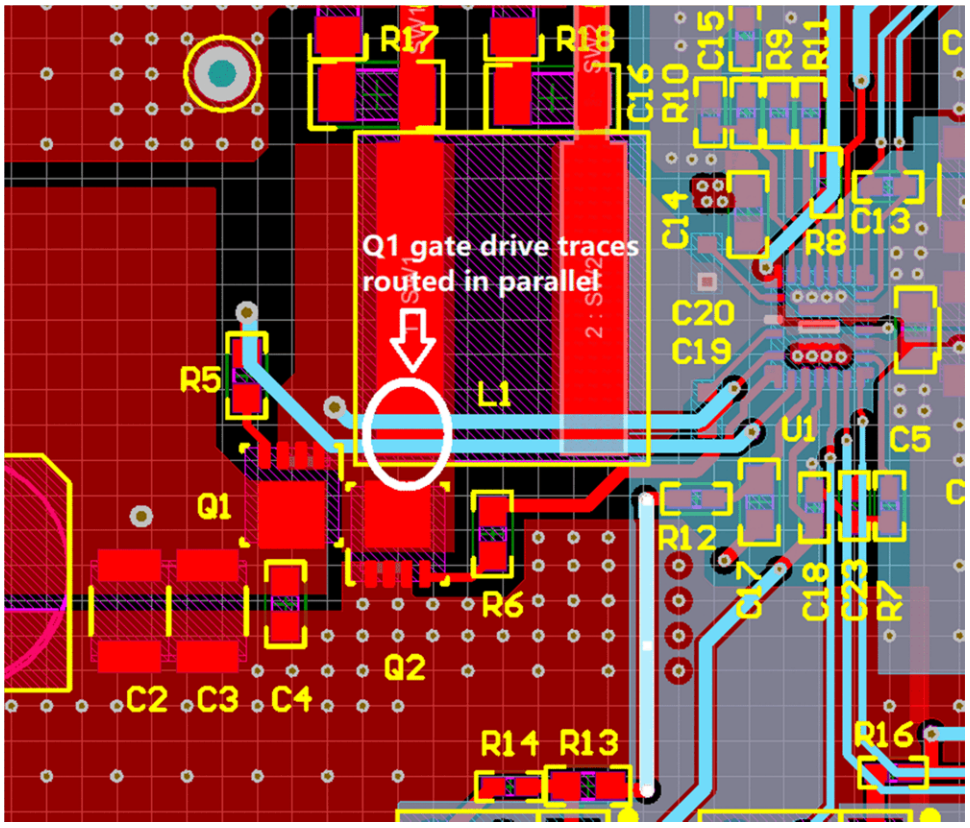

Figure 2-4. High-Side-FET Drive Traces Routing

Figure 2-5 shows the traces for the output current sensing. The traces were routed as a tightly-coupled differential pair from the shut resistor to the IC, which can enhance the noise immunity and the accuracy. Place the current-sense filter capacitor close to the IC.

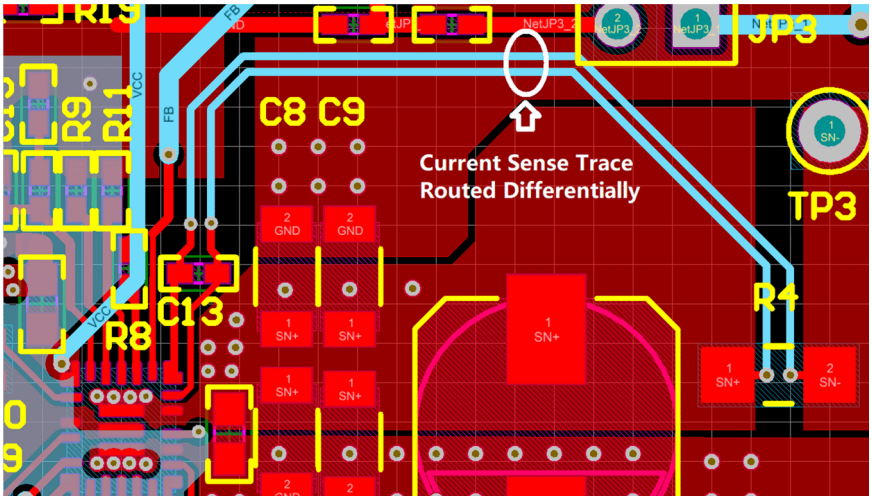

Figure 2-5. Output-Current-Sense Traces Routing

Figure 2-6 shows the AGND and the PGND connection. AGND and the PGND pin of the TPS55288 are directly poured together at the top layer. The GND net of the feedback network and the compensation network connected with the GND copper plane with vias. The VCC capacitor should be placed as close to the IC as possible. The GND net of the VCC capacitor should be directly connect with the GND plane at the inner layer through vias, so that the VCC supply current can return to the PGND of the IC with low impedance.

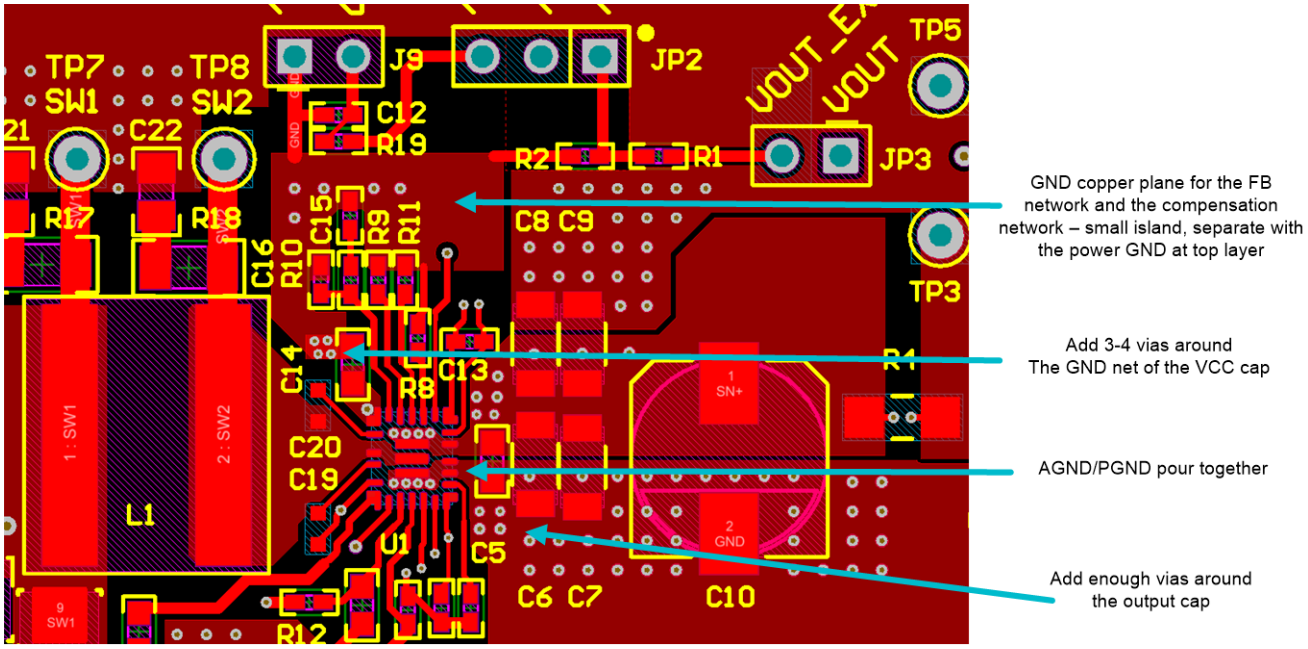

Figure 2-6. AGND-PGND Connection

2.4 Power and GND Plane Design

While paying special attention to the component placement, critical traces and loop routing, inner layer GND copper plane routing is also important. Placing a whole layer GND copper plane under the switching loops establish a passive shielding for the circuit. By Lenz's law, the current in the shield layer generates a magnetic field to counteract the original switch-loop magnetic field. The result is magnetic flux reduction and better EMI performance. Having an uninterrupted, whole GND copper plane right under the high frequency switching-loops offers the best performance.

For the high-power integrated boost or buck-boost converters, thermal performance is critical to the success of the circuit design. Thermal performance determines the system reliability. TI recommends using thermal vias beneath the TPS55288 connecting PGND pin and VOUT pin to the PGND plane and a large VOUT area separately. Figure 2-7 and Figure 2-8 show examples of a proper layout with good thermal performance. Two whole GND layers are placed on layer 2 and layer 4. A large VOUT area is placed on layer 3.

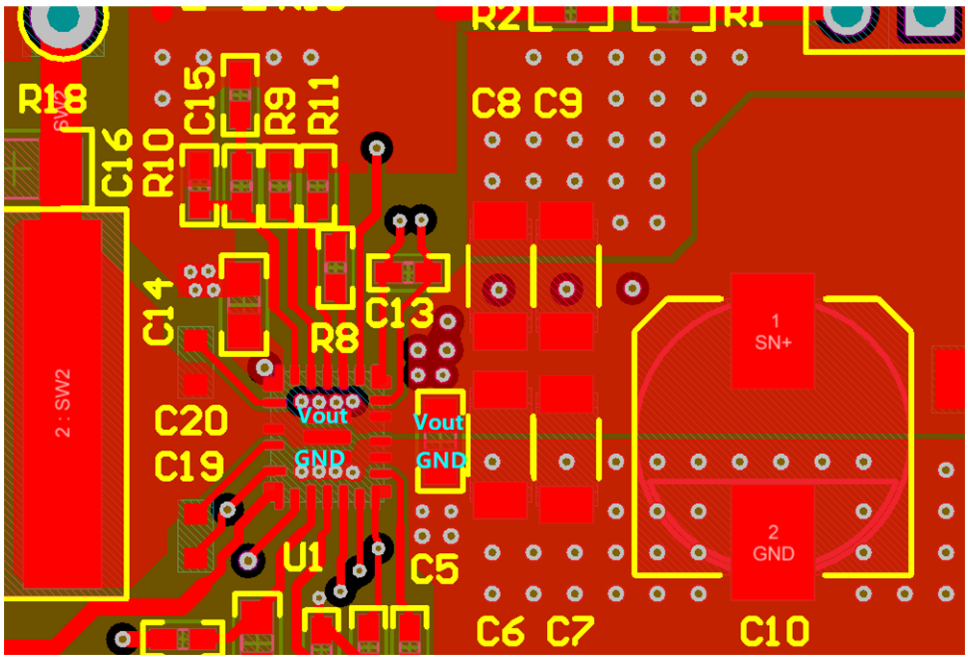

Figure 2-7. Place Thermal-Vias on the PGND Pin

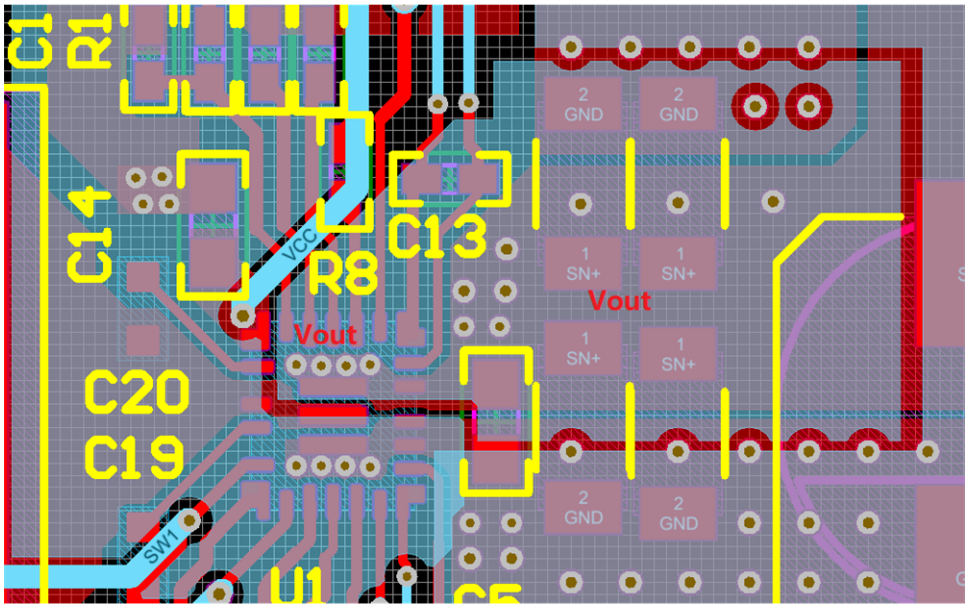

Figure 2-8. Place Thermal-Vias on the VOUT Pin

3 Summary

This application note describes how to route the TPS55288 buck-boost converter with a 4-layer printed circuit board. It begins with the identification of the critical switching loops. By proper power component placement, keeping critical loops small, placing a whole layer GND copper plane under the switching- loops, and carefully routing the sensitive traces, you can achieve a success buck-boost converter design.

4 References

- Texas Instruments, *TPS55288 36-V, 16-A Buck-boost Converter with I²C Interface Data Sheet*
- Texas Instruments, *Reducing Radiated EMI in TPS61088 Boost Converter Application Report*
- *Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter*

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2020) to Revision B (December 2020) **Page**

Changes from Revision * (June 2020) to Revision A (August 2020) **Page**

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