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Input Output Mode Application Note

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ABSTRACT

The TI-GC5016 is a multi-function Digital Down Converter (DDC) and Digital Up Converter (DUC). The DDC and DUC functions have a variety of input and output modes. This application note illustrates the input and output modes, external connections, timing relation to external devices, and cmd5016 programming.

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1 GC5016 Input and Output Buses (seeFigure 1)

The GC5016 has four input buses, four output buses, a sync bus, and a control bus.

- In the DDC mode, the input buses are connected to the high-speed output of other signal processing equipment or ADC outputs. The output buses are connected to the lower speed baseband digital signal processing equipment. The Ck clock input is used to sample the input and register the output DDC signals. The frame strobe signal identifies the start of the DDC data output cycle.
- In the DUC mode, the output buses are connected to the high-speed input of other signal processing equipment or DAC inputs. The input buses are connected to the lower speed baseband digital signal processing equipment. The Ck clock input is used to sample and clock-out the DUC signals. The frame strobe signal identifies the start of the DUC data input cycle.
- The sync bus can be used to synchronize one or more GC5016s with other signal processing equipment. The $\overline{\text{SIA}}$ and $\overline{\text{SIB}}$ are the sync inputs. The $\overline{\text{SO}}$ is the sync output.
- The Ck clock input is used to sample the sync inputs. The Ck clock is used to clock-out the sync output signal.
- External Reset $\overline{\text{RST}}$– The external reset must be low until VCore is stable. Alternatively, this input must be pulled up. This pin is NOT designed as a sync input pin.
- The control bus is used to program the GC5016 registers to perform specified DDC or DUC functions.
- The control bus can have a chip enable and single strobe, or a chip enable and dual strobe. The two-wire (single strobe) mode is compatible with older GC devices.

The control bus is not synchronized with the Ck signal. The WRMODE, $\overline{\text{WE}}$, and $\overline{\text{RD}}$ identify the local bus cycle. There are four different control bus modes. Each is shown in a figure in the data sheet:

WRMODE	$\overline{\text{WE}}$	$\overline{\text{RD}}$	DESCRIPTION
GND			Pulse write – edge with dual strobe(1) Control data registered on first rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$
GND		GND	Pulse write – edge with single strobe Control data registered on first rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$(2)
VCC-IO			Latch write – with dual strobe Control data is held during entire $\overline{\text{WE}}$ cycle access
VCC-IO		GND	Latch write – with single strobe Control data is held during entire $\overline{\text{WE}}$ cycle access

(1) Recommended control bus mode
(2) The $\overline{\text{WE}}$ must be active before $\overline{\text{CE}}$ in this mode.

The control bus consists of:

$\overline{\text{CE}}$– Chip enable active low
WRMODE – static configuration pin for Write cycle, recommend GND (*)
$\overline{\text{WR}}$– Write strobe, active low
$\overline{\text{RD}}$– Read strobe, active low
Adr[4..0] – Address bus
C[15..0] – Bidirectional control bus

JTAG – The JTAG connections are not part of this application note. In general IO terms, if JTAG is not used, $\overline{\text{TRST}}$ must be connected to GND. The pin names are TMS, TDI, TCK, TDO, and TRST. To use JTAG, without driving the $\overline{\text{TRST}}$ through the JTAG connections, the $\overline{\text{TRST}}$ must be connected to a VCore power supervisory circuit that transits from 0->1 after VCore is within limits.

2 GC5016 DDC Input Bus Configuration

The GC5016 DDC input bus can be configured in several modes:

- Real Input – Each input port represents a real sample sampled with the Ck clock.
- Interleaved Complex – Each input port represents a 1/2 rate complex signal. The I or Q data is received on each Ck clock. A special synchronization is required for this mode, from the sync input 0->1 transition aligned with the Q input.
- Parallel Complex – A pair of inputs A-B and C-D are used to input the full rate complex sample. The I and Q data is received on each Ck clock.
- Double Rate Real Input – A pair of inputs A-B and C-D are used to input double rate data as even and odd samples. The even and odd samples are received on each Ck clock.
- Double Rate Complex Input – All four input ports are used to sample one double rate complex signal. The double rate complex input can be processed by DDC A-B and C-D separately.

DDC INPUT MODE	Rin_rate	Rin_cmplx	PORTS USED
Real – Full Rate	1	0	1 port, 2s complement Real input
Interleaved Complex – Half Rate	0	1	1 port, 2s complement, Interleaved complex input, synchronized to zpad_sync
Parallel Complex – Full Rate	1	1	2 ports, A-B or C-D. A and C are I, B and D are Q
Real – Double Rate	2	0	2 ports, A-B or C-D. AC are even real, BD are odd real
Complex – Double Rate	2	1	4 ports. A-even I, B-even Q, C-odd I, D-odd Q

The cmd5016 channel command, mix_rcv_sel, selects one of four input buses. The value to select an input bus is:

0-A
1-B
2-C
3-D

The real interleaved complex and parallel complex input modes can use receive interpolation. The receive interpolation is controlled by the Rinf_zpad variable. Rinf_zpad is the number of zeros inserted between samples. The real input and parallel complex input modes insert zeros between each valid input sample. The interleaved complex mode alternates between a zero and the Q sample (both I and Q are used, at the Q sample time).

The Rinf_zpad function is common to all DDC channels.

The DDC input modes can be used to process a specific range of inputs:

Double Rate Complex	Complex –> -Ck to 5016 Clock Rate (Ck)
Double Rate Real	Real –> 0 to 5016 Clock Rate (Ck)
Parallel Complex	Complex -> -Ck/2 to Ck/2 Rate
Interleaved Complex	Complex -> -Ck/4 to Ck/4 Rate
Real	Real -> 0 to Ck/2

2.1 DDC Input Timing Registration (see Figure 2)

The input data to the GC5016 DDC input buses must meet the TSetup and THold time relative to the Ck input clock.

2.2 DDC Rinf_Zpad Timing (See Figure 2)

A special synchronization selection for zpad_sync is used to align the zpad counter with an external event. The 0 ->1 sync signal is aligned with the Q input data.

2.3 DDC Real Input – (See Figure 3)

The GC5016 in real input DDC mode has four input buses. Each input bus uses 2s complement data format and has 16 bits. If the customer input is less than 16 bits, the data is MSB aligned or sign-extended. Unconnected input bits must be connected to GND.

2.4 DDC Interleaved Complex Input Timing – (See Figure 4)

The GC5016 DDC interleaved complex input requires special timing to align the I and Q input. The external sync input must identify the Q data sample two Ck cycles before the 0->1 sync signal.

2.5 DDC Interleaved Complex Input – (See Figure 5)

The GC5016 in interleaved complex input DDC mode has four input buses. Each of the four channels can have a ½ rate complex input. Each input bus uses 2s complement data format and has 16 bits. If the customer input is less than 16 bits, the data is MSB aligned or sign-extended. Unconnected input bits must be connected to GND.

2.6 DDC Parallel Complex Input – (See Figure 6)

The GC5016 in parallel complex input DDC mode has two input buses. Each of the four channels can select either of the two parallel complex input sets. Each input bus uses 2s complement data format and has 16 bits. If the customer input is less than 16 bits, the data is MSB aligned or sign-extended. Unconnected input bits must be connected to GND.

2.7 DDC Double Rate Real Input – (See Figure 7)

The GC5016 can process two double rate real inputs. The double rate mode requires a special mode called Split IQ. In this mode two DDC channels, A-B or C-D, work together as a pair. Two inputs are used to supply an ‘Even’– A,C and ‘Odd’– B,D input signal for each Ck clock.

2.8 DDC Double Rate Complex Input

The GC5016 can process one double rate complex input. The double rate mode requires a special mode called Split IQ. In this mode two DDC channels, A-B or C-D, work together as a pair. The even time complex samples are A-I and B-Q. The odd time complex samples are C-I and D-Q.

3 GC5016 DDC Output Bus Configuration

The DDC output modes are used to output real, interleaved complex, parallel complex, or time-division multiplexed complex data from the GC5016.

The DDC output bus timing is based on several conditions. The output pins 4, 8, or 16, a frame strobe, and a channel clock are provided for each of four ports.

The channel clock has control register values that invert the clock output. (ckp_A, ckp_B, ckp_C, ckp_D). The frame strobe is active for one channel clock at the start of an output cycle. The clock-to-output and output-hold timing are measured with the Ck clock as a reference.

The channel clock can be divided by the sck_div register value. The channel clock can be 1:1 to 1:16 based on the sck_div value of 0 to 15.

The DDC output bus and input bus selection are related to the use of the GC5016 in DDC mode:

- Real Output – in the special case where the DDC is used as a FIR filter, each channel has a real parallel output.

- Parallel Complex Output – in the split IQ mode, when two DDC channels are used together, the I and Q data can be output in parallel. Each I or Q output is an A,C-I, or B,D-Q.
- Interleaved Complex Output – each of the DDC outputs has separate pins which can be used to output interleaved IQ data for the connected channel.
- Time Division Multiplexed (TDM) Complex Output – combines all the DDC channels at the output port. All channels must be at a common decimation to use this feature. The channel output order is reversed to D, C, B, and A.

DDC Output Mode	Pseudo-Command Variables	Register Variables
Real, Parallel Complex	routf_tdm = 0	routf_iqmux = 0
Interleaved Complex	routf_tdm = 0	routf_iqmux = 1
TDM Complex	routf_tdm = 1	routf_iqmux = 0

3.1 DDC Output Channel Clock and Data Framing Options

The DDC output can be connected with a variety of pins and bits. This is used to transfer the desired DDC output to the receiver logic. The DDC channel has 20-bit resolution. The DDC can have rounding applied that provides for 4, 8, 12, 16, or 20 bits of resolution. This is controlled with the 'BITS' pseudo command for the DDC channel.

Each DDC output port has 16 pins. In cases where the customer wants to minimize the number of IO connections, the number of pins can be reduced. The DDC output can be transferred 4, 8, or 16 pins for each channel output clock. The number of pins that are active is controlled with the 'PINS' pseudo command for the DDC channel. The following table illustrates the combinations of bits, pins, and output cycles:

Output Type	Bits	Pins	Number of Channel Clocks Per Output Cycle
Real, Parallel IQ	20	16	2
	16	16	1
	20	8	3
	16-12	8	2
	8	8	1
	20	4	5
	16	4	4
	12	4	3
	8	4	2
Interleaved IQ	20	16	4
	16	16	2
	20	8	6
	16-12	8	4
	8	8	2
	20	4	10
	16	4	8
	12	4	6
	8	4	4
TDM IQ (Split IQ)	20	16	8
	16	16	4
	20	8	12
	16-12	8	8
	8	8	4
	20	4	20
	16	4	16
	12	4	12
	8	4	8

Output Type	Bits	Pins	Number of Channel Clocks Per Output Cycle
TDM IQ	20 16 20 16-12 8 20 16 12 8	16 16 8 8 8 4 4 4 4	16 8 24 16 8 40 32 24 16

Each DDC output has a start-of-frame signal and a divided channel clock. The frame strobe signal (AFS, BFS, CFS, DFS) is the start of the output frame signal. It is asserted for one divided channel.

The divided clock period is controlled by the 'sck_div' register control for each channel. Each divided channel clock also has a clock polarity control. If clock-inversion is used, the positive edge of the inverted channel divided clock can be used to sample the DDC output data in the external device.

3.2 Real or Parallel Complex DDC Output – (See Figure 8 and Figure 9)

The DDC output for each channel has a 4-, 8-, or 16-pin interface. The DDC output bits can be 4, 8, 12, 16, or 20. The data-output width matches the channel divided clock period. The engineering selection of pin, bits, sck_div, cic_dec, and fir_dec must be considered in generating an output.

Figure 8 shows the timing diagram. Figure 9 shows the logic output connections. The pseudo-variable, 'routf_tdm' is set to 0. The register variable 'routf_iqmux' is also set to 0.

The frame strobe repeats every (cic_dec * fir_dec) Ck clocks. The frame strobe sub-frame-data can occur in (cic_dec * fir_dec) / (sck_div + 1) sub frames.

The real mode output can have independent decimations for each channel. The parallel complex output must have the same decimation for the pair (A,B) (C,D) of channels.

The following real or parallel complex DDC output table lists the number of sub-frames required to output the 'n' bits of DDC output data:

Bits	Pins	scl_div	Number of sub_frames	Number of Ck Clocks
4	4	1	1	2
8	8			
16	16			
8	4	1	2	4
12, 16	8			
20	16			
12	4	1	3	6
20	8			
16	4	1	4	8
20	4	1	5	10

The number of Ck clocks needed to transmit the output must be less than the fir_dec * cic_dec.

3.3 Interleaved Complex DDC Output – (See Figure 10–Figure 13)

The DDC output for each channel has a 4-, 8-, or 16-pin interface. The DDC output bits can be 4, 8, 12, 16, or 20. The data-output width matches the channel divided clock period.

The engineering selection of pin, bits, sck_div, cic_dec, and fir_dec must be considered in generating an output.

Figure 10 shows the timing diagram. Figure 11–Figure 13 show the logic output connections.

The frame strobe repeats every (cic_dec * fir_dec) Ck clocks. The frame strobe sub-frame-data can occur in (cic_dec * fir_dec) / (sck_div + 1) sub frames.

The interleaved complex output has the I and Q data on the same output pin interface:

Bits	Pins	scl_div	Number of sub_frames	Number of Ck Clocks
4	4	1	2	4
8	8			
16	16			
8	4	1	4	8
12, 16	8			
20	16			
12	4	1	6	12
20	8			
16	4	1	8	16
20	4	1	10	20

The number of Ck clocks needed to transmit the output must be less than the channel decimation (fir_dec * cic_dec).

Note: A special format for the 16-bit interface can provide both the current gain and 8 bits of I and Q data. See Table 2 in the GC5016 data sheet.

3.4 Time Division Multiplexed DDC Output – (See Figure 14 and Figure 15)

The Time Division Multiplexed (TDM) DDC output mode uses the least number of output pins to transmit the IQ data from the DDC channels. The restriction in using this mode is the minimum decimation, and that all channels have to be at the same decimation.

The TDM mode uses the D output pin interface.

There are two sub-modes, related to using four-channel or split IQ two-channel mode:

4-channel, (output format) DI, DQ, CI, CQ, BI, BQ, AI, AQ

Split IQ (output format) BQ(D), BI(C), AQ(B), AI(A)

Note: A special format for the 16-bit interface can provide both the current gain and 8 bits of I and Q data. See Table 2 in the GC5016 data sheet.

The 4-channel output format interface needs the following clocks per frame (i.e., minimum decimation)

Bits	Pins	scl_div	Number of sub_frames	Number of Ck Clocks
4	4	0	8	8
8	8			
16	16			
8	4	0	16	16
12, 16	8			
20	16			
12	4	0	24	24
20	8			
16	4	0	32	32
20	4	0	40	40

Note: The channel clock divide is set to 0. If the sck_div = 1, the number of Ck clocks doubles.

The split IQ output format interface needs the following clocks per frame (i.e., minimum decimation).

Bits	Pins	scl_div	Number of sub_frames	Number of Ck Clocks
4	4	0	4	4
8	8			
16	16			
8	4	0	8	8
12, 16	8			
20	16			
12	4	0	12	12
20	8			
16	4	0	16	16
20	4	0	20	20

Note: The channel clock divide is set to 0. If the sck_div = 1, the number of Ck clocks doubles.

4 GC5016 DUC Input Bus Configuration

The GC5016 DUC input provides the low speed input interface from the external logic.

The DUC provides a frame strobe signal that is used to indicate when the next complex or real input is needed. The frame strobe period after initialization should match the overall interpolation (fir_int * cic_int).

4.1 Real or Parallel Complex DUC Input – (See Figure 16, Figure 17, Figure 18 and Figure 19)

The real or parallel complex DUC input is used to transfer real or complex data in parallel to the GC5016.

The DUC input timing is based on the Ck clock Tsetup and Thold. The customer logic uses the channel frame strobe (nFS) and channel clock (nCk) to determine when the next I and Q data are to be transmitted. The 1-> 0 transition of the frame strobe (non-inverted output) corresponds with the tinf_fs_dly = 0 time to receive the data. The tinf_fs_dly value can be adjusted to cause the zero reference time to be delayed in channel clocks. Increasing the tinf_fs_dly value causes the sampling of the DUC input to be delayed by ‘value’ channel clocks.

The DUC input can be operated in several modes. Some of the modes are dependent on the channel operating mode:

- Real – If the DUC is used as an interpolating FIR filter, the DUC input corresponds to the FIR filter input. The frame strobe signal and divided channel clock are used to output signals from the GC5016 requesting the next real input. Each of the DUC channels can operate independently.
- Parallel Complex (Split IQ) – If the DUC is used in the split IQ mode, the A-B, and C-D pairs of channels have I and Q inputs. The frame strobe signal and divided channel clock are used to request the next complex input. The A,B and C,D pairs of channels need to be the same settings for the DUC split IQ mode.
- Parallel Complex (8-bit) – Each of the DUC channels has an 8-bit I and Q interface over the 16-pin interface. The frame strobe signal and divided channel clock are used to request the next complex input. Each of the DUC channels can operate independently.
- Interleaved Complex IQ – Each of the DUC channels can operate with an interleaved I then Q interface over the channel DUC input. The frame strobe signal and divided channel clock are used to request the next complex input. Each of the DUC channels can operate independently.
- TDM Complex – The A input port is used to synchronously transfer data to the active DUC input channels. The TDM mode can support both split IQ and four-channel mode. The active DUC channels

must be at a common interpolation rate for this to work properly.

Table 1. DUC Input Configuration Items

Description	Splitiq	tinf_tdm	tinf_cmplx	tinf_iqmux	tinf_pariq
4-channel TDM mode	0	1	1	0	0
4-channel interleaved IQ	0	0	1	1	0
4-channel parallel IQ > 8-bit real	0	0	0	0	0
2-channel parallel IQ > 8-bit real	1	0	0	0	0
2-channel TDM	1	1	0	0	0
2-channel parallel IQ > 8-bit parallel, parallel complex (split IQ)	1	0	1	0	0

4.2 Sck_div, fir_int, cic_int inputs to CMD5016

The sck_div is used to determine the divided channel clock period.

Channel divided clock period = Ck period * (1 + sck_div)

The fir_int and cic_int are used to determine the interpolation ratio for this DUC channel.

Interpolation_ratio = (fir_int * cic_int)

4.3 Synchronizing the DUC Input to the External Logic

The DUC channels need complex or real input data every (fir_int * cic_int) clocks. The frame strobe signal from the GC5016 signifies that the next input is required. The frame strobe is output one divided clock before the input data is required (i.e., the 1->0 transition of the frame strobe and corresponding Ck clock identify reference time tinf_fs_dly = 0). See Figure 16.

The frame strobe repeats every (fir_int * cic_int) after initialization. The frame strobe signal width and data received width are based on the divided channel clock.

Using an example of interpolate by 24, and sck_div = 1, there are 12 divided channel clocks in each DUC input frame. The real and parallel complex input modes require one divided channel clock for input. The interleaved complex (IQ) input mode requires two divided channel clocks for input. The TDM Split IQ mode requires four divided channel clocks for input

4.4 PINS and BITS Interfacing

Each DUC channel has a 20-bit complex input bus. Each DUC channel has a 16-pin input interface. The DUC input mode has user selection to optimize the logic interface, reducing the number of input pins utilized depending on the overall interpolation and desired IO clock rate. This interface is similar to the DDC output interface in functions.

Note: The selected input mode, real, parallel IQ (8-bit), and interleaved IQ can be configured for different interpolation ratios between channels. The split IQ, parallel IQ, and TDM modes have restrictions that require the paired channel (split IQ) to have the same interpolation ratio. If the TDM input mode is used, all channels must have the same interpolation ratio. The interpolation ratio must be equal to or greater than the number of Ck clocks required for the desired DUC input mode.

DUC Input Mode	Bits	Pins	sck_div	Number of sub_frames	Number of Ck clocks
Real, 8-bit parallel IQ or split IQ parallel complex	4 8 16	4 8 16	1	1	2
	8 12, 16 20	4 8 16	1	2	4

DUC Input Mode	Bits	Pins	sck_div	Number of sub_frames	Number of Ck clocks
	12 20	4 8	1	3	6
	16	4	1	4	8
	20	4	1	5	10
Interleaved IQ	4 8 16	4 8 16	1	2	4
	8 12, 16 20	4 8 16	1	4	8
	12 20	4 8	1	6	12
	16	4	1	8	16
	20	4	1	10	20
TDM complex – split IQ	4 8 16	4 8 16	1	4	8
	8 12, 16 20	4 8 16	1	8	16
	12 20	4 8	1	12	24
	16	4	1	16	32
	20	4	1	20	40
TDM complex – 4-channel	4 8 16	4 8 16	1	8	16
	8 12, 16 2	4 8 16	1	16	32
	12 20	4 8	1	24	48
	16	4	1	32	64
	20	4	1	40	80

The DUC input is 2s complement. The 8-bit I and Q input has 2s complement for each value.

4.5 Frame Strobe

The frame strobe signal is used to signal when the GC5016 needs the next input sample

The user-adjusted tinf_fs_dly and the frame strobe determine when the DUC input is sampled for the next interpolation set of clocks. Figure 17 shows the timing diagram.

Figure 18 shows the data connections for the single port real or two-port parallel complex inputs. This connection is used for wideband complex inputs where split IQ mode is used. In this configuration, the I data goes to port A or C, while the Q data goes to port B or D.

Figure 19 shows another version where a single port parallel complex is split into eight bits of I and eight bits of Q. This is typically used for independent channel interpolation, where eight bits of I and Q resolution are acceptable.

4.6 Interleaved IQ Complex DUC Input – (Figure 20, Figure 21, Figure 22, and Figure 23)

The DUC input for interleaved IQ complex data allows each DUC channel to have separate interpolation ratios. The DUC input uses the channel divided clock (ACK, BCK, CCK, DCK) and frame strobe (AFS, BFS, CFS, DFS) to identify that the next IQ sample is needed.

The timing diagram in Figure 20 shows the I and Q data separately transmitted depending on the pins and bits interface.

There are three choices of pin and four choices of bits. The DUC input has 20 bits of resolution. The table above shows the 4-, 8-, 16-pin and 4-, 8-, 12-, 16-, and 20-bit sub-frames, as more clock cycles are needed to input the data. If more sub-frames are needed, the minimum interpolation ratio is higher.

In a four channel application, all four sets of DUC input pins are used. The selection is to use 4, 8, or 16 input pins. Figure 21 shows the connection for the 16-bit IQ input mode. Figure 22 and Figure 23 show the connections for the 8-bit and 4-bit IQ input modes.

4.7 TDM IQ Complex DUC Input – (Figure 24 and Figure 25)

The DUC input TDM mode can be used in the four-channel or split IQ modes. The data is received on the A DUC input pins. Figure 24 shows the timing diagram. The four-channel mode has eight time slots for input data, based on the frame strobe synchronization. This sets the minimum interpolation ratio to 8. The sub-frame data order is:

IA, QA, IB, QB, IC, QC, ID, QD

The split IQ mode can also use the TDM DUC input mode. The minimum interpolation ratio is 4. The sub-frame data order is:

IA, QA(B), IB(C), QB(D)

The divided channel clock is used to identify one specific sub-frame. The frame strobe, similar to other DUC modes, occurs once every (cic_int * fir_int) interpolation count.

Figure 25 shows the 16-bit connection of the TDM input to the GC5016. There are options of 8-pin and 4-pin input interfaces.

5 GC5016 DUC Output Bus Configuration

The GC5016 has four DUC output ports when the sum input option is not used. In the sum input mode, the C and D outputs are used as inputs.

The output timing for the DUC output bus is based on the clock-to-output and output-hold time. The reference for these time delays is the Ck input clock.

The DUC output ports active are based on the output mode (real, interleaved complex, parallel complex, double rate real, double rate complex, and sum input):

Output type – sum input not used (tout_sumin = 0)	tout_ rate	tout_ res	tout_ nsig	tout_ cmplx
Real output- full rate-16 bits, Separate outputs	1	0	4	0
Real output- full rate-16 bits, A+B->A, C+D->B	1	0	2	0
Real output- full rate-16 bits, A+B+C+D->A	1	0	1	0
Real output- full rate-22 bits, A+B->AB; C+D->CD	1	1	2	0
Real output- full rate-22 bits, A+B+C+D->AB	1	1	1	0
Real output double rate – 16 bits; AB->AB; CD->CD	2	0	2	0
Real output double rate – 22 bits; AB+CD->AB	2	1	1	0
Interleaved IQ – half rate – 16 bits, Separate outputs	0	0	4	1
Interleaved IQ – half rate – 16 bits, A+B->A, C+D->B	0	0	2	1
Interleaved IQ – half rate – 16 bits, A+B+C+D->A	0	0	1	1
Interleaved IQ – half rate – 22 bits, A+B->AB; C+D->CD	0	1	2	1
Interleaved IQ – half rate – 22 bits, A+B+C+D->AB	0	1	1	1
Parallel IQ output – full rate – 16 bits, AB->AB, CD->CD	1	0	2	1
Parallel IQ output – full rate – 16 bits, A+C, B+D->AB	1	0	1	1
Parallel IQ output – full rate – 22 bits, A+C, B+D->ABCD	1	1	1	1
Parallel IQ output – double rate – 16 bits, AB+CD->ABCD	2	0	1	1

The GC5016 DUC outputs have an IFLG signal used with interleaved complex mode to identify the I output cycle. The user controlled output decimation function is not used in the interleaved complex output mode.

The GC5016 has several output modes using the ports individually or in combination:

5.1 DUC Real Output

The DUC real output has a 16- or 22-bit output mode. The 16-bit output mode utilizes one 16-pin output port. The 22-bit output mode utilizes two output ports. The DUC real output mode can use the output-hold function to provide output decimation. Figure 25 shows the 16-bit real output block diagram. Figure 26 illustrates the DUC digital output timing.

The output can have 12-, 14-, 16-, or 22-bit rounding. The MSB of the output port is always connected to the MSB of the digital input device. The variables that control the DUC output rounding are toutf_rnd_AB, and toutf_rnd_CD.

The Ck clock is used as the clock reference for the output. The Clock-to-output delay and hold-output delay are used to determine the proper timing with the next digital device.

Figure 27 shows the configuration for the 22-bit real output. In this case the B and D output ports have the lower 6 bits of the 22-bit output. The A and C ports have the upper 16 bits of the 22-bit real output.

5.2 DUC Double Rate Real Output

A special mode can be used to output DUC data at 2x the Clock (Ck) rate. This is called double rate. The double rate mode outputs an even and an odd sample at the Ck rate. 16- and 22-bit resolution can be used in this configuration. The 16-bit double rate occurs in that the A,C ports output the even data, and the B,D ports output the odd time data. The double rate 16-bit real mode is shown in Figure 28. The double rate 22-bit real mode is shown in Figure 29.

Note: The output timing for the double rate real modes is identical to the real output shown in Figure 26 .

5.3 DUC Interleaved IQ Output

The four GC5016 output ports can be used with a 1/2 rate complex output. In this case, the interpolation occurs from the symbol input to the clock rate and the output is decimated by 2 in the output logic.

Since the I and Q outputs are interleaved onto a single set of output pins, there is a signal called IFLG that identifies when the I signal is output.

The interleaved IQ output mode can use four ports with 16-bit resolution, or two ports with 22-bit resolution. The output can have 12-, 14-, 16-, or 22-bit rounding.

Figure 30 shows the timing diagram of the interleaved IQ output. Figure 25 shows the four-port output configuration (with the added IFLG) at 16-bit resolution.

Figure 27 shows the two-port output configuration (with the added IFLG) at 22-bit resolution.

5.4 DUC Parallel Complex Output

The GC5016 can have two parallel full rate complex outputs with 16-bit resolution. The I and Q are output on the I-A,C and Q-B,D ports. The timing is identical to Figure 26.

Figure 31 shows the two port output configuration.

The output bit resolution can be extended to 22 bits. The 22-bit parallel complex configuration is shown in Figure 32.

5.5 DUC Parallel Complex Double Rate Output

The 16-bit parallel complex can also be used at double the Ck rate. The one port 16-bit double rate complex configuration is shown in Figure 33. Port AB provides the IQ even output, and port CD provides the IQ odd output.

6 GC5016 DUC Sum Input Bus Configuration

The sum input mode allows for multiple GC5016 DUCs to be used with a set of common output ports. The sum input uses the C and D output ports as input ports:

DUC Output Mode	C_Output Port	D_Output Port
Real – full rate 16 bits	Real 16-bit input	Not used
Real – full rate 22 bits	Top 16 of 22 real inputs	Bottom 6 of 22 real inputs
Real – double rate 16 bits	Even real	Odd real
Parallel IQ – full fate 16 bits	I 16-bit input	Q 16-bit input

The DUC output variables that can be used with the sum input bus are shown in the next table. Both GC5016s must be configured to output the same type of data in order to have the sum bus combine the external sum A (C output as an input) and internal sum A. The sum bus also combines the external sum B (D output as an input) and internal sum B.

Output type – sum input not used (tout_sumin = 1)	tout_ rate	tout_ res	tout_ nsig	tout_ cmplx
Real output – full rate – 16 bits, A+B+SumInA->A, C+D+SumInB->B	1	0	2	0
Real output – full rate – 16 bits, A+B+C+D+SumInA->A	1	0	1	0
Real output - full rate – 22 bits, A+B+C+D+SumInAB->AB	1	1	1	0
Real output double rate – 16 bits; AB+CD+SumInAB->AB	2	0	1	0
Interleaved IQ – half rate – 16 bits, A+B+SumInA; C+D+SumInB	0	0	2	1
Interleaved IQ – half rate – 16 bits, A+B+C+D+SumInA->A	0	0	1	1
Interleaved IQ – half rate – 22 bits, A+B+C+D+SumInAB->AB	0	1	1	1
Parallel IQ output – full rate – 16 bits, AB+CD+SumInAB->AB	1	0	1	1

The GC5016 using the sum input mode cannot use the C and D outputs.

The sum input timing follows the Tsetup and Thold time related to the Ck clock input.

The sum input also has special output considerations since only the A and B output ports are available. The DUC output is identical in diagram to the DUC output section above.

DUC output (A and B only) using sum input bus

(2) 16-bit real outputs

(1) 22-bit real output

(1) 16-bit parallel complex output

A general diagram is shown in Figure 34.

7 Figures

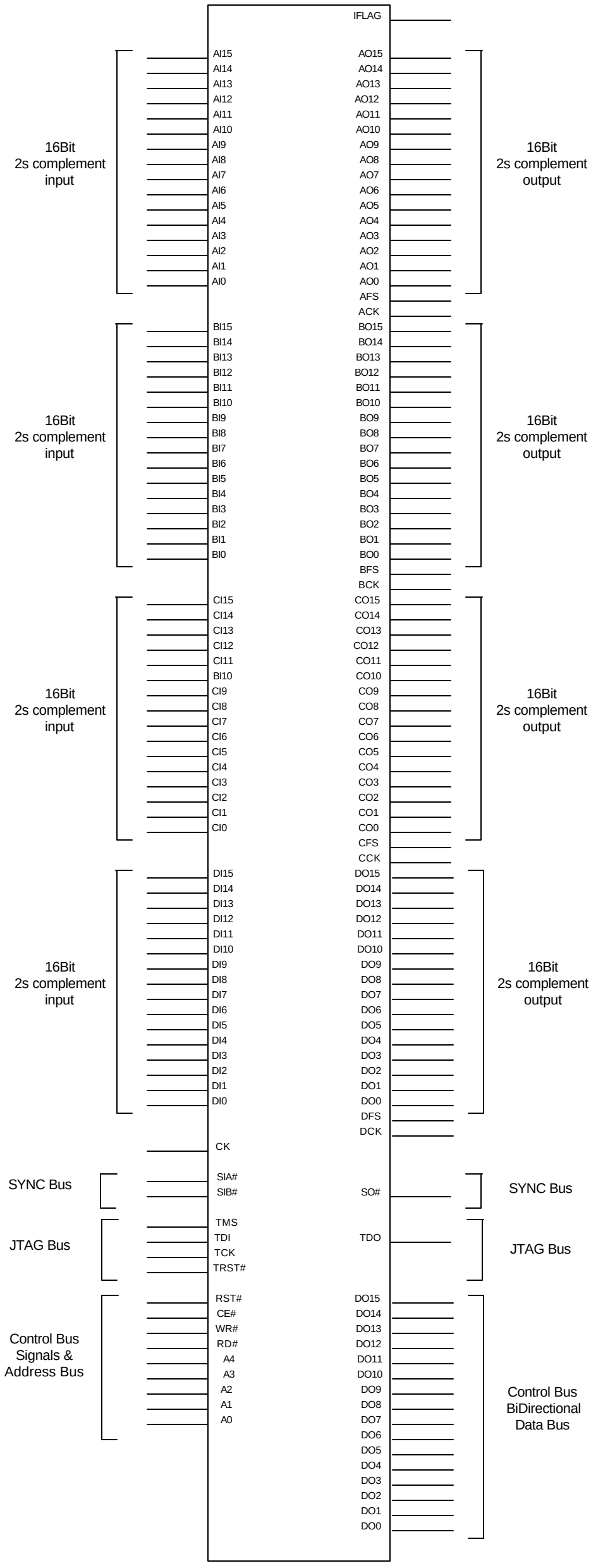


Figure 1. GC5016 Input and Output Buses

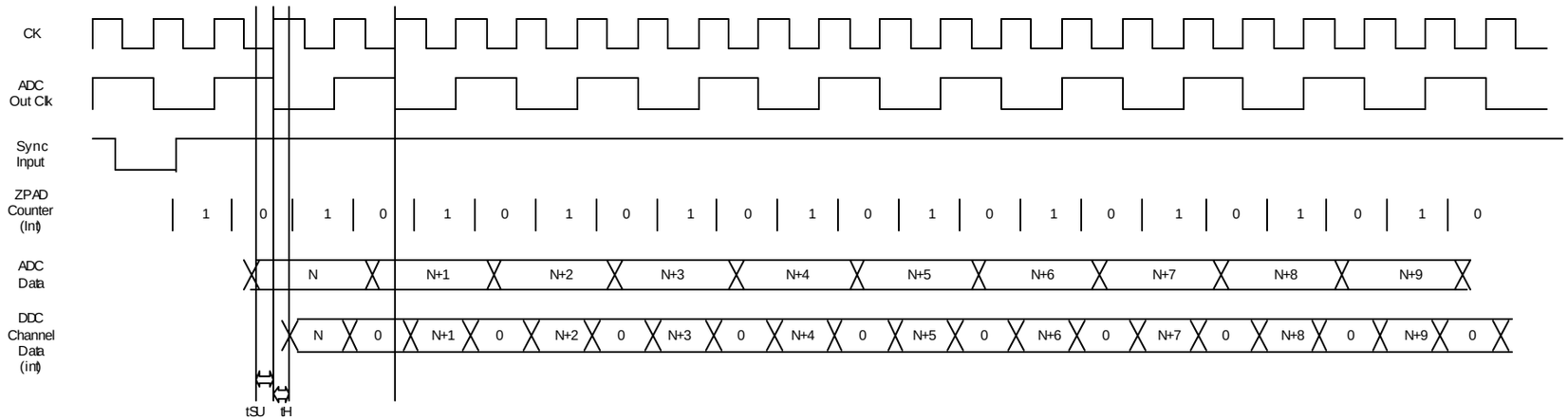


Figure 2. GC5016 DDC Real, Parallel Complex Input Timing (rinf_zpad 1)

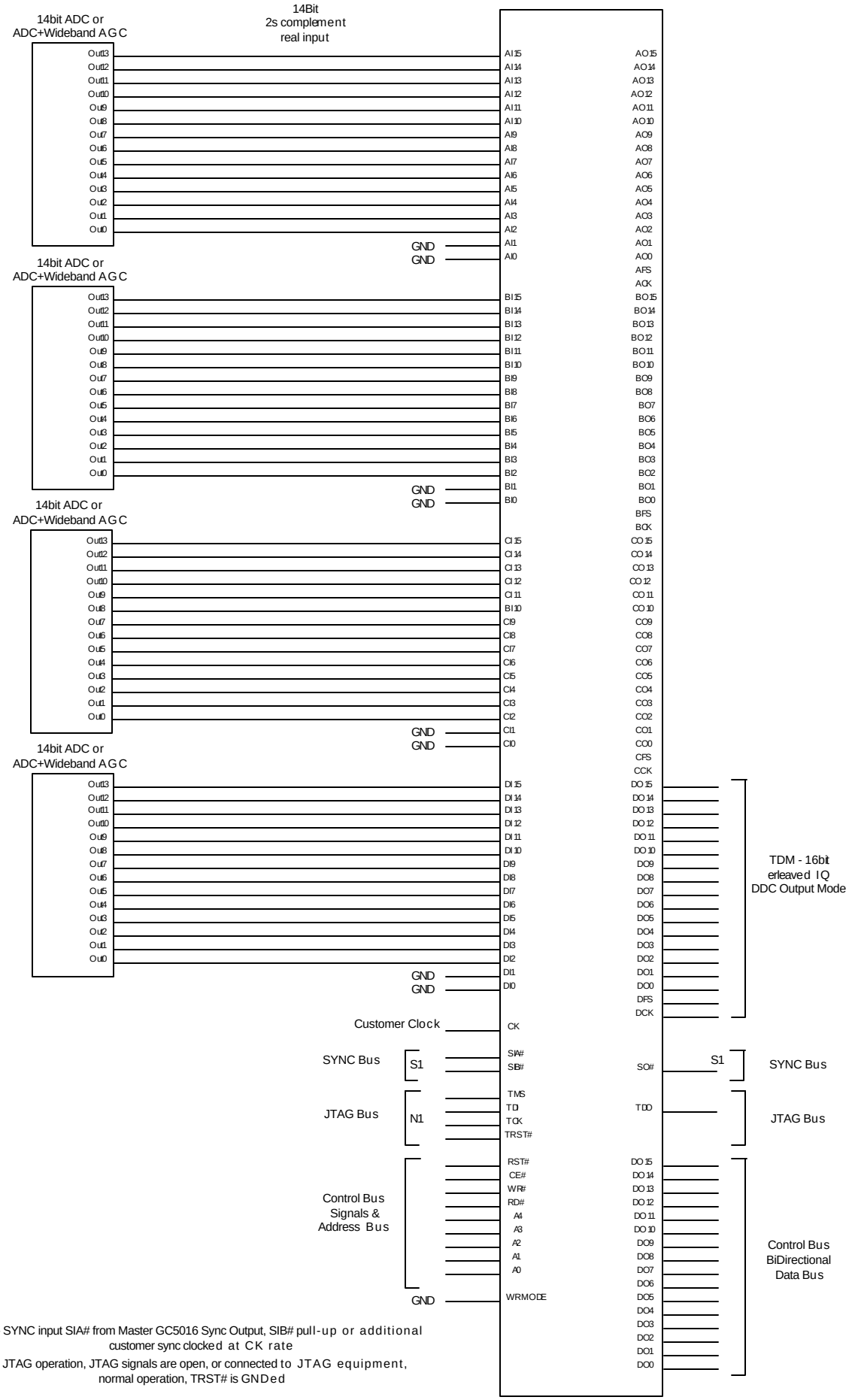


Figure 3. GC5016 DDC Real Input Diagram
Connection to 14bit ADC, Wideband AGC and ADC, TDM IQ All Channel Output

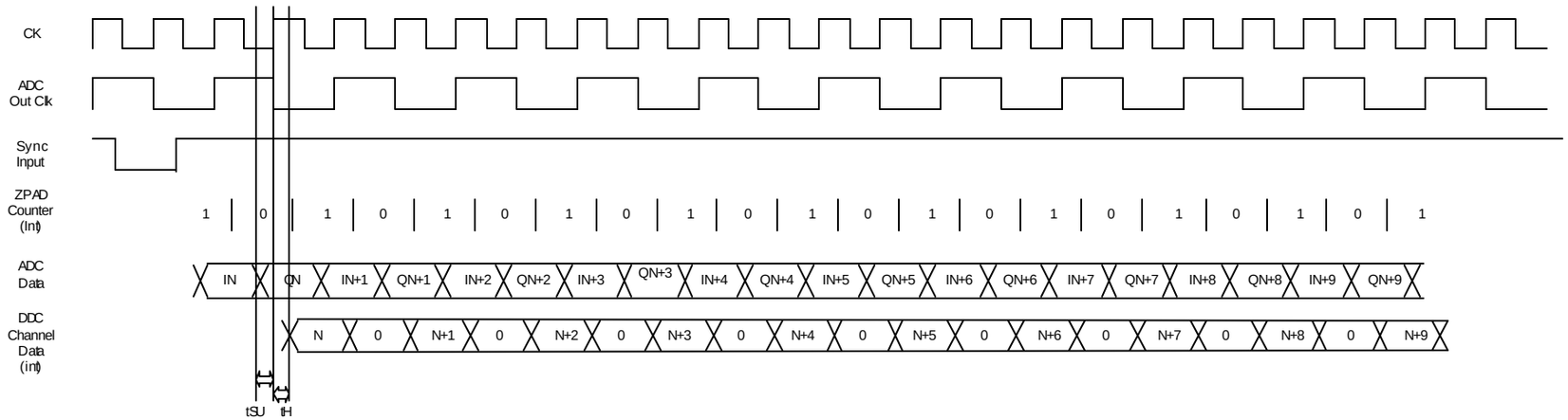


Figure 4. GC5016 DDC Interleaved IQ Input Bus Timing

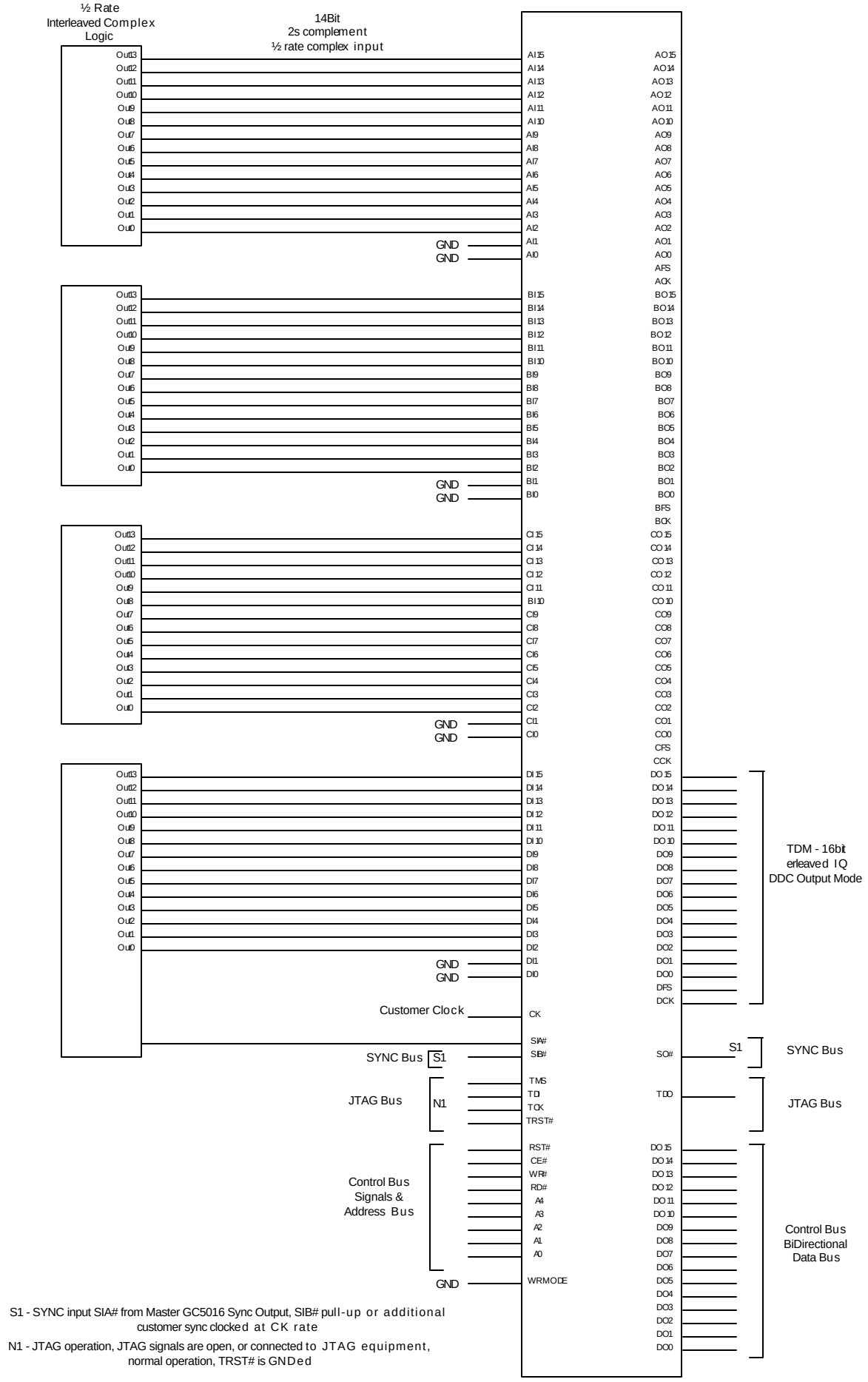


Figure 5. GC5016 DDC Interleaved IQ Input Diagram
Connection to Interleaved IQ Logic, TDM IQ All Channel Output

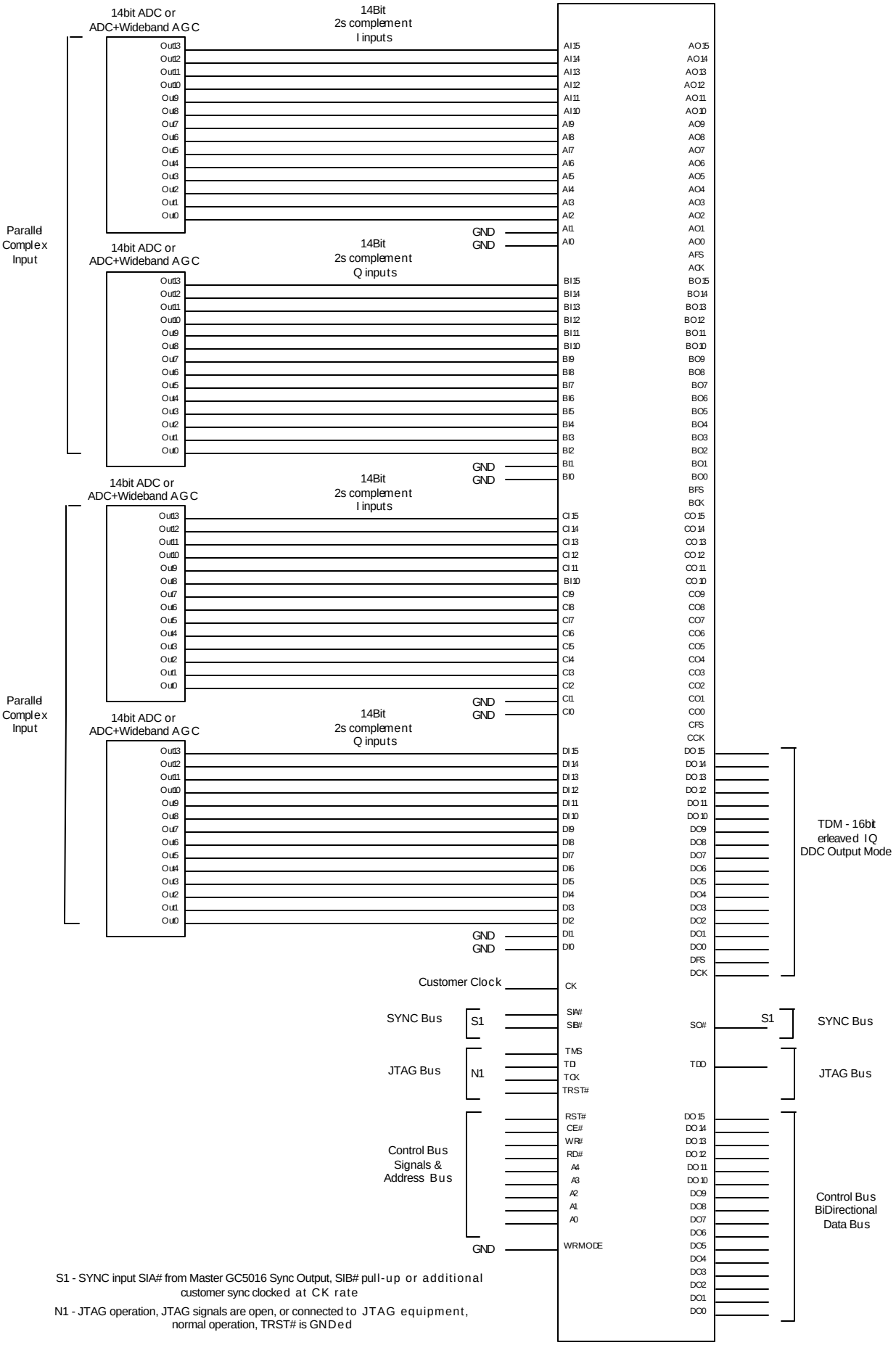


Figure 6. GC5016 DDC Parallel Complex Input Diagram
Connection to Full Complex ADC Inputs, TDM IQ All Channel Output

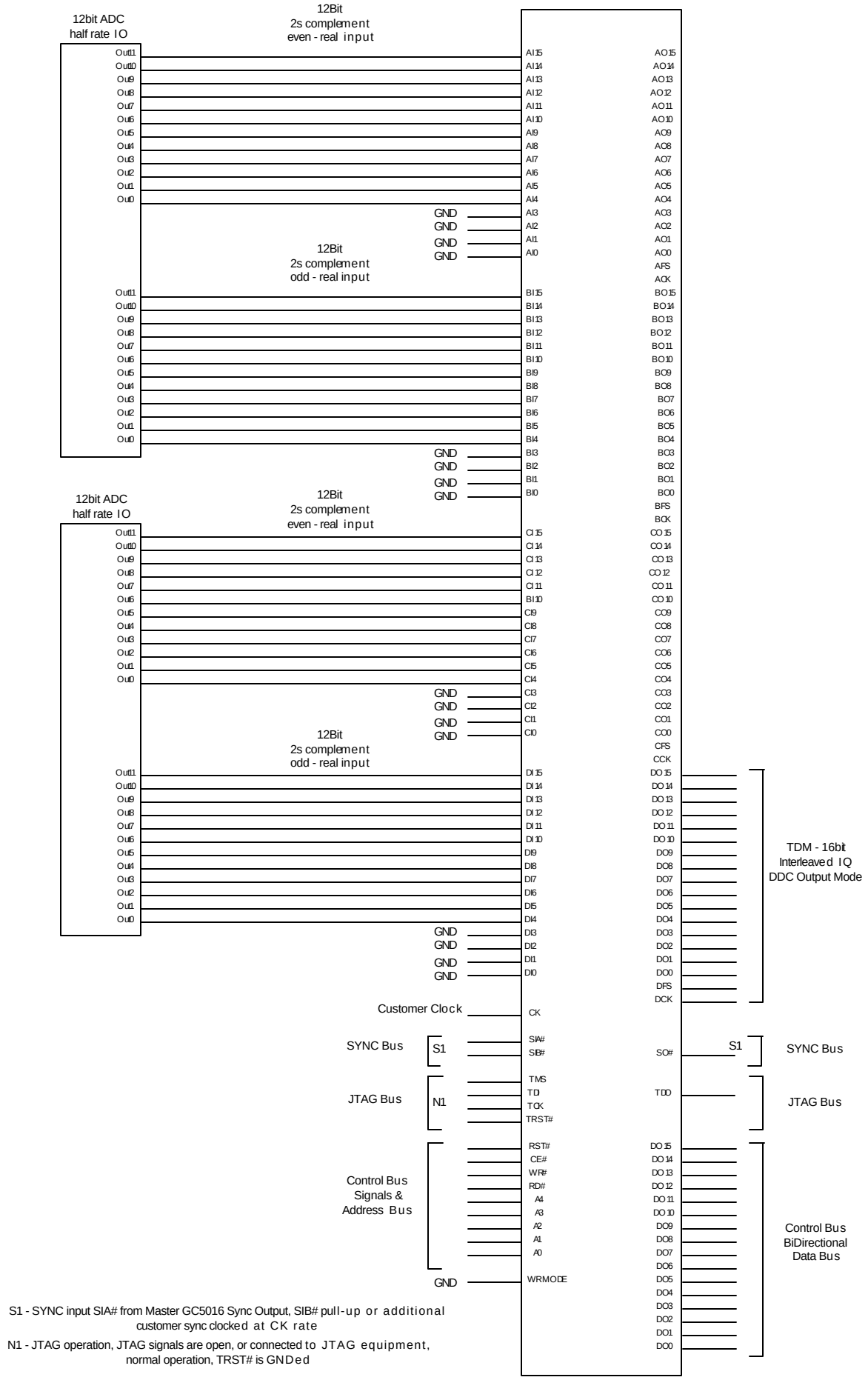


Figure 7. GC5016 Double Rate Real Input Diagram
12-Bit ADC, TDM IQ All Channel Output

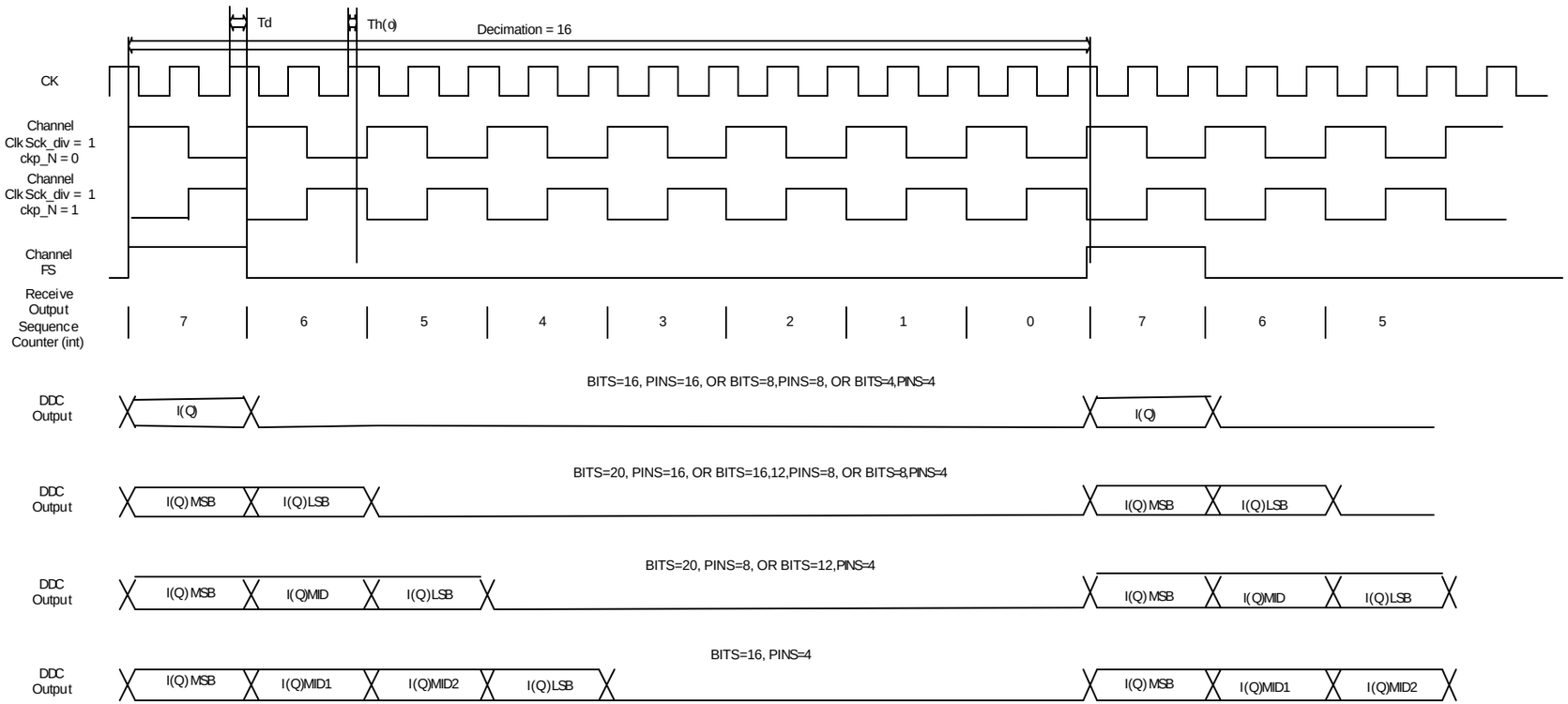


Figure 8. GC5016 DDC Parallel Complex, Real Output Timing

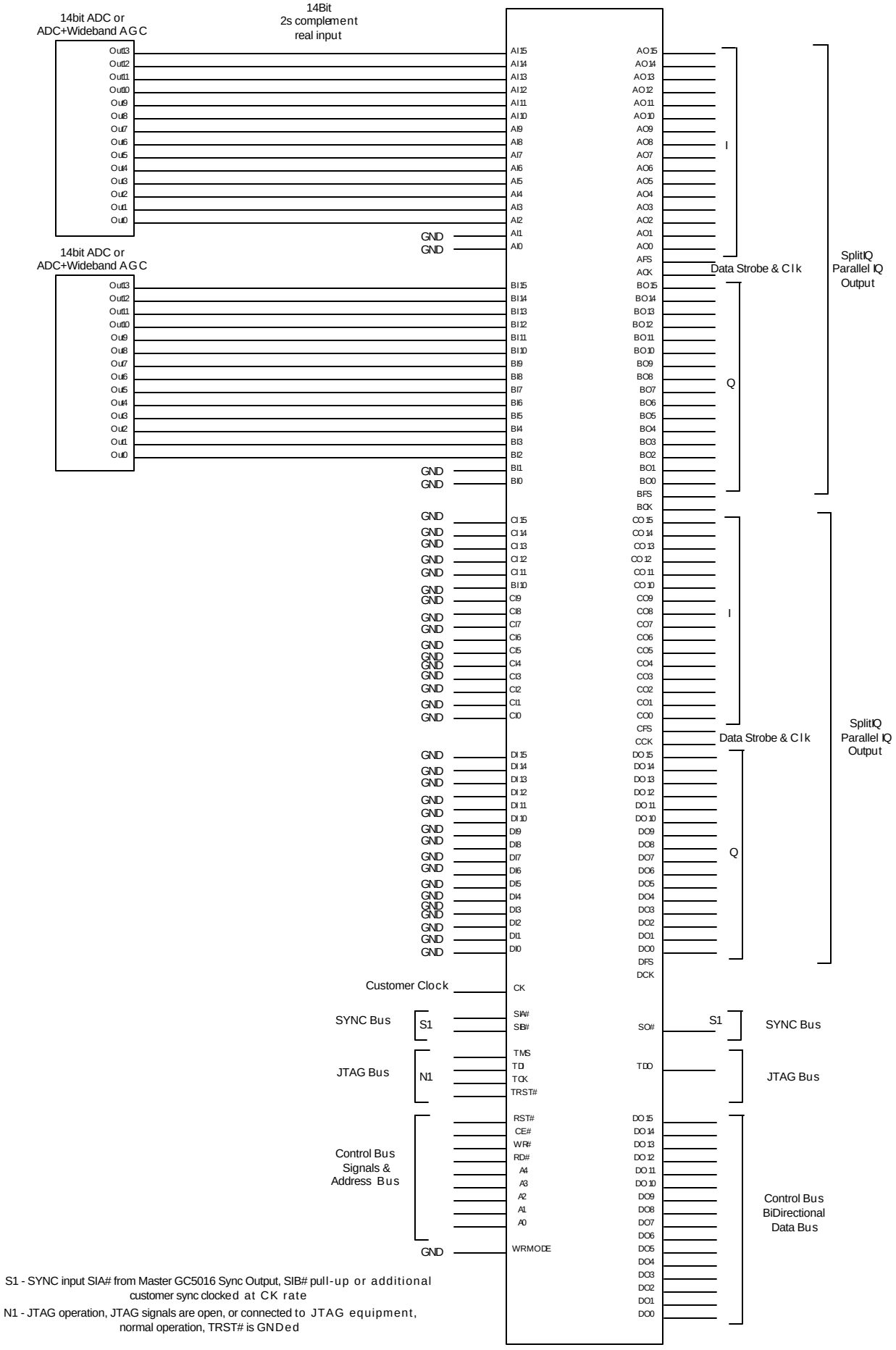


Figure 9. GC5016 DDC Output Parallel Complex Output Diagram
Connection to 14-Bit ADC, Wideband AGC and ADC, 2 Channel SplitIQ Processing, Wideband Output

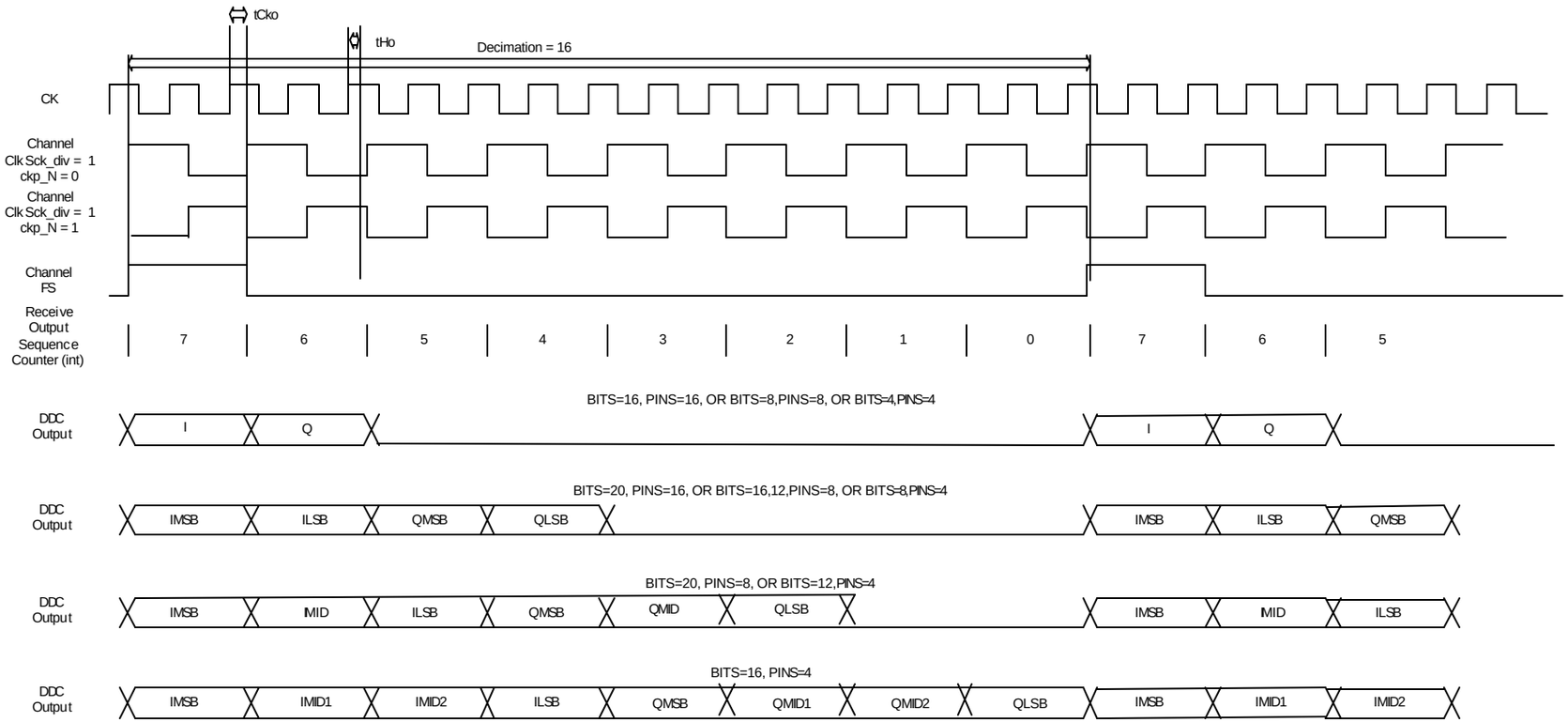


Figure 10. GC5016 DDC Interleaved IQ Output Timing

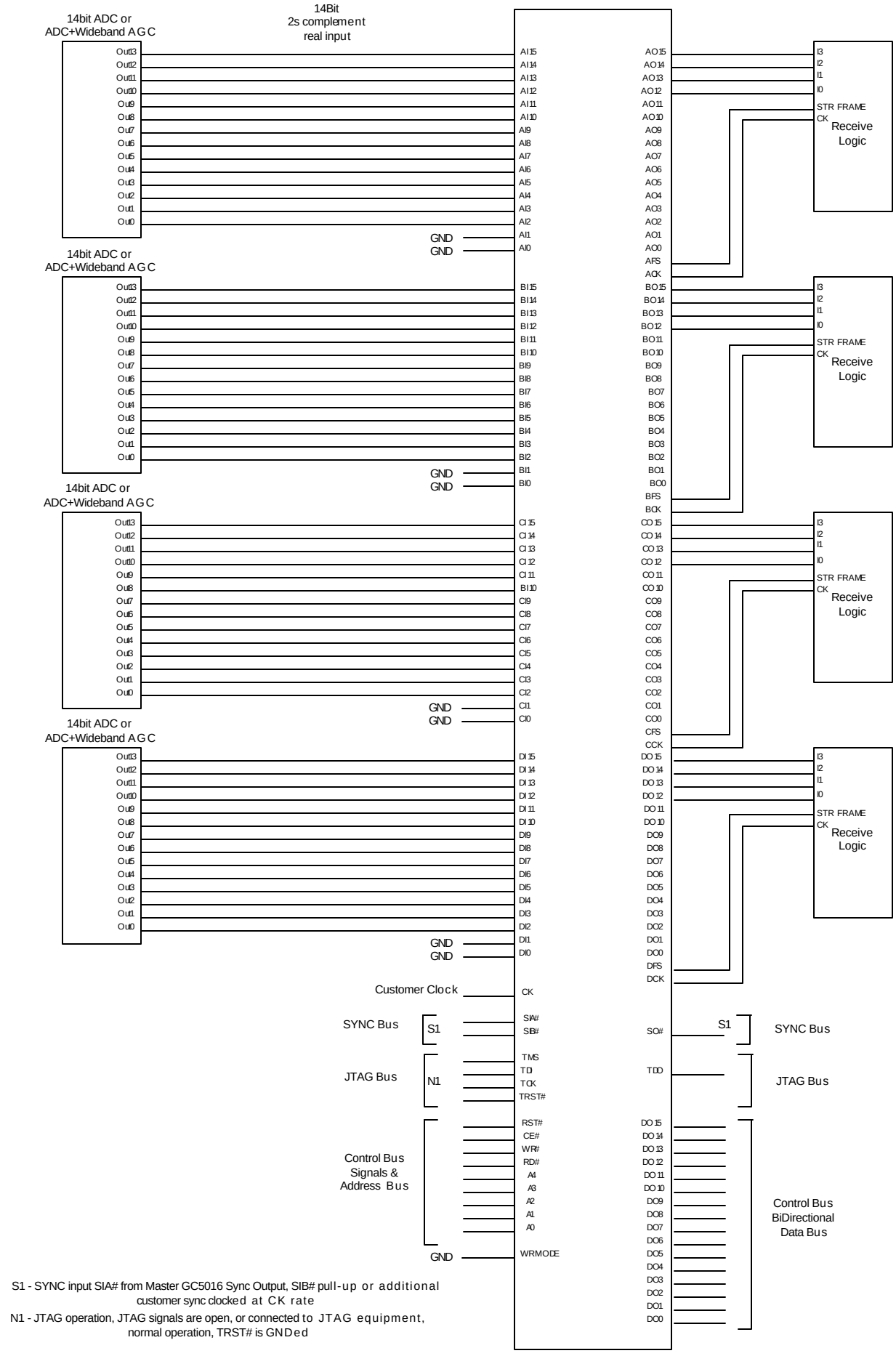


Figure 11. GC5016 DDC Interleaved 4-Pin IQ Output Diagram
Connection to 14bit ADC, Wideband AGC and ADC, 4pin Interleaved IQ Individual Channel Output

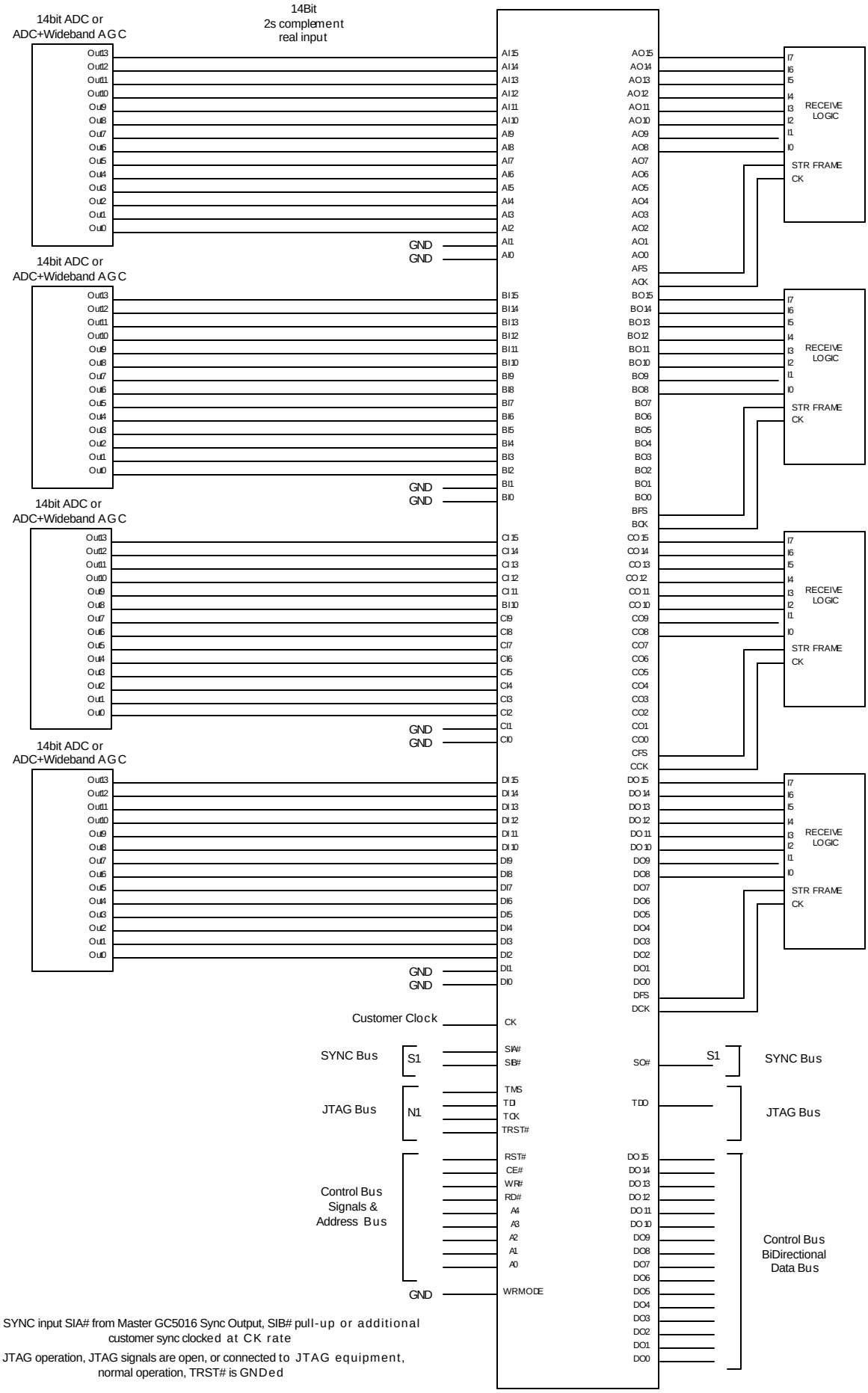
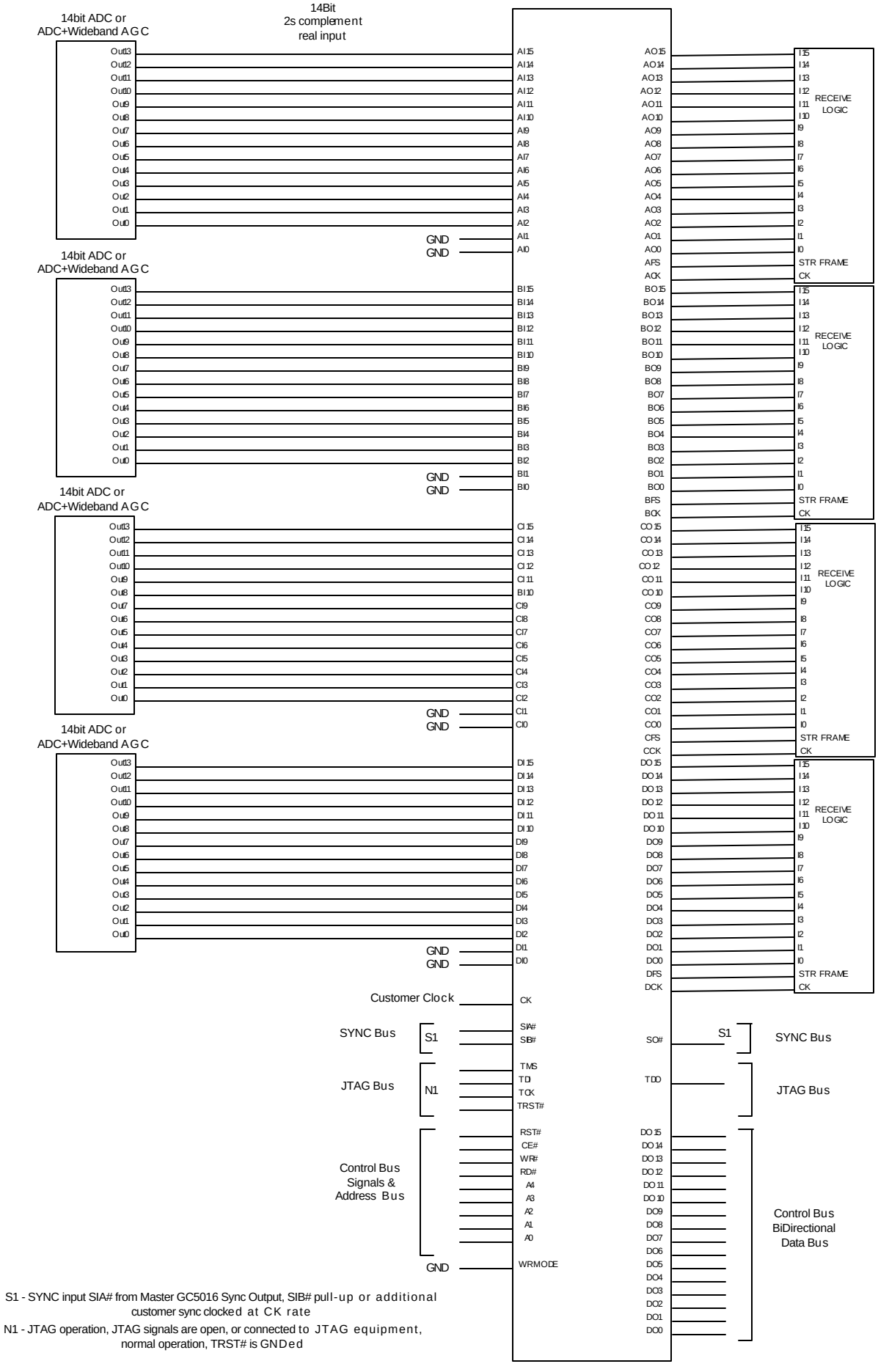


Figure 12. GC5016 DDC Interleaved 8-Pins IQ Output Diagram
Connection to 14bit ADC, Wideband AGC and ADC, 8pin Interleaved IQ Individual Channel Output



S1 - SYNC input SIA# from Master GC5016 Sync Output, SIB# pull-up or additional customer sync clocked at CK rate

N1 - JTAG operation, JTAG signals are open, or connected to JTAG equipment, normal operation, TRST# is GNDed

Figure 13. GC5016 DDC Interleaved 16-Pins IQ Output Diagram
Connection to 14bit ADC, Wideband AGC and ADC, TDM IQ All Channel Output

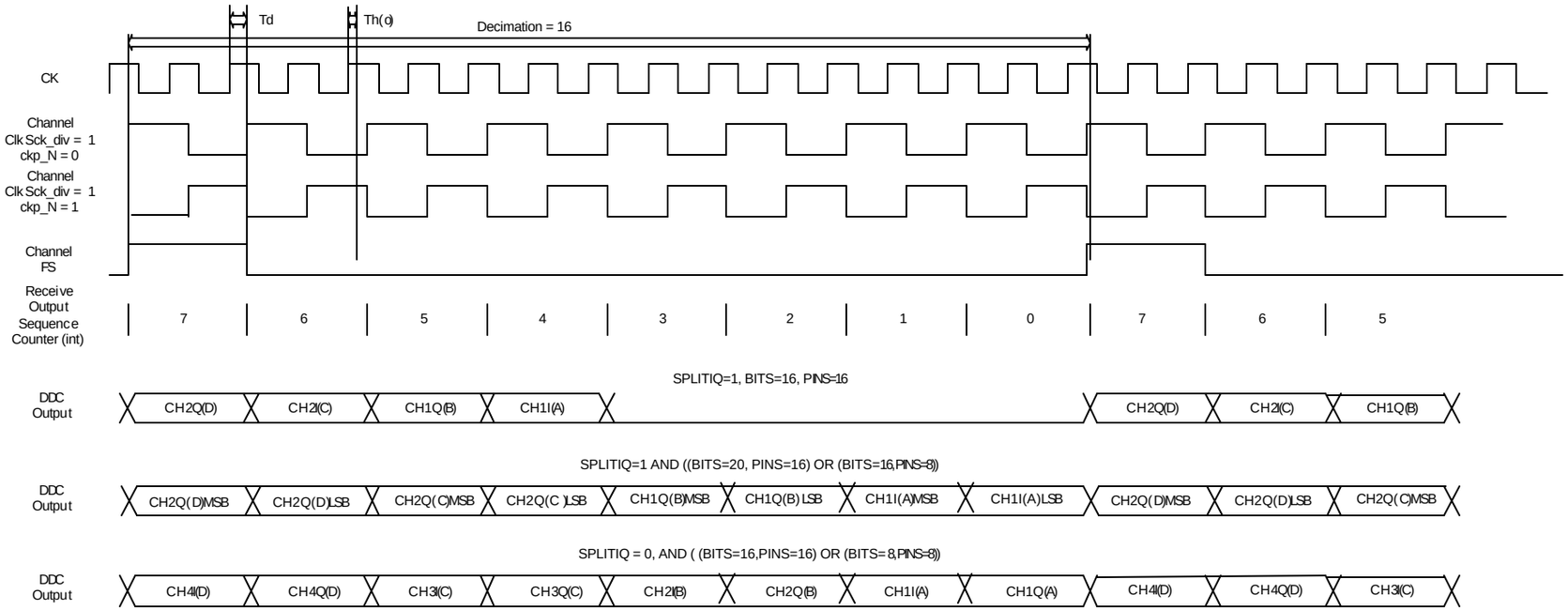


Figure 14. GC5016 DDC TDM Output Timing

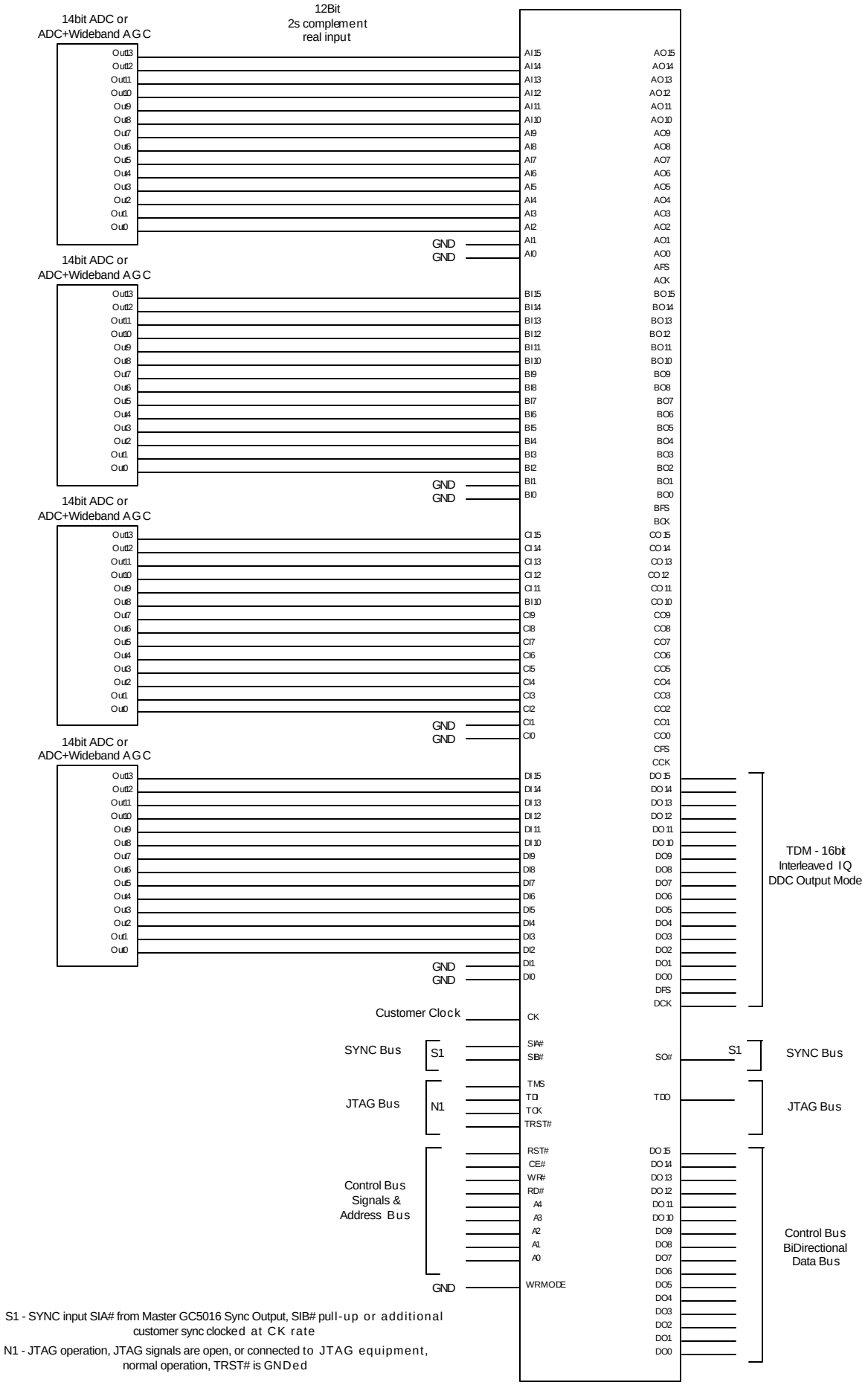


Figure 15. GC5016 DDC TDM Output Bus Diagram
Connection to 14-Bit ADC, Wideband AGC and ADC, TDM IQ All Channel Output

16bits, 16pins, sck_div1, tinf_fs_dly 1

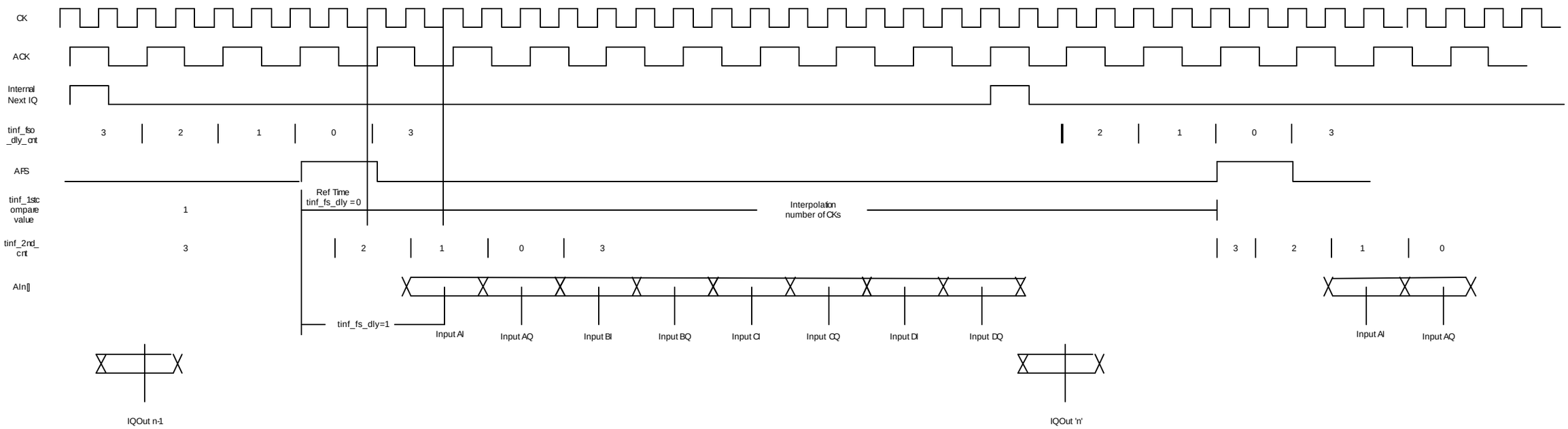


Figure 16. GC5016 DUC Input Bus tinf_fs_dly Timing

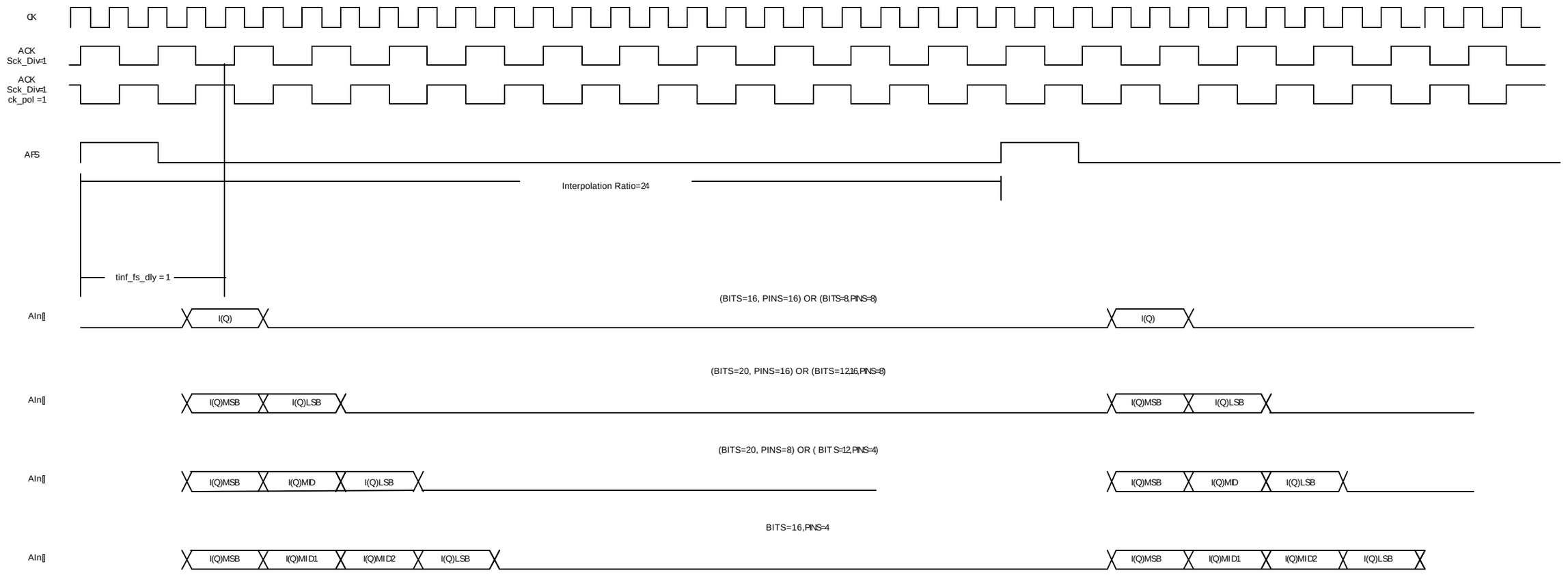


Figure 17. GC5016 DUC Real or Parallel IQ Input Bus Timing (sck_div=1, tinf_fs_dly 1)

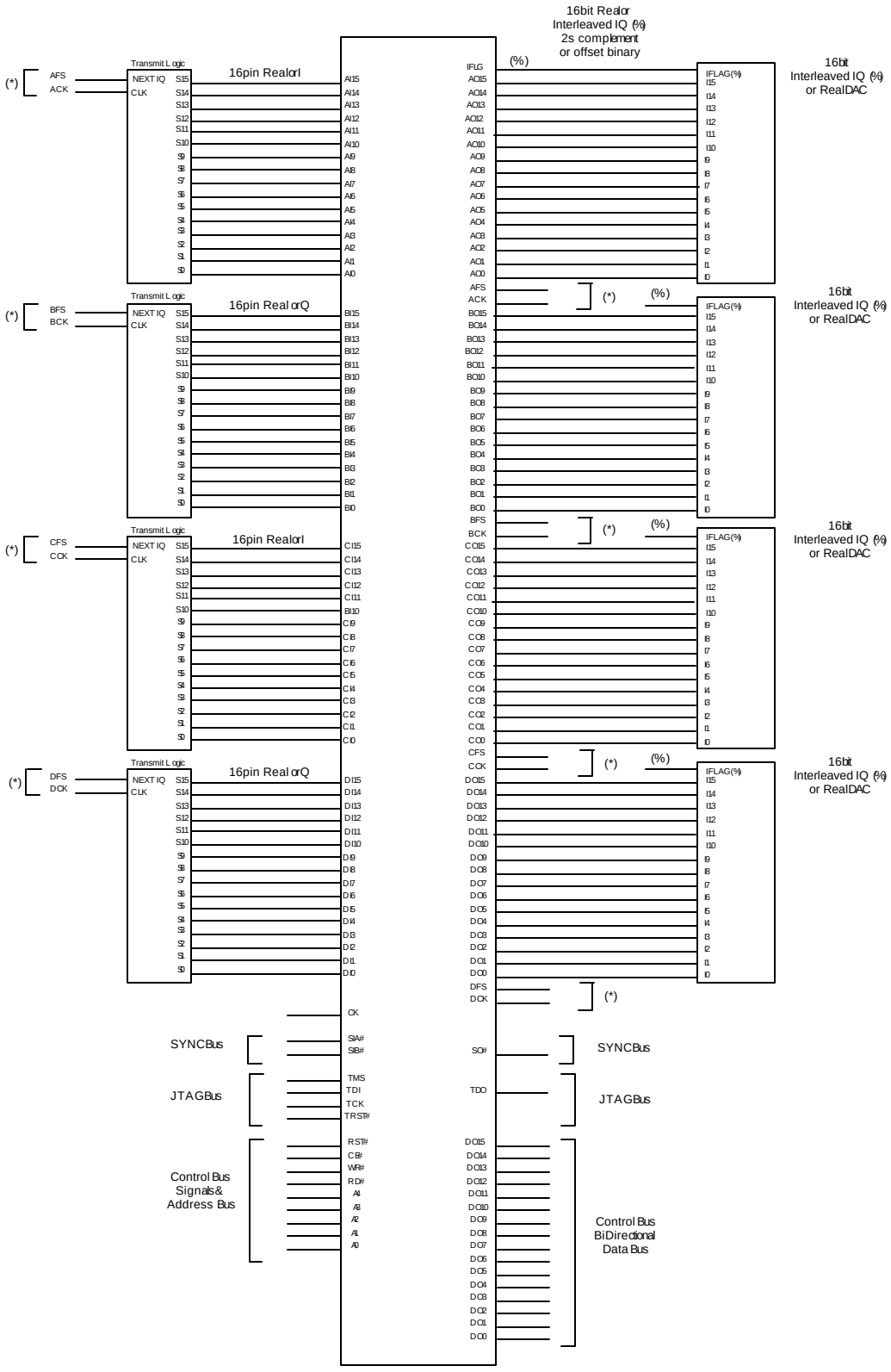


Figure 18. GC5016 DUC Real or SplitIQ-Parallel IQ Input Diagram
16pin Real or SplitIQ, 16bit DAC

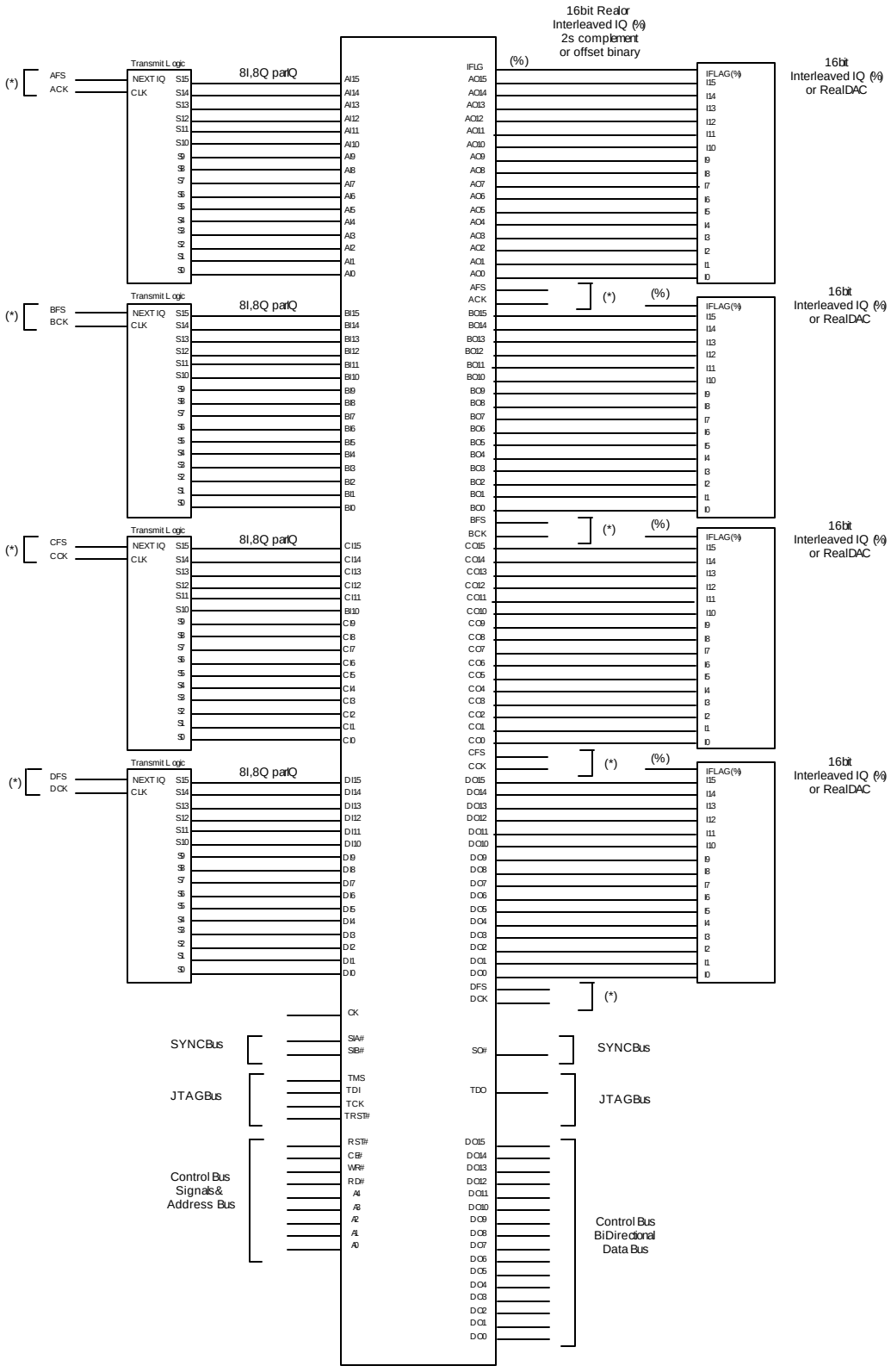


Figure 19. GC5016 DUC Parrallel IQ Input Diagram
16pin ParIQ, 16bit DAC

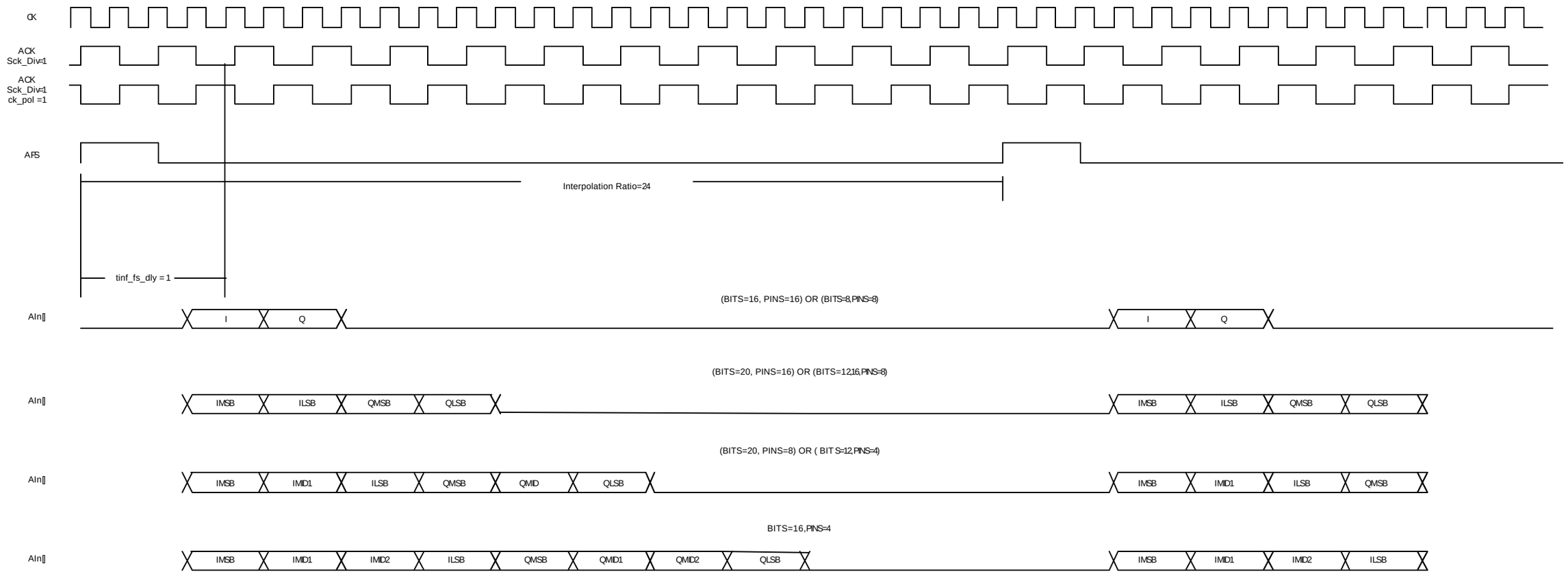


Figure 20. GC5016 DUC Interleaved IQ Timing, sck_div=1, tinf_fs_dly 1

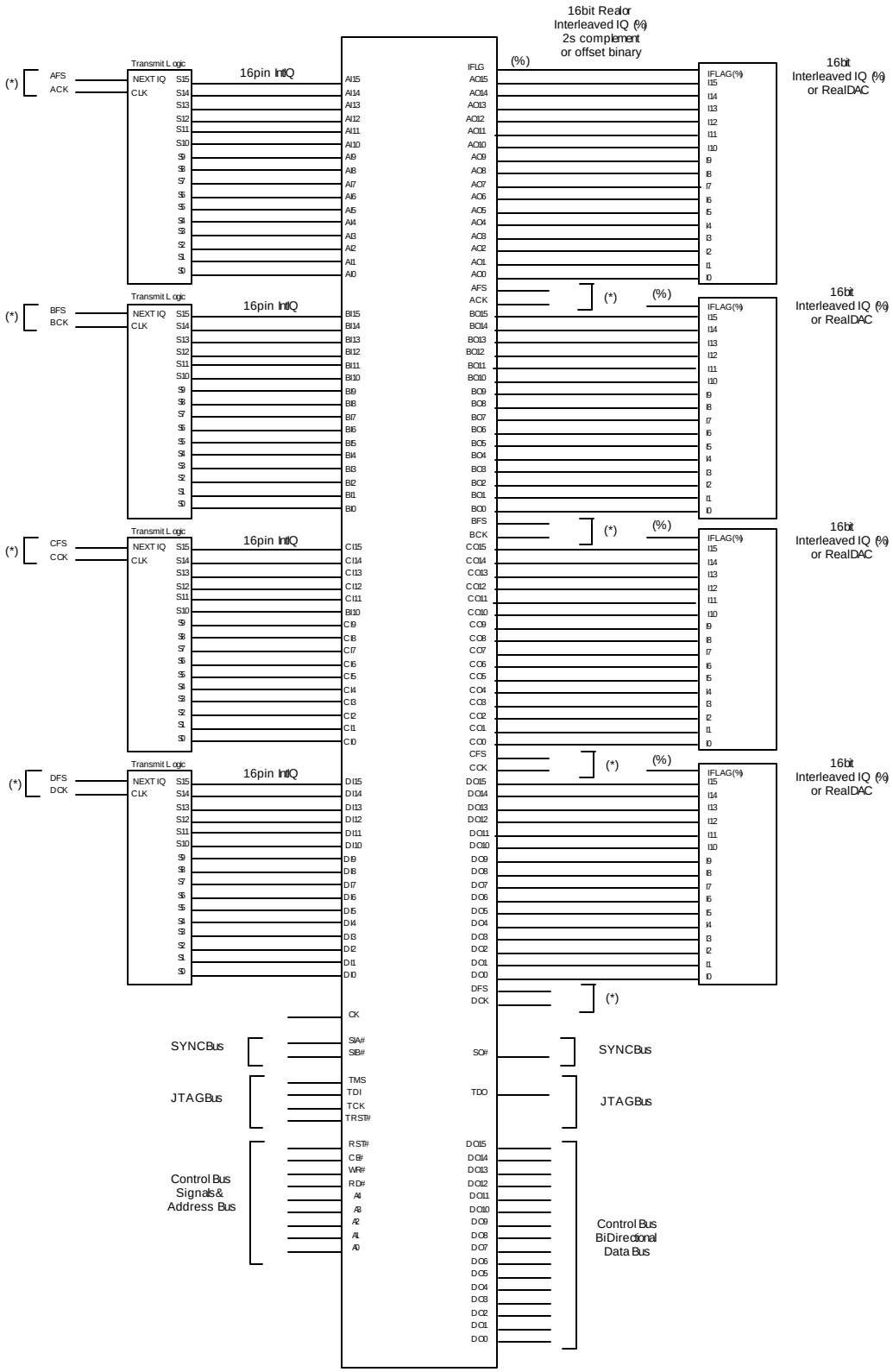


Figure 21. GC5016 DUC Interleaved IQ Input 16-Bit Diagram
16pin IntIQ, 16bit DAC

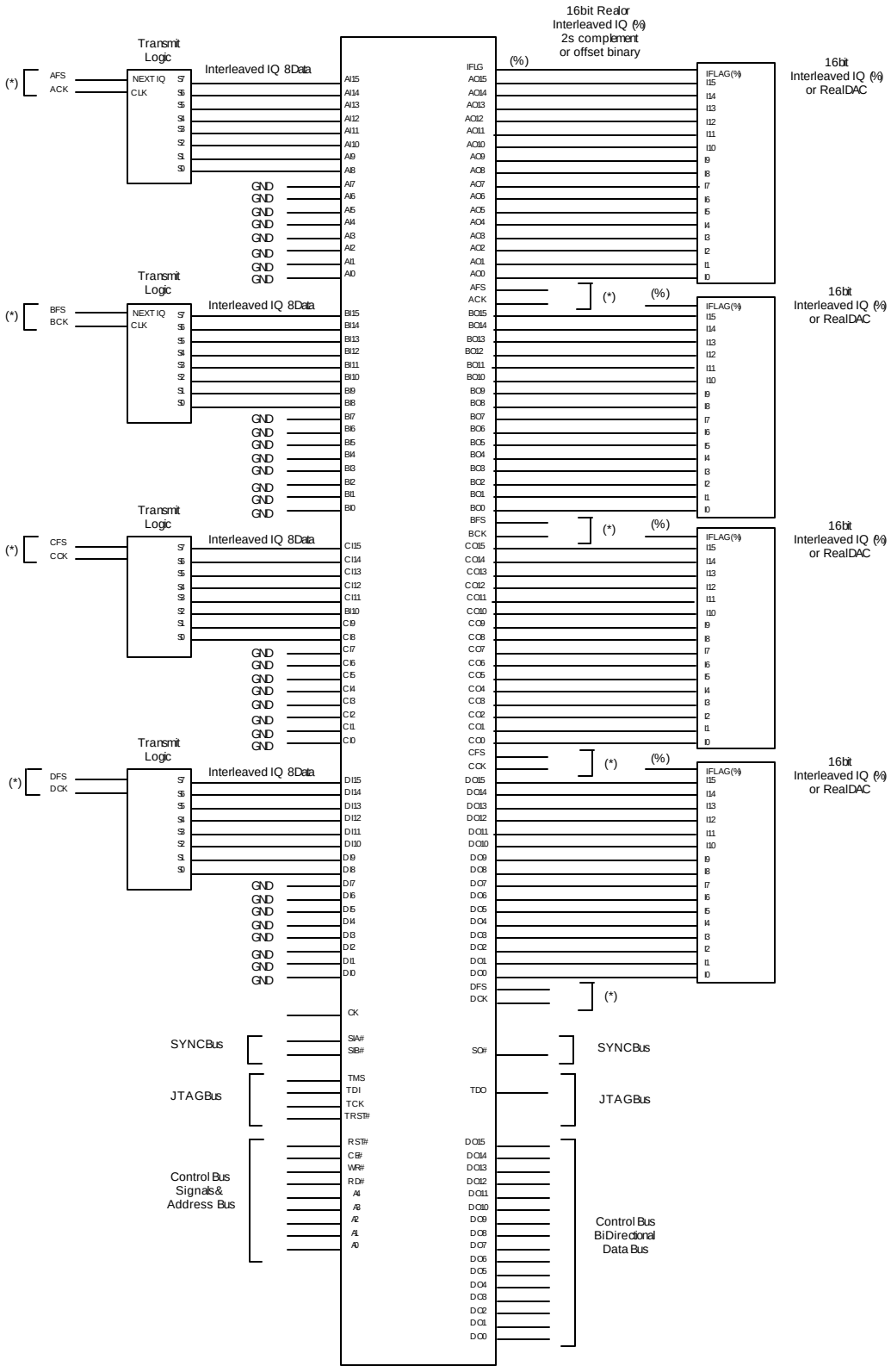


Figure 22. GC5016 DUC Interleaved IQ Input 8-Bit Diagram
8-Pin IntIQ, 16-Bit DAC or Interleaved IQ Interface

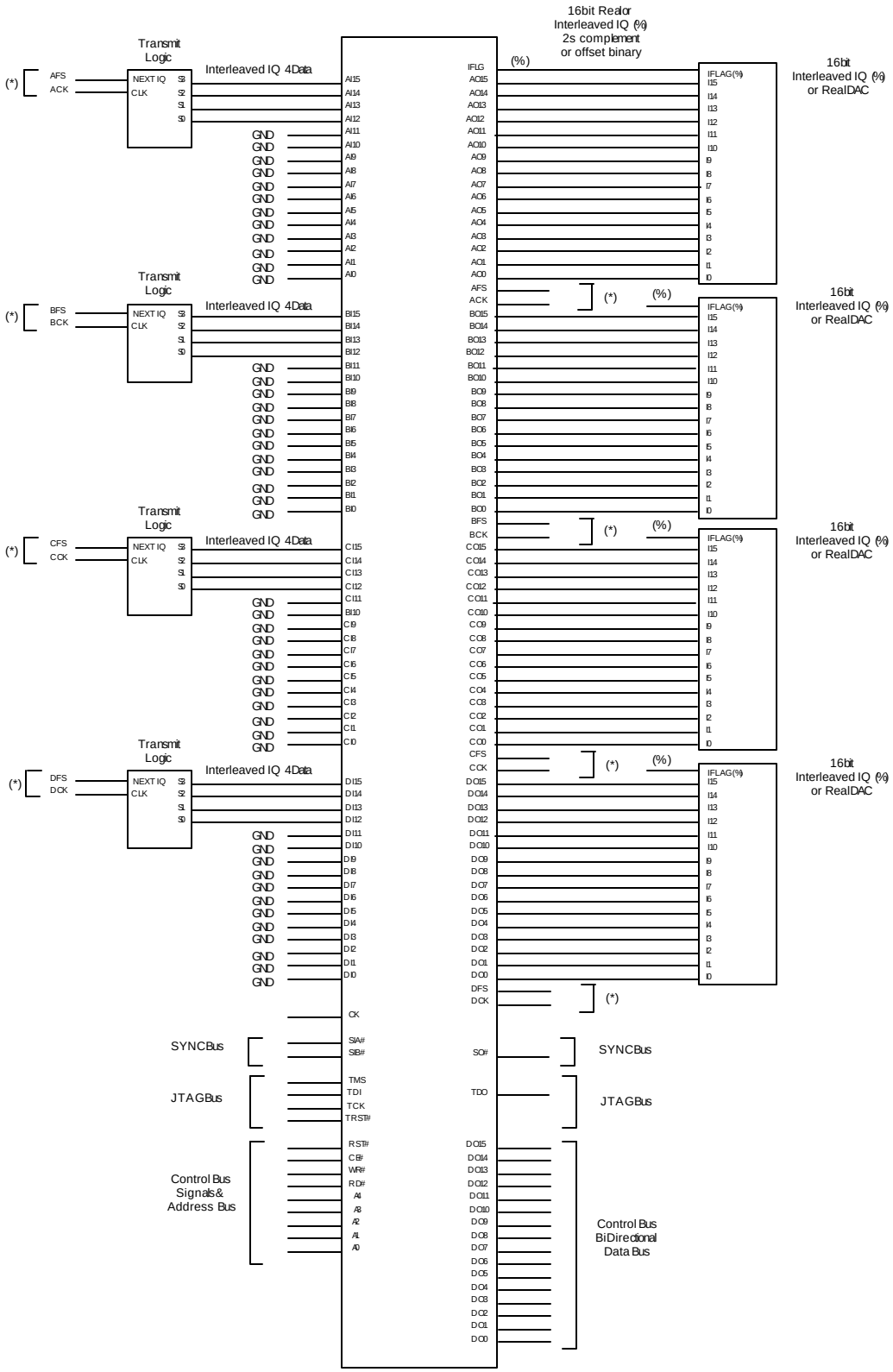


Figure 23. GC5016 DUC Interleaved IQ Input 4-Bit Diagram
4-Pin IntIQ, 16-Bit DAC or Interleaved IQ Interface

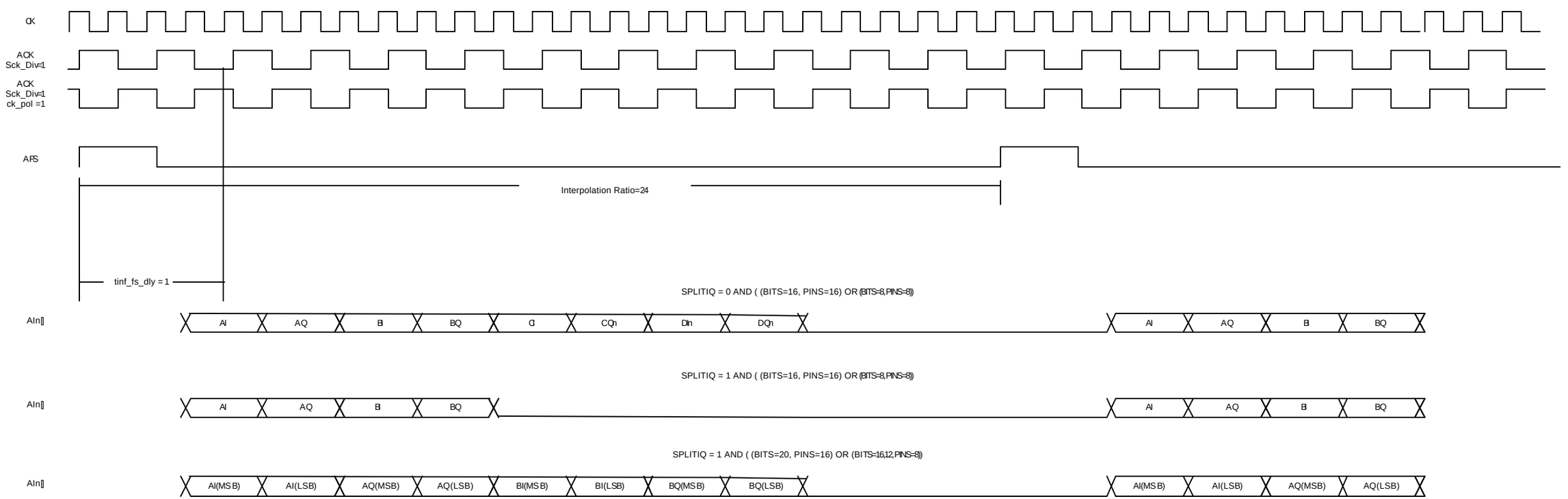


Figure 24. GC5016 DUC TDM IQ Input Timing (sck_div=1, tinf_fs_dly 1)

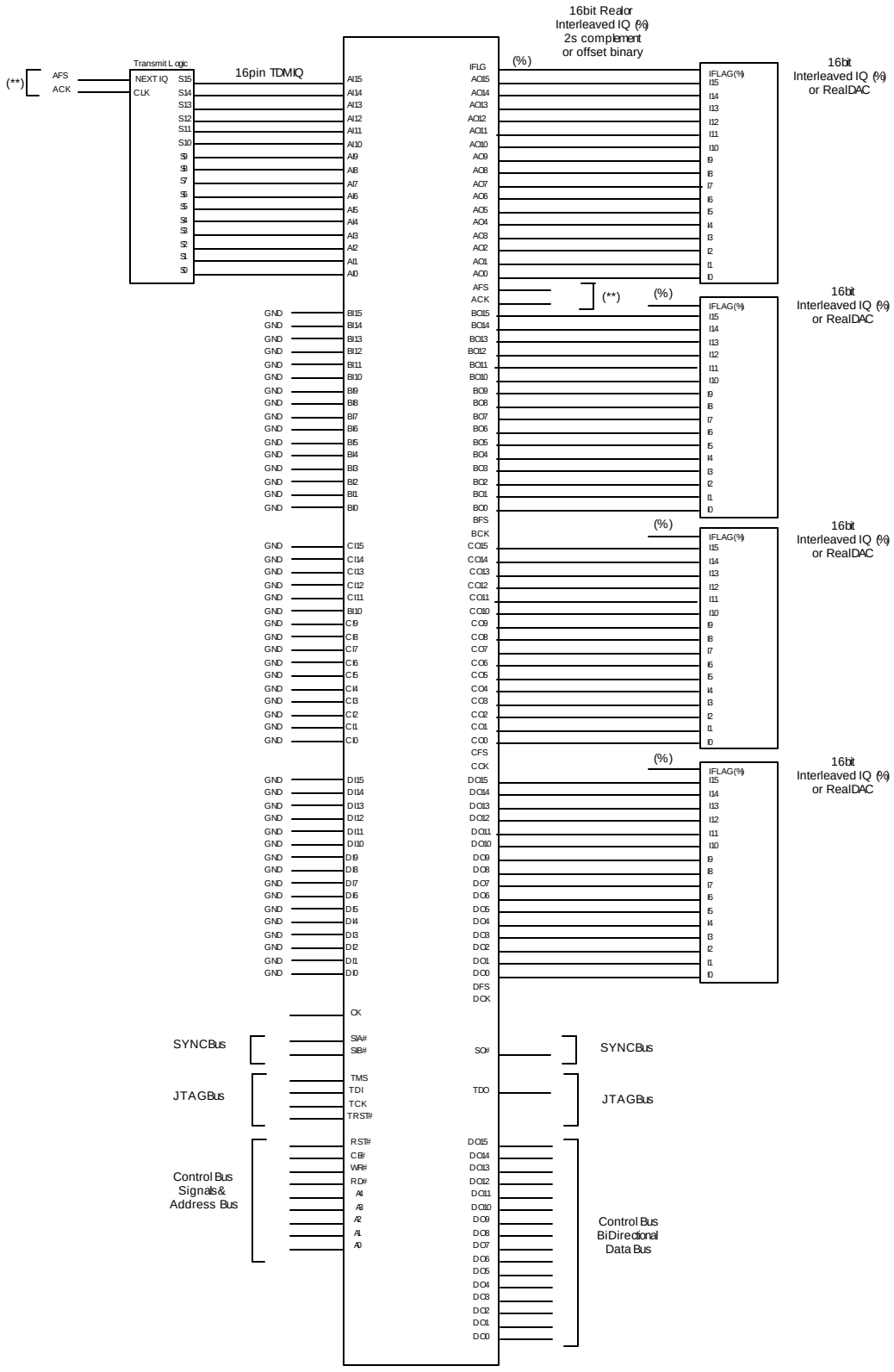


Figure 25. GC5016 DUC TDM Input Diagram
16pin TDM-IQ, 16bit DAC

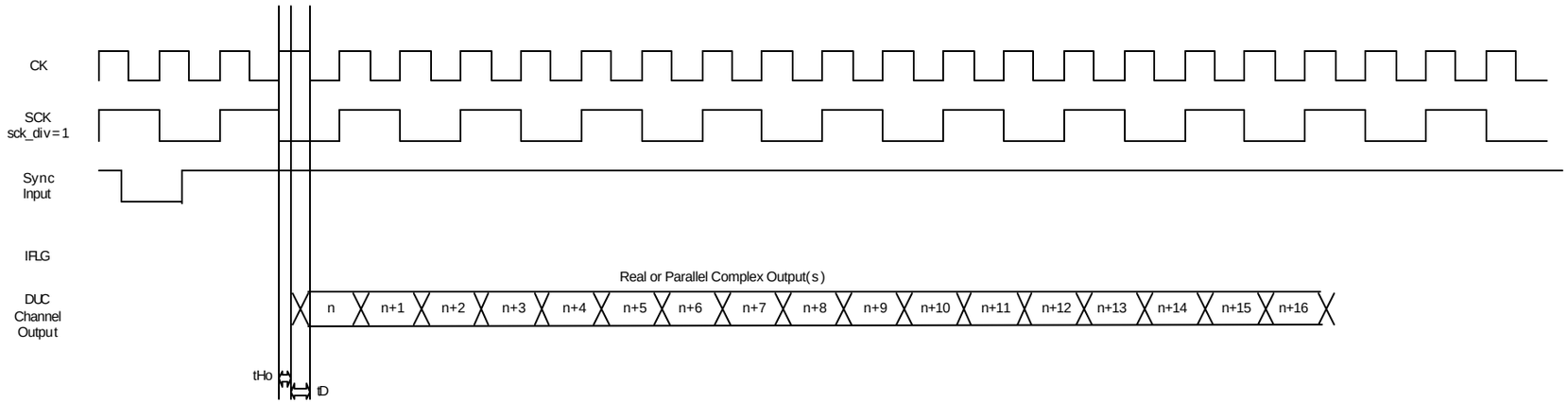


Figure 26. GC5016 DUC Real or Parallel Complex Output Timing (sck_div=1)

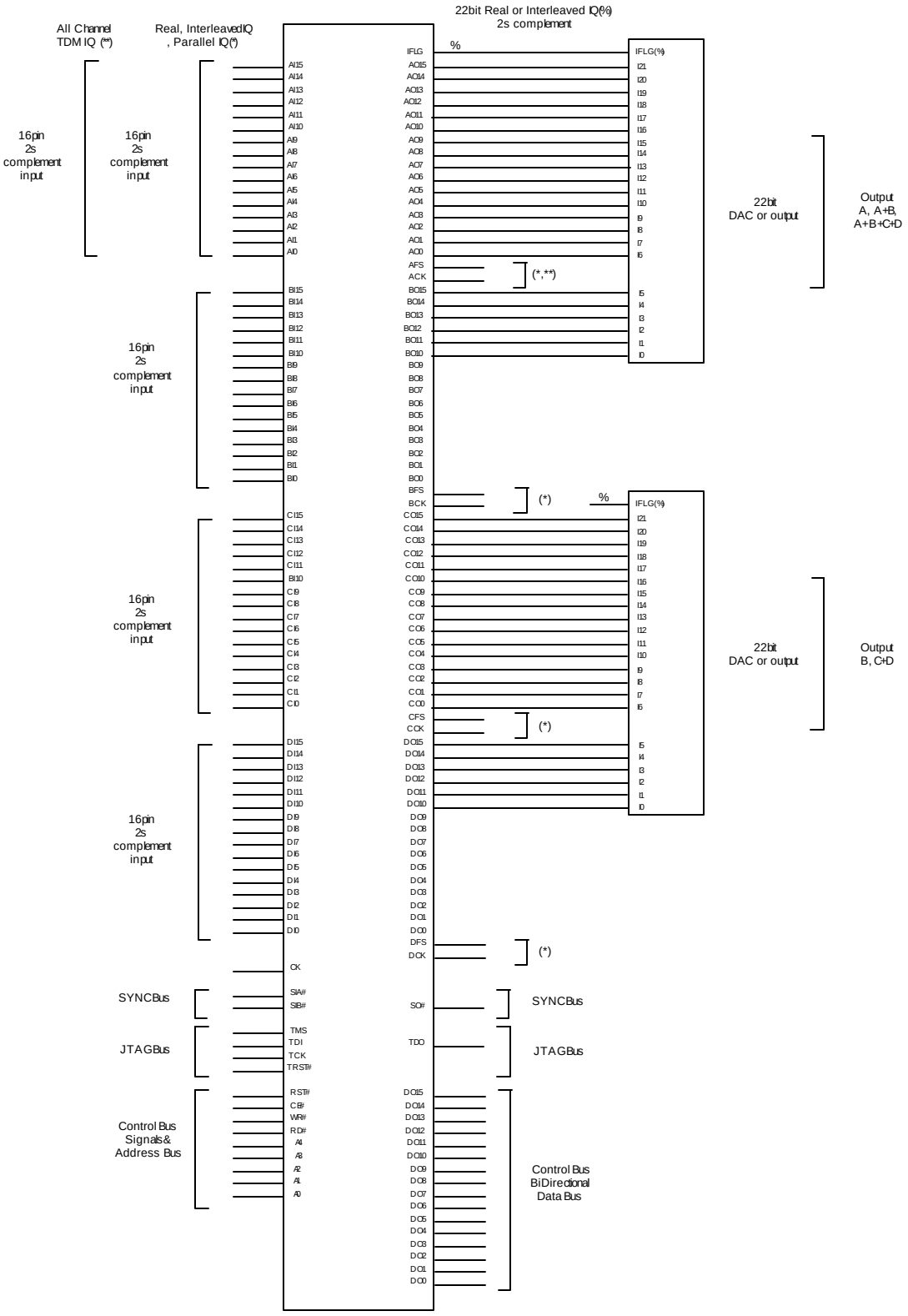


Figure 27. GC5016 DUC 22-Bit Real or Interleaved IQ Output Diagram

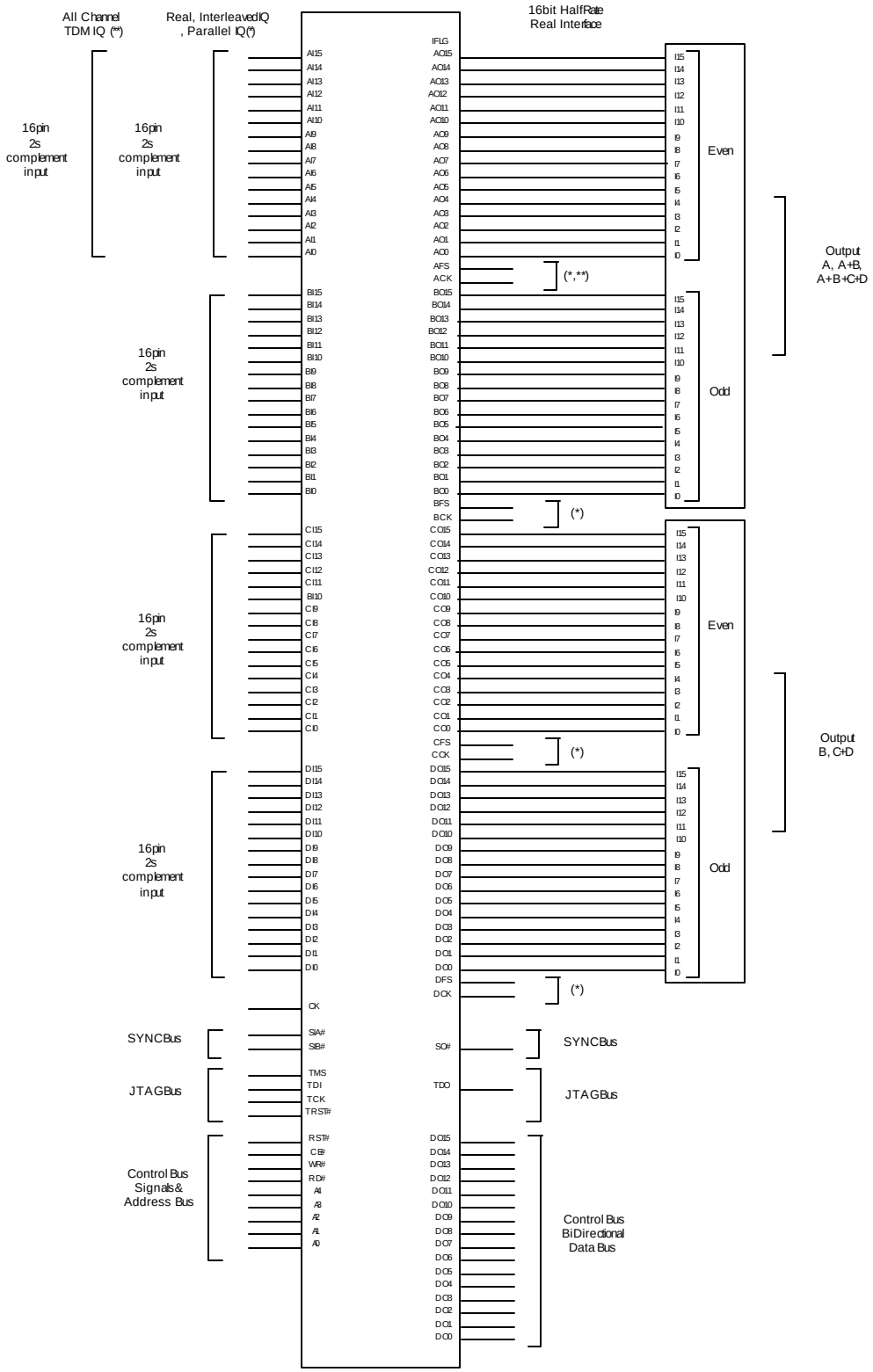


Figure 28. GC5016 DUC 16-Bit Double Rate Real Diagram

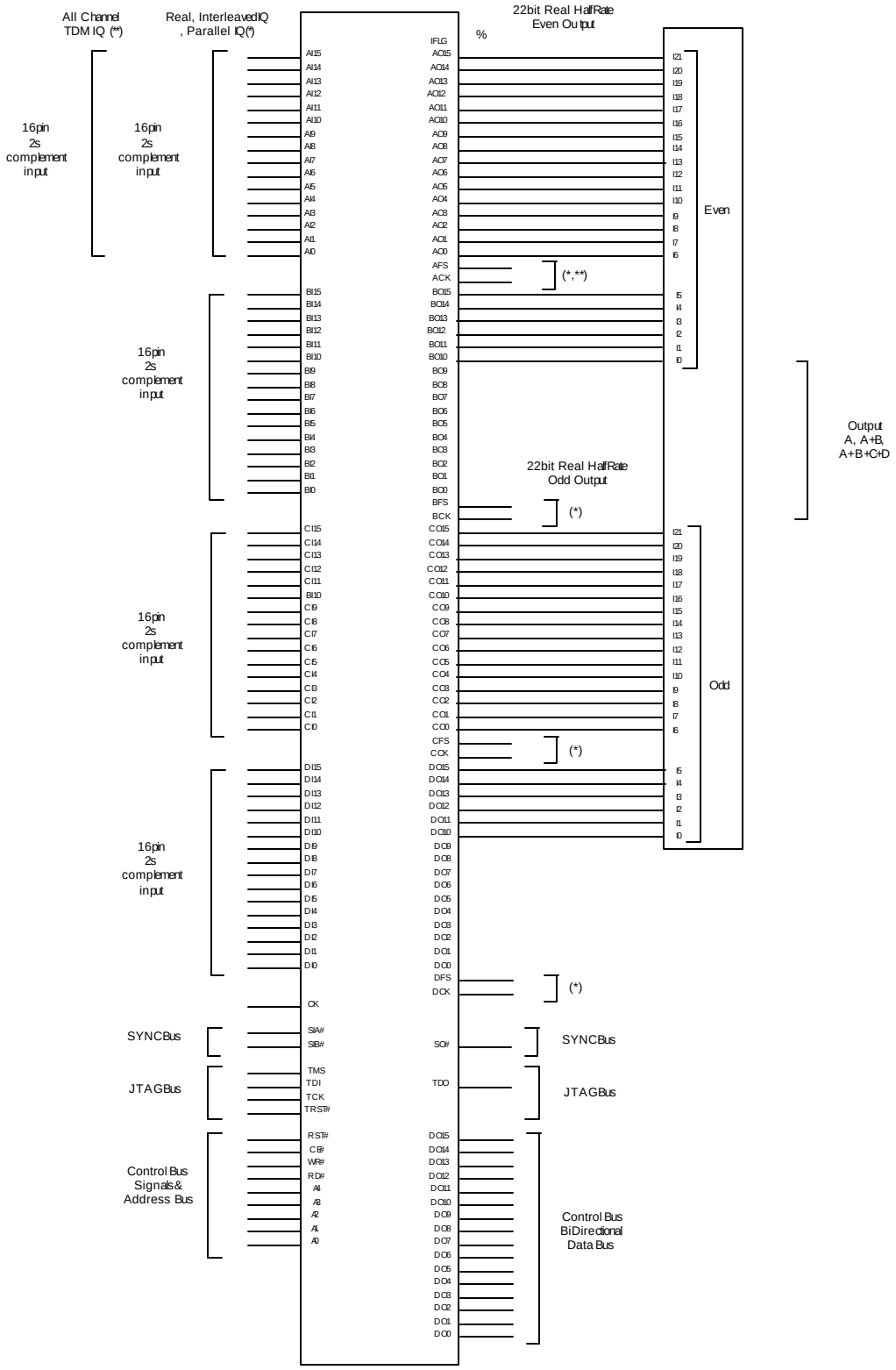


Figure 29. GC5016 DUC 22-Bit Double Rate Real Diagram
Transmit (2) 22-Bit Real, or Interleaved IQ Interface

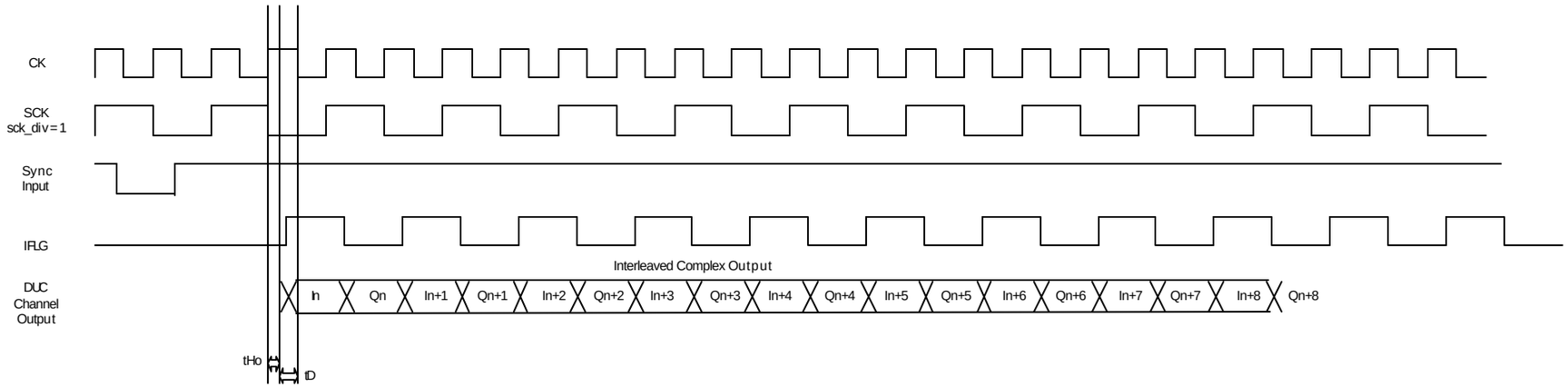


Figure 30. GC5016 DUC Interleave Complex Output Timing (sck_div = 1)

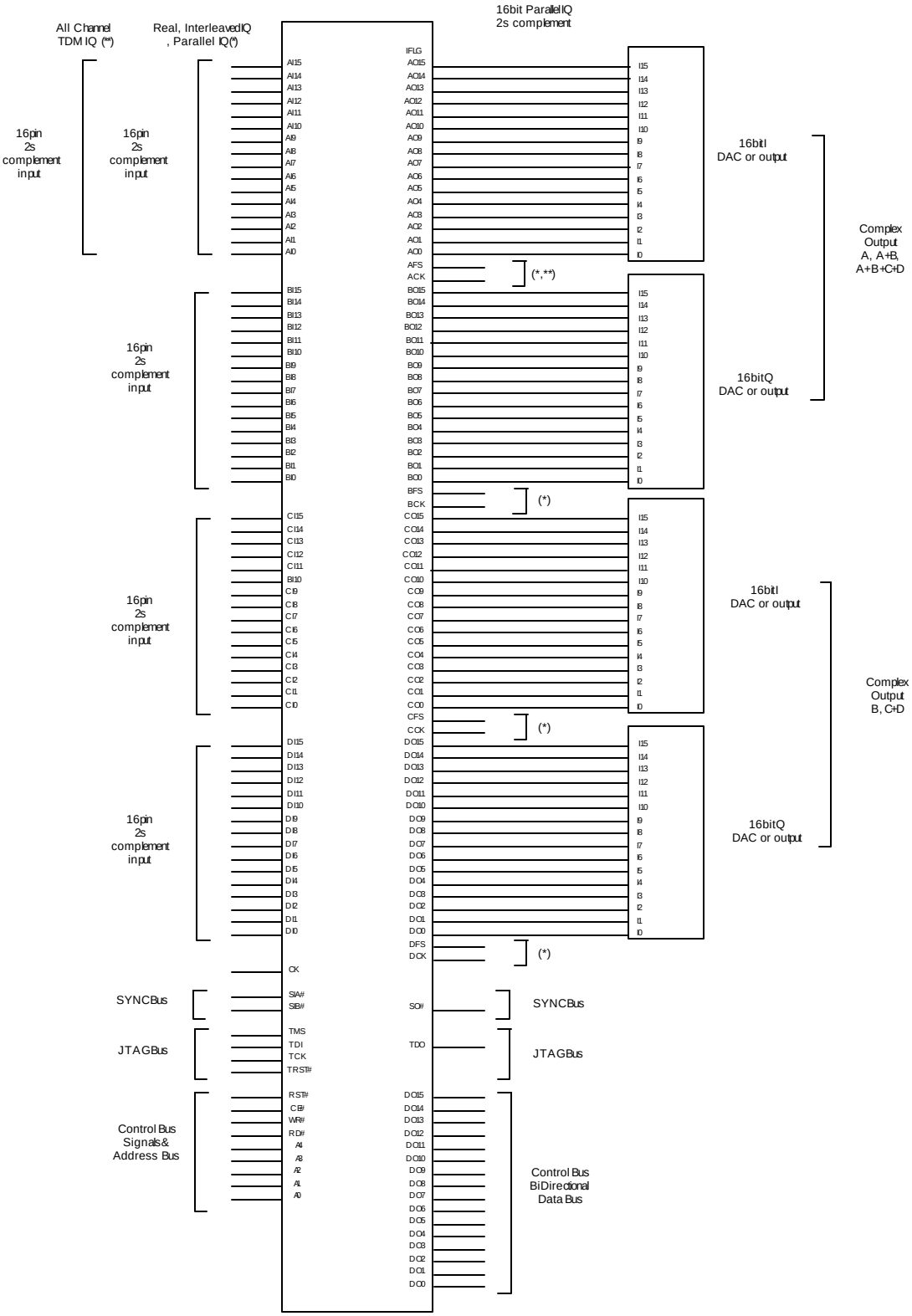


Figure 31. GC5016 DUC16-Bit Parallel Complex Full Rate Diagram (not using Sum Input) Transmit 16bit Parallel IQ Interface

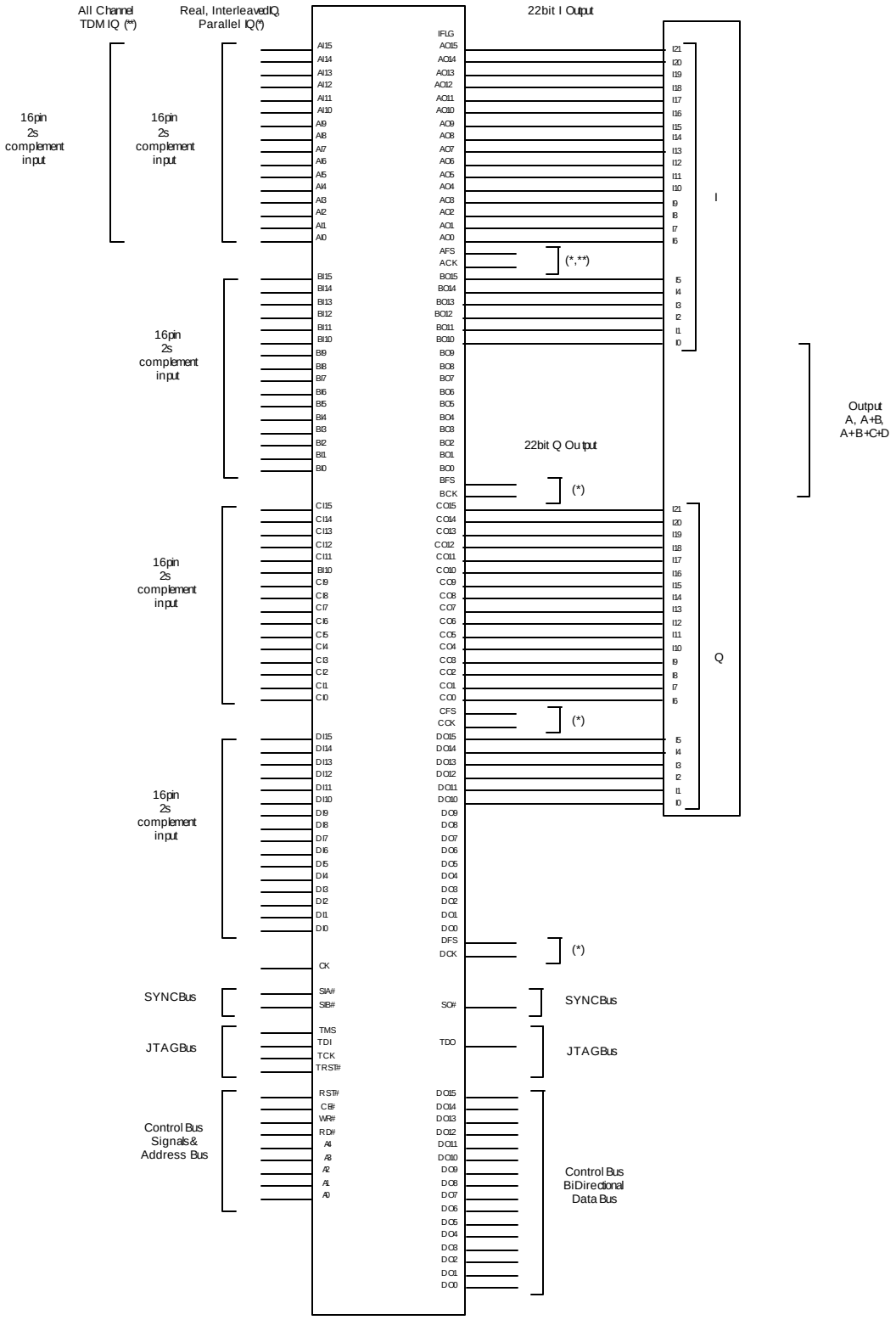


Figure 32. GC5016 DUC 22-Bit Parallel Cpmplex Full Rate Diagram
Double Rate Complex Output Interface

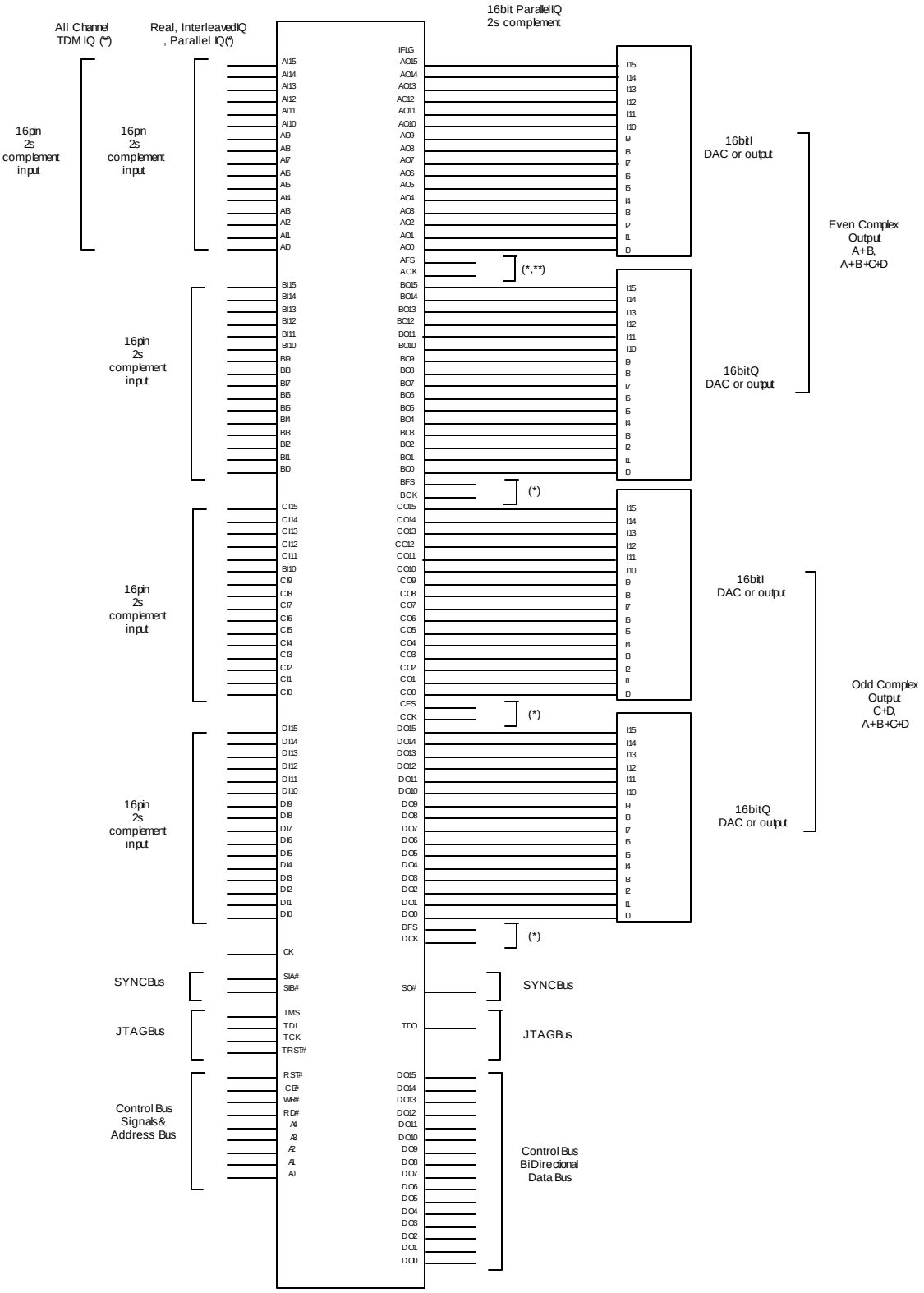


Figure 33. GC5016 DUC 22-Bit Double Rate Parallel Complex Diagram (not using Sum Input) Transmit 16bit Double Rate Parallel IQ Interface

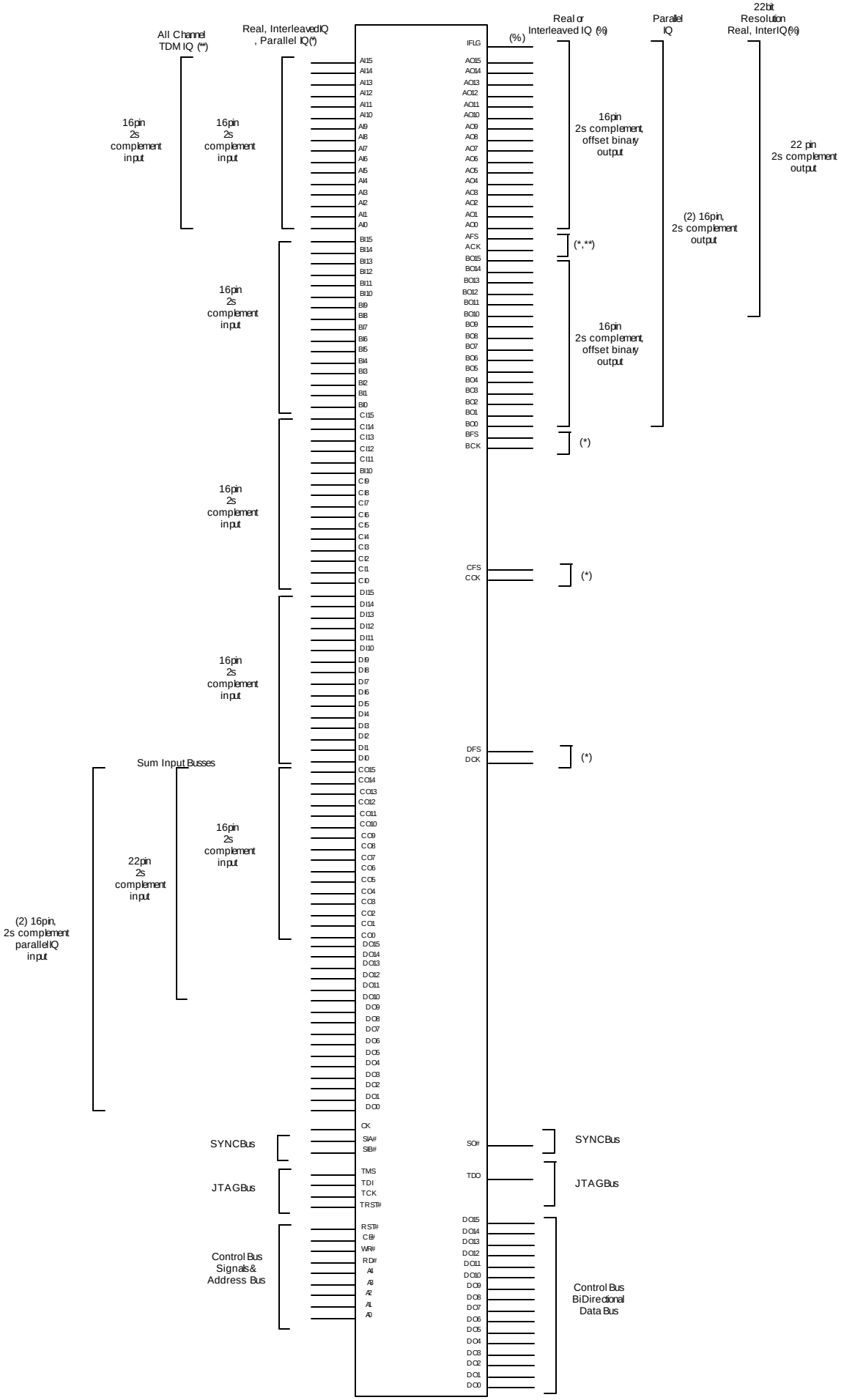


Figure 34. GC5016 DUC Sum Input Bus Diagram (using Sum Input) Transmit Output Modes

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