Failsafe in RS-485 Data Buses

By Kevin Gingerich (Email: k-gingerich@ti.com)
High-Performance Linear/Interface

Introduction

After bus-pin electrical overstress, the second most common cause of inquiries to the Texas Instruments (TI) Interface Applications Group is the unanticipated response of differential, and in particular RS-485*, line receivers to loss of input signal. When the response of a circuit is designed to provide a known state under this condition, it is commonly referred to as "failsafe." The intent of this article is to share the answers to many of these questions and to help the reader avoid similar problems.

While there are many different data transmission standards that employ differential signaling, the scope of this article is limited to RS-485-compatible circuits and standard usage. Many of the principles detailed here can be applied to other differential signaling schemes with appropriate adaptation of the system-level constraints.

We will first develop a bus electrical model and analyze receiver responses to and reasons for no input signal. Then we will investigate adding a signal and redefining the bus logic states through external and integrated options to provide failsafe response.

Bus model

A standard RS-485 bus is a single balanced-pair transmission line terminated at each end by a resistance equal to the characteristic impedance of the line. RS-485 line drivers, receivers, or transceivers are distributed along the transmission line to share data over the common bus (see Figure 1).

If the local ground connection of any line driver is selected as the zero potential reference point and noise sources are included, the equivalent circuit of the bus appears as shown in Figure 2. V_{OA} and V_{OB} are the output voltages of the line driver, R_{INEQ} is the equivalent input resistance of all the connected line circuits to their local ground, V_{ncm} is the common-mode noise voltage between the driver ground and receiver grounds (C), and V_{ndiff} is the differential noise voltage. We are assuming that the effect of the transmission line resistance on the node voltages is negligible.

Since we are primarily concerned with the voltage between A and B, it is convenient to make our zero potential at the B node and to substitute the difference voltage source (V_{OD}) for $V_{OA} - V_{OB}$, as shown in Figure 3. Calculation of the receiver differential input voltage, V_{ID}, is then trivial: $V_{ndiff} + V_{OD}$.

*RS-485 is specified in ANSI TIA/EIA-485-A and ISO/IEC-8482:1993.

Figure 1. Standard RS-485 bus

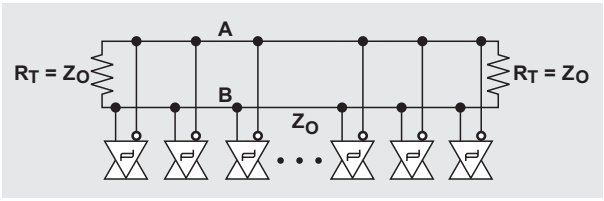


Figure 2. Electrical equivalent circuit for the standard RS-485 bus

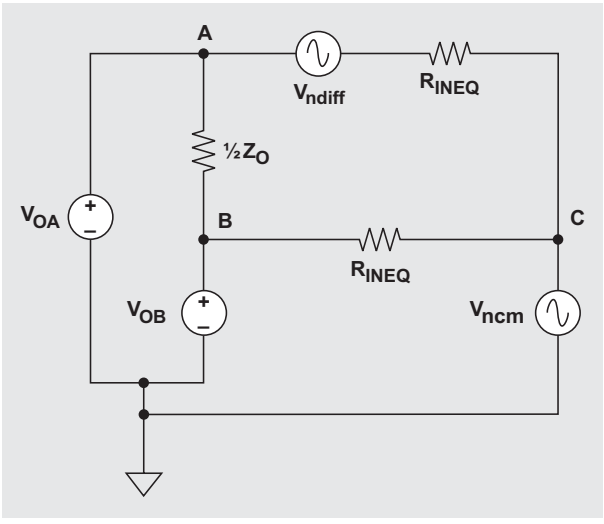
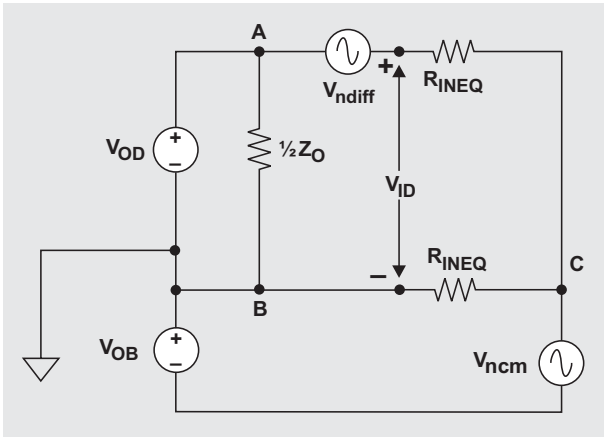


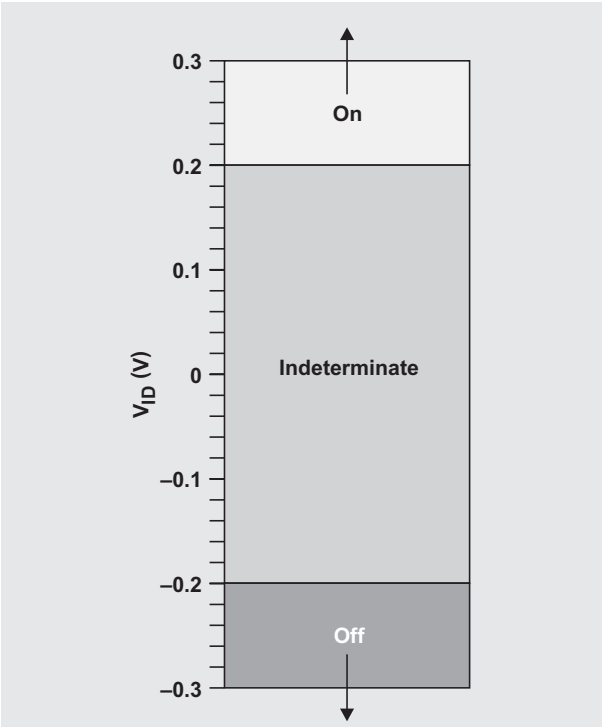
Figure 3. Redrawn RS-485 bus equivalent circuit



Differential receiver responses

The input signal to the transmission line is the driver output voltage; the differential receiver must detect what comes out. The first parameter to consider for a receiver is the differential input voltage threshold, V_{IT}, as it defines the voltage needed to place the receiver output in a high or low state. The specified maximum and minimum V_{IT} establish the limits for V_{IT}, and difference voltages above or below them assure that the receiver will indicate a valid logic state at its output. RS-485 requires a maximum V_{IT} of 200 mV and a minimum of –200 mV under all operating conditions and common-mode input voltages. Figure 4 shows a graphical representation of the differential voltage states transition region between 0.3 V and –0.3 V. The arrows indicate that the valid differential input voltage extends to 6 V or –6 V.

Figure 4. RS-485 differential voltage states



A differential input voltage between the maximum and minimum threshold lies in the transition region and results in an indeterminate output state. The output may be high, low, or on its way between states. Consider a line receiver as a differential amplifier with a gain of about 100,000. V_{IT} is the input voltage where the output would be one-half of the way between high and low; and, with no feedback for hysteresis, it takes only a few tens of microvolts above or below the threshold for the output to switch to a high or low state. There is likely this much in differential noise in the system that, if near the threshold, could cause oscillation of the output.

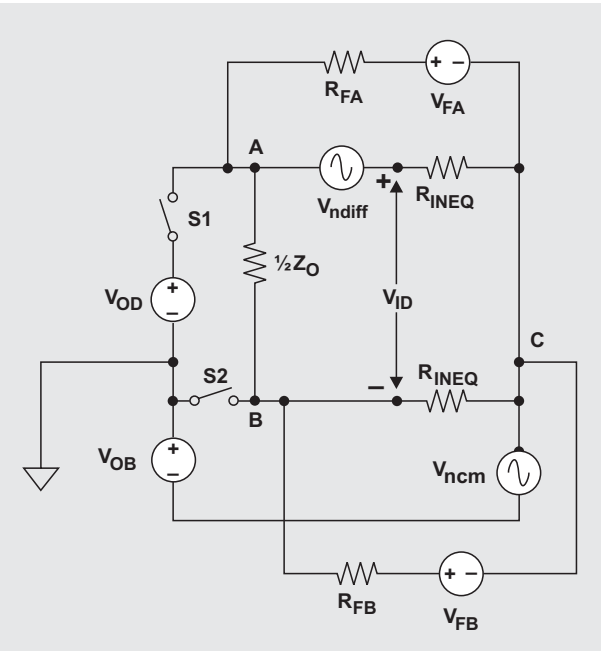
For this reason, it is common to employ some positive feedback to the differential amplifier input stages to provide some hysteresis in the input-to-output transfer function. This makes the positive-going differential threshold higher than the negative-going threshold and requires that the difference be exceeded to switch to the opposite state. This decreases the chance of oscillation from differential noise but does not provide a predictable output state, as the output will remain in the last state prior to input loss.

Adding a steady-state bias signal

Since the V_{OD} source in Figure 3 defines the bus state, disconnecting it or a zero-volt output leaves the standard bus state to be determined by the differential noise in the system or indeterminate. Operating scenarios that may disconnect V_{OD} from the circuit would include physical removal or, much more commonly, disabling the driver while bus access is being granted to another driver on the bus. A zero-volt output may occur due to a short circuit between signal wires or damage to a line circuit.

The problem of keeping the bus in a known state when no active driver is connected may be solved by adding a steady-state differential voltage to the bus. This in effect adds a driver that will not be switched, disabled, or disconnected. This failsafe driver is added to the circuit model in Figure 5 as voltage sources V_{FA} and V_{FB}, along with their respective source resistances R_{FA} and R_{FB}. The failsafe driver is referenced to node C since V_{OD} represents any driver on the circuit and the two grounds may not be at the same potential. Note that S1 and S2 are added to show the driver disconnected from the bus.

Figure 5. Failsafe driver added to equivalent bus circuit



The effect of adding the failsafe driver is determined by shorting all voltage sources other than V_{FA} and V_{FB} and summing the currents at nodes A and B as follows.

$$\frac{V_{FA}-V_A}{R_{FA}}-\frac{V_A}{R_{INEQ}}+\frac{V_B-V_A}{\frac{1}{2}Z_O}=0$$

$$\frac{V_{FB}-V_B}{R_{FB}}-\frac{V_B}{R_{INEQ}}+\frac{V_A-V_B}{\frac{1}{2}Z_O}=0$$

Dispensing with the algebra details and solving for $V_A - V_B$ gives us

$$V_A-V_B=\frac{\frac{V_{FA}}{R_{FA}}\left(\frac{1}{R_{FB}}+\frac{1}{R_{INEQ}}\right)-\frac{V_{FB}}{R_{FB}}\left(\frac{1}{R_{FA}}+\frac{1}{R_{INEQ}}\right)}{\left(-\frac{1}{R_{INEQ}}-\frac{1}{R_{FA}}-\frac{2}{Z_O}\right)\left(-\frac{1}{R_{INEQ}}-\frac{1}{R_{FB}}-\frac{2}{Z_O}\right)-\left(\frac{2}{Z_O}\right)^2}.$$

Since circuit balance requires that $R_{FA} = R_{FB} = R_F$, the *failsafe differential bias voltage* then becomes

$$V_A-V_B=\frac{\frac{V_{FA}}{R_F}\left(\frac{1}{R_F}+\frac{1}{R_{INEQ}}\right)-\frac{V_{FB}}{R_F}\left(\frac{1}{R_F}+\frac{1}{R_{INEQ}}\right)}{\left(\frac{1}{R_{INEQ}}+\frac{1}{R_F}+\frac{2}{Z_O}\right)^2-\left(\frac{2}{Z_O}\right)^2}. \quad \textbf{(1)}$$

Normally, only a 5- or 3.3-V supply is available for the failsafe voltage sources V_{FA} or V_{FB}; and, from Equation 1, we know they cannot be the same and generate a difference voltage. Therefore, we set $V_{FB} = 0$ V in the equation for *single-supplied failsafe differential voltage*,

$$V_A-V_B=\frac{\frac{V_{FA}}{R_F}\left(\frac{1}{R_F}+\frac{1}{R_{INEQ}}\right)}{\left(\frac{1}{R_{INEQ}}+\frac{1}{R_F}+\frac{2}{Z_O}\right)^2-\left(\frac{2}{Z_O}\right)^2}. \quad \textbf{(2)}$$

Note that we could just as well have made $V_{FA} = 0$ V and generated a negative failsafe bias voltage.

Before applying Equation 2, we establish a constraint for R_F. In Figure 5, the added R_F is in parallel with R_{INEQ}, which represents the equivalent resistance of the line circuits attached to the bus. This additional load has the effect of requiring more output current from a bus driver with the common-mode voltage V_{CM}. Since standard RS-485 line drivers are required to handle only 375-Ω common-mode loads, the parallel combination of R_F and R_{INEQ} is limited by

$$\frac{1}{375}>\left(\frac{1}{R_F}+\frac{1}{R_{INEQ}}\right).$$

Applying this constraint gives us the equation for the *maximally loaded-bus failsafe voltage*,

$$V_A-V_B=\frac{\frac{V_{FA}}{R_F}\left(\frac{1}{375}\right)}{\left(\frac{1}{375}+\frac{2}{Z_O}\right)^2-\left(\frac{2}{Z_O}\right)^2}. \quad \textbf{(3)}$$

The failsafe bias voltage $V_A - V_B$ is chosen and the R_F is determined with the appropriate substitutions for V_{FA} and Z_O. For example, a desired 0.25-V failsafe bias on an RS-485 bus segment with a 120-Ω characteristic impedance cable, differentially terminated with 120-Ω resistors at each end, and a 5-V ±5% supply would give us the values of Z_O= 120 Ω, V_{FA} = 4.75 V, and $V_A - V_B$ = 0.25 V. Solving for R_F results in 528 Ω. In application, a 510-Ω pull-up resistor to 5 V on line A and a 510-Ω pull-down resistor to ground on line B are connected somewhere on the bus. It is important to recognize that R_{INEQ} must be greater than 1.4 kΩ to meet the common-mode loading constraint. This limits the bus to eight 12-kΩ, sixteen 24-kΩ, or thirty-two 48-kΩ input resistance nodes.*

Adding a failsafe bias keeps a known state on the bus at all times but does not come without some system-level trade-offs. As already discussed, the number of nodes may be limited and the differential noise margin is reduced compared to the bus without the failsafe bias. Although we have developed a lumped instantaneous model for the bus, in reality it is a distributed-parameter dynamic system; and initial conditions are superimposed upon the response from desired inputs. In other words, when V_{OD} is changed, the failsafe bias voltage is added to the response. This causes an asymmetrical V_{ID} with more differential voltage in one state than the other. Both of these trade-offs call for keeping the failsafe bias as low as possible; but how much is enough?

We know that a standard RS-485 receiver needs a V_{ID} of 200 mV to define the bus state, and V_{ID} with no active driver connected is the failsafe bias $V_A - V_B$ plus the differential noise voltage V_{ndiff}. Therefore, the requirement is that $(V_A - V_B) > (200\text{ mV} + V_{ndiff})$. In well-balanced systems, it is not difficult to keep the differential noise below 50 mV, so a failsafe bias of 250 mV would be sufficient. If there is doubt about the differential noise in a particular environment, measurement is the only recourse to be sure of sufficient failsafe noise margin without unduly limiting the number of bus connections or differential noise margin.

*In RS-485 parlance, these are 1-UL, ½-UL, and ¼-UL circuits, respectively.

Redefining bus states

If the constraints imposed on the system by adding a bus failsafe bias voltage are too great or if shorted lines are included, the user may avoid the problem altogether by defining zero volts as a valid bus state. Since RS-485 defines the bus state with a more than 200-mV difference, the user is free to use lower decision thresholds to avoid unpredictable receiver responses with no input signal.

The SN65HVD08 and other recent RS-485 products from TI offer this option. Figure 6 shows the input thresholds for the SN65HVD08 compared to those of RS-485. It also shows that the SN65HVD08 will indicate the on and off states as required by the standard but is also on with no difference voltage—the failsafe condition. (The arrows indicate that the valid differential input voltages extend beyond the scale shown.)

The maximum V_{IT} for the SN65HVD08 is –10 mV and provides a worst-case 10 mV of differential noise margin with no input signal. Depending upon the user's risk tolerance or the system noise, an additional margin may be added with the steady-state failsafe bias as described earlier in conjunction with the redefined input thresholds. This reduces the required offset voltage and the negative trade-offs associated with that technique.

Since this failsafe approach is implemented in the receiver, it has a few drawbacks. Application to an entire bus requires that the user have configuration control over all the nodes connected to it. The default failsafe output is predetermined by the IC manufacturer, possibly limiting design options; and V_{IT} asymmetry adds jitter. These affect only a small percentage of applications.

Loss-of-signal detection

Another approach to failsafe was introduced with TI's SN65HVD20 family of transceivers. These devices include a differential window comparator in parallel with the RS-485 receiver to detect loss of signal. Once detected, the output of the receiver is forced to a high level after a time delay. This results in the state thresholds shown in Figure 7.

Separation of the window comparator from the main line receiver allows symmetry of V_{IT} about zero on the main receiver, avoiding addition of jitter for high-speed applications. This separation, as implemented in the SN65HVD2x devices, offers 40 mV of differential noise margin with no signal. This is the only approach that creates a unique signal indicating signal loss that could be brought out of the line circuit for customized user processing.

The propagation-delay time of the window comparator can be a system issue since it is set by a timer in the SN65HVD2x and the user must account for the output state during the time between signal loss and activation of the failsafe output.

Figure 6. SN65HVD08 and RS-485 input voltage thresholds

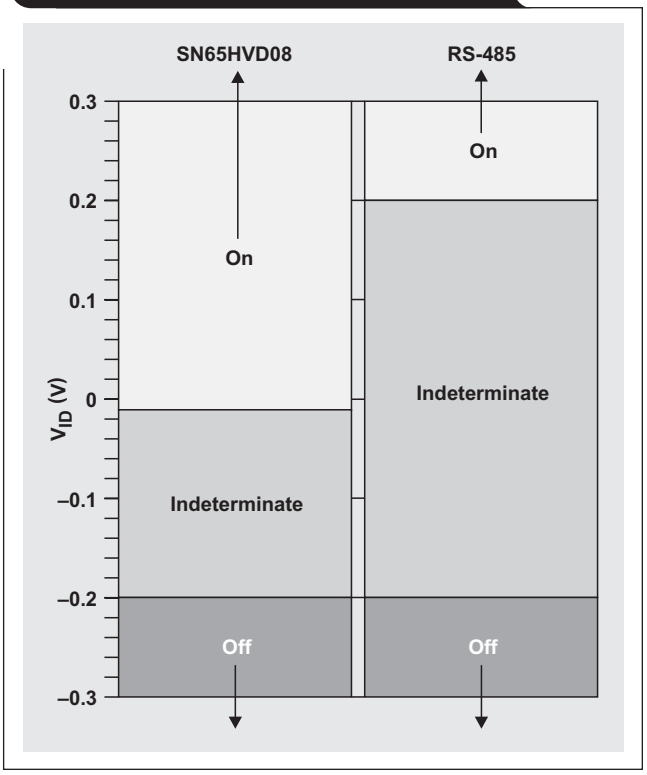
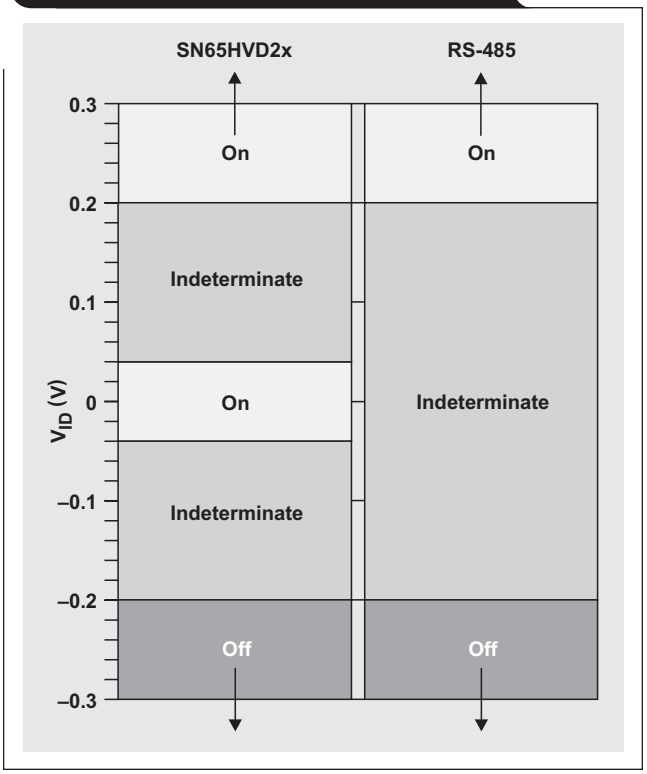


Figure 7. SN65HVD2x and RS-485 input voltage thresholds



Summary

Unexpected differential receiver behavior due to the loss of input signal is a common source of application problems. Obtaining a predictable output under this condition is called failsafe and three approaches were presented; adding a failsafe bias voltage to the bus, redefining the bus states, and loss-of-signal detection. The advantages and disadvantages of these are summarized in Table 1.

Related Web sites

analog.ti.com
www.ti.com/sc/device/SN65HVD08
www.ti.com/sc/device/SN65HVD20

Table 1. Summary of failsafe techniques

FAILSAFE TECHNIQUE	ADVANTAGES	DISADVANTAGES
Adding a bus bias voltage	• Uses standard receivers • Adaptable to application	• Reduces maximum number of nodes • Reduces differential noise margin • Adds jitter • Requires two resistors • Does not handle shorted lines
Redefining zero volts	• Available integrated with the receiver • Handles shorted-line condition	• Requires nonstandard receiver • Fixed failsafe output state • Adds jitter
Loss-of-signal detector	• Available integrated with the receiver • Uses standard receivers (with stand-alone window detector) • Handles shorted-line condition • Does not add jitter • Can create information for use by application	• Delay time from signal loss to forced output

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265