Analog Applications Journal

Power factor corrected (PFC) preregulators are generally used in offline ac/dc power converters with a power level higher than 75 W or to meet line harmonic requirements such as EN61000-3-2. PFC is typically done with a boost converter ac/dc topology due to the continuous input current that can be manipulated through average current-mode control to achieve a near-unity power factor (PF). However, due to the high output voltage of a boost converter, a second dc/dc converter is generally needed to step down the output to a usable voltage. In the past this has been accomplished with two pulse-width modulators (PWMs). One PWM controlled and regulated the PFC power stage, while the second was used to control the step-down converter. The UCC28517 controller reduces the need for two PWMs and combines both of these functions into one control-integrated circuit. The UCC28517 operates the second converter at twice the switching frequency of the PFC stage, which reduces the size of the boost magnetics and the ripple current in the boost capacitor. For more information on this device, please see Reference 7. This article reviews the design of a 100-W ac/dc power stage with power factor correction. A review of the second stage can be found in a future issue of TI’s Analog Applications Journal.

Variable definitions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΔI</td>
<td>Change in boost inductor current</td>
</tr>
<tr>
<td>η1</td>
<td>Output A efficiency</td>
</tr>
<tr>
<td>η2</td>
<td>Output B efficiency</td>
</tr>
<tr>
<td>CDiode</td>
<td>Boost diode capacitance</td>
</tr>
<tr>
<td>Comp</td>
<td>Dynamic range of the multiplier comp pin</td>
</tr>
<tr>
<td>Coss</td>
<td>FET drain-to-source capacitance</td>
</tr>
<tr>
<td>fc</td>
<td>Voltage-loop crossover frequency</td>
</tr>
<tr>
<td>fline</td>
<td>Input line frequency</td>
</tr>
<tr>
<td>f1p</td>
<td>Single-pole filter frequency</td>
</tr>
<tr>
<td>fP</td>
<td>Ripple frequency</td>
</tr>
<tr>
<td>fS</td>
<td>Minimum switching frequency</td>
</tr>
<tr>
<td>fSA</td>
<td>Output A switching frequency</td>
</tr>
<tr>
<td>fSB</td>
<td>Output B switching frequency</td>
</tr>
<tr>
<td>Gid(s)</td>
<td>Power stage gain</td>
</tr>
<tr>
<td>Gca</td>
<td>Current amplifier gain</td>
</tr>
<tr>
<td>Gcs(s)</td>
<td>Control transfer function</td>
</tr>
<tr>
<td>Gcol(s)</td>
<td>Control to output transfer function</td>
</tr>
<tr>
<td>Gm</td>
<td>Transconductance amplifier gain</td>
</tr>
<tr>
<td>Gvea</td>
<td>Voltage amplifier gain</td>
</tr>
<tr>
<td>HI(s)</td>
<td>Voltage divider gain</td>
</tr>
<tr>
<td>IMout</td>
<td>Multiplier output</td>
</tr>
<tr>
<td>IPK</td>
<td>Peak inductor current, peak diode current, peak switch current</td>
</tr>
<tr>
<td>IRMS</td>
<td>RMS device current</td>
</tr>
<tr>
<td>ISS</td>
<td>UCC28517 soft-start current of 10 µA</td>
</tr>
<tr>
<td>K</td>
<td>Constant typically equal to 1/V</td>
</tr>
<tr>
<td>Pcond</td>
<td>Device conduction losses</td>
</tr>
<tr>
<td>PCoss</td>
<td>Power dissipated by the FET’s drain-to-source capacitance</td>
</tr>
<tr>
<td>Pdiode</td>
<td>Total loss in the boost diode</td>
</tr>
<tr>
<td>PDIODE</td>
<td>Loss due to boost diode capacitance</td>
</tr>
<tr>
<td>PFET, TR</td>
<td>FET transition losses</td>
</tr>
<tr>
<td>PGATE</td>
<td>Power dissipated by the FET gate</td>
</tr>
<tr>
<td>POUTA</td>
<td>Output A maximum power</td>
</tr>
<tr>
<td>POUTB</td>
<td>Output B maximum power</td>
</tr>
<tr>
<td>PQ1</td>
<td>Total FET losses</td>
</tr>
<tr>
<td>Psemi</td>
<td>Power dissipated by a semiconductor device</td>
</tr>
<tr>
<td>QGate</td>
<td>FET gate charge</td>
</tr>
<tr>
<td>RDCS</td>
<td>Thermal impedance case-to-sink</td>
</tr>
<tr>
<td>RJC</td>
<td>Thermal impedance junction-to-case</td>
</tr>
<tr>
<td>RGsa</td>
<td>Thermal impedance sink-to-air</td>
</tr>
<tr>
<td>RDS(ON)</td>
<td>On resistance of the FET</td>
</tr>
<tr>
<td>RAC</td>
<td>Multiplier input resistance</td>
</tr>
<tr>
<td>Rsense</td>
<td>Current sense resistor</td>
</tr>
<tr>
<td>s(f)</td>
<td>Frequency domain (2πf)</td>
</tr>
<tr>
<td>Tamb</td>
<td>Ambient temperature</td>
</tr>
<tr>
<td>tblank</td>
<td>Amount of leading-edge blanking time</td>
</tr>
<tr>
<td>tf</td>
<td>FET fall time</td>
</tr>
<tr>
<td>tholdup</td>
<td>Boost capacitor hold-up time</td>
</tr>
<tr>
<td>Tjmax</td>
<td>Maximum semiconductor temperature</td>
</tr>
<tr>
<td>ton</td>
<td>Boost inductor energizing on time</td>
</tr>
<tr>
<td>TR</td>
<td>FET rise time</td>
</tr>
<tr>
<td>TS(f)</td>
<td>Voltage loop frequency response</td>
</tr>
<tr>
<td>Vc</td>
<td>Control voltage</td>
</tr>
<tr>
<td>VCSense</td>
<td>Maximum current sense voltage</td>
</tr>
<tr>
<td>Vdrop</td>
<td>Amount of voltage the boost capacitor has to hold up</td>
</tr>
<tr>
<td>VEA</td>
<td>Voltage amplifier gain</td>
</tr>
<tr>
<td>Vf</td>
<td>Forward voltage of a diode</td>
</tr>
<tr>
<td>VGATE</td>
<td>Gate-drive voltage</td>
</tr>
<tr>
<td>VIN</td>
<td>RMS input voltage</td>
</tr>
<tr>
<td>VOUTA</td>
<td>Boost output voltage</td>
</tr>
<tr>
<td>VOUTB</td>
<td>Auxiliary output voltage</td>
</tr>
<tr>
<td>VP</td>
<td>Oscillator ramp voltage</td>
</tr>
<tr>
<td>Vpp</td>
<td>Output peak-to-peak ripple voltage</td>
</tr>
<tr>
<td>Vripple</td>
<td>Output B ripple voltage</td>
</tr>
<tr>
<td>VREF</td>
<td>UCC28517 internal reference</td>
</tr>
<tr>
<td>VVFF</td>
<td>Multiplier feed-forward voltage</td>
</tr>
<tr>
<td>Zout</td>
<td>Compensation impedance</td>
</tr>
</tbody>
</table>
The following design example was generated using typical parameters rather than worst-case values. Please refer to Table 1 and Figures 1–3 for design specifications and component placement. All variables are defined in the sidebar on page 13.

### PFC boost ac/dc regulator design (OUTA)

#### Inductor selection

The boost inductor is selected based on the maximum ripple current at the peak of minimum line voltage. The following equations can be used to calculate the required inductor for the boost power stage, assuming that the boost inductor ripple current is 25% of the maximum input current.

\[
\Delta I = \frac{P_{OUTA} \times 0.25 \times \sqrt{2}}{V_{IN(min)} \times \eta_1}
\]

\[
D = 1 - \frac{V_{IN(min)} \times \sqrt{2}}{V_{OUTA}}
\]

\[
L_1 = \frac{V_{IN(min)} \times \sqrt{2} \times D}{\Delta I \times f_{SA}}
\]
Figure 2. dc/dc power stage schematic

Figure 3. Controller schematic
The calculated inductance for this design was roughly 1.7 mH. To make the design process easier, Cooper Electronics designed the inductor (part number CTX08-14730).

**Boost switch (Q1) and boost diode (D3) selection**

To select Q1 and D3 properly, a power budget is generally set for these devices to maintain the desired efficiency goal. To meet the power budget for this design, an IRFP450 HEX FET and an HFA08TB60 fast-recovery diode from International Rectifier were chosen.

Equations used to calculate the loss in Q1 were:

\[ I_{RMS\_FET} = \frac{P_{OUTA}}{\eta_1 \times V_{IN(min)}} \times \frac{V_{OUTA}}{V_{IN(min)}} \times \sqrt{2 \times \frac{16 \times \sqrt{2} \times V_{IN(min)}}{3\pi \times V_{OUTA}}} \]

\[ I_{RMS\_L} = \frac{P_{OUTA} \times \sqrt{2}}{\eta_1 \times V_{IN(min)}} \times \frac{V_{OUTA}}{V_{IN(min)}} \]

\[ P_{GATE} = Q_{GATE} \times V_{GATE} \times f_s \]

\[ P_{COSS} = \frac{1}{2} C_{COSS} \times \frac{V_{OUTA(min)}}{V_{IN(min)}} \times f_s \]

\[ P_{COND\_FET} = R_{DS(on)} \times I_{RMS\_FET} \]

\[ P_{FET\_TR} = \frac{1}{2} V_{OUTA} \times I_{RMS\_L} \times t_R \times f_s \]

\[ P_{Q1} = P_{GATE} + P_{COSS} + P_{COND\_FET} + P_{FET\_TR} \]

\[ I_{PK} = \frac{P_{OUTA} \times \sqrt{2}}{\eta_1 \times V_{IN(min)}} \]

\[ I_{RMS\_DIODE} = \frac{P_{OUTA}}{\eta_1 \times V_{IN(min)}} \times \sqrt{\frac{16 \times V_{OUTA}}{3\pi \times \sqrt{2} \times V_{IN(min)}}} \]

\[ P_{COND\_DIODE} = V_I \times I_{RMS\_DIODE} \]

\[ P_{DIODE\_CAP} = C_{DIODE} \times V_{OUTA} \times f_S \]

\[ P_{DIODE} = P_{COND\_DIODE} + P_{DIODE\_CAP} \]

**Heat sinks**

The following equation can be used to calculate the minimum required thermal impedance of the heat sinks (\(R_{BSA}\)) for this design for Q1 and D3.

\[ R_{BSA} = \frac{T_{j_{max}} - T_{amb}}{P_{semi} \times (R_{hes} + R_{hec})} \]

The heat sink was designed to ensure that the junction temperature would not go above 75% of these devices’ rated maximum with convection cooling, assuming a maximum ambient temperature of 60°C. The heat sink required for Q1 was an AVVID, part number 513201 B 0 25 00.

**Output hold-up capacitor (C3) selection**

The following equations were used to estimate the minimum hold-up capacitor (C3) size and the maximum allowable RMS current through the boost capacitor (\(I_{RMS\_C3}\)).

\[ C_3 \geq 2 \times \frac{P_{OUTA}}{V_{OUTA} - (V_{OUTA} - V_{drop})^2} \]

\[ I_{RMS\_C3} = \frac{P_{OUTA}}{V_{OUTA}} \times \sqrt{\frac{16 \times V_{OUTA}}{3\pi \times V_{IN(min)} \times \sqrt{2}} - 1} \]

The hold-up capacitor was designed for 16.7 ms of hold-up time (\(t_{holdup}\)), allowing an output voltage drop (\(V_{drop}\)) of 85 V.

**Peak-current limit for the boost power stage**

Resistor dividers R14 and R29, along with current sense resistor R5, set up the peak-limit comparator of the UCC28517 that is used to protect the boost switch Q1 from excessive currents. This comparator should be set up so that it does not interfere with the boost converter’s power limit or with the pulse-by-pulse current limiting of the step-down converters. For this design example, the flyback converter was designed to go into pulse-by-pulse current limiting at roughly 130% of maximum output power, and the power limit of the boost converter was set at 140% of the maximum output power. The peak-current limit for the boost stage was selected to engage at 150% of the maximum output power to ensure circuit stability.

The current sense resistor R5 was selected to operate over a 1-V dynamic range (\(V_{dynamic}\)) with the following equation.

\[ R5 = \frac{V_{dynamic}}{I_{PK} + 0.5 \times \Delta I} \]

The following equation can be used to size resistor R14 properly if R29 is first selected as a standard resistance value.

\[ R14 = \left( \frac{P_{OUTA} \times 1.5 \times \sqrt{2}}{V_{IN(min)} \times \eta_1 + \Delta I} \right) \times R5 \times R29 \times \frac{V_{REF}}{V_{OUTA}} \]
Multiplier

The multiplier output of the UCC28517 is a signal representing the desired input line current. It is an input to the current amplifier, which programs the current loop to control the input current to give high-PF operation. As such, the proper functioning of the multiplier is key to the success of the design. The output of the multiplier, $I_{MOUT}$, can be expressed as

$$I_{MOUT} = I_{IAC} \frac{V_{eal(max)} - 1}{K \times V_{VFF}}$$

where $K$ is a constant typically equal to $1/V$.

The $I_{IAC}$ signal is obtained through a high-value resistor ($R_{IAC} = R18 + R24$) connected between the rectified ac line and the IAC pin of the UCC28517. This resistor is sized to give the maximum $I_{IAC}$ current at the highest expected line voltage. For the UCC28517 the maximum $I_{IAC}$ current is about 500 $\mu$A. A higher current than this can drive the multiplier out of its linear range. A smaller current level is functional; but noise can become an issue, especially during low line voltages, assuming a universal line operation of 85 to 265 Vac gives an $R_{IAC}$ value of 750 k$\Omega$.

Because of voltage-rating constraints of standard $\frac{1}{4}$-W resistors, two or more lower-value resistors connected in series are needed to give roughly a 750-k$\Omega$ value and to distribute the high voltage across them.

The current through $R_{IAC}$ is mirrored internally to the VFF pin, where it is filtered to produce a voltage feed-forward signal proportional to line voltage that is free of the 120-Hz ripple component. This second harmonic ripple component at the VFF pin is one of the major contributors to harmonic distortion in the system, so adequate filtering is crucial (see Reference 4). Assuming that an allocation of 1.5% total harmonic distortion from this input is allowed, and that the second harmonic ripple is 66% of the input ac line voltage, the amount of attenuation required by this filter is

$$\frac{1.5\%}{66\%} = 0.022 \text{ (see Reference 5).}$$

A ripple frequency ($f_R$) of 120 Hz and an attenuation of 0.022 gives us a single-pole filter with

$$f_p = 120 \text{ Hz} \times 0.022 = 2.6 \text{ Hz}.$$ 

The voltage at the VFF pin not only supplies a voltage feed-forward signal but also activates input current foldback when the $V_{VFF}$ drops below 1.5 V. Please see Reference 2 for a detailed explanation of how these control ICs provide power limiting. The following equations were used to size resistor R30 and filter capacitor C20.

$$R30 = \frac{1.5 \text{ V}}{\frac{V_{IN(min)} \times 0.9}{(R18 + R24) \times 2}}$$ 

$$C20 = \frac{1}{2\pi \times 30 \text{ k}\Omega \times 2.6 \text{ Hz}}$$

This results in a single-pole filter, which adequately attenuates the harmonic distortion and provides power limiting.

The multiplier’s output resistor R19 is sized to match the maximum current through the sense resistor (R5) to the maximum multiplier current. R15 is sized to balance the offset current in the current amplifier and needs to be set to the same value as R19. The following equations were used to size R15 and R19.

$$I_{MOUT(max)} = \frac{I_{IAC} \times V_{IN(min)} \times (V_{eal(max)} - 1 \text{ V})}{K \times V_{VFF}}$$

$$R19 = R15 = \frac{V_{dynamic}}{I_{MOUT(max)}}$$

Current loop compensation for the boost converter

The following equation defines the gain of the power stage, where $V_P$ is the maximum voltage swing of the UCC28517 oscillator ramp, roughly 5 V.

$$G_{ID}(s) = \frac{V_{OUTA} \times R5}{s \times L1 \times V_P}$$

To have a good dynamic response, the crossover frequency of the current loop was set to $\frac{f_0}{2}$ the switching frequency. This can be achieved by setting the gain of the current amplifier ($G_{CA}$) to the inverse of the current loop power-stage gain at the crossover frequency. For this design the current amplifier required a gain of 2.581 at 10 kHz. The following equations were used to compensate the current amplifier of the boost power stage.

$$G_{CA} = \frac{1}{G_{ID}(s)} = 2.581$$

$$R17 = G_{CA} \times R19$$

$$C19 = \frac{1}{2\pi \times R17 \times \frac{f_{SA}}{10}}$$

$$C22 = \frac{1}{2\pi \times R17 \times \frac{f_{SA}}{2}}$$
Voltage loop compensation for the boost converter

Figure 4 shows the small-signal-control block diagram for this application. The following equations describe small-signal gain as well as the voltage loop frequency response, $T_s(f)$.

$$H(s) = \frac{R20}{R20 + R32 + R32}$$

$$G_c(s) = g_m \times \frac{s(f) \times R28 \times C23 + 1}{s(f) \times (C23 + C25) \times \left( \frac{s(f) \times C23 \times C25}{C23 + 25} + 1 \right)}$$

$$G_{col}(s) = \frac{\Delta V_{OUTA}}{\Delta V_c} = \frac{P_{OUTA}}{V_{eal(max)} \times s \times V_{OUTA} \times C3}$$

$$T_s(f) = -H(s) \times G_c(s) \times G_{col}(s)$$

To reduce third-harmonic distortion, the voltage loop typically crosses over at roughly 10 to 12 Hz. For this design, the voltage-loop crossover frequency ($f_c$) was selected to be roughly 10 Hz. The following equations were used to select the components to compensate the voltage loop, $T_s(f)$, to cross over at the desired $f_c$ with 45 degrees of phase margin.

$$R28 = 2\pi \times V_{eal(max)} \times f_c \times C3 \times \frac{V_{OUTA} \times n1}{g_m \times P_{OUTA} \times H(s)}$$

$$C23 = \frac{1}{2\pi \times R28 \times f_c}$$

C25 was selected to attenuate the 120-Hz output ripple voltage ($V_{pp}$) to 1.5% (% THD) of the voltage amplifier's dynamic output range.

After the design was complete, the frequency response of the voltage loop, $T_s(f)$, was measured with a network analyzer; and the results are shown in Figure 5. It can be observed that $f_c$ was roughly 8 Hz with a phase margin of roughly 50 degrees.
Summary
This article reviewed the design of a 100-W PFC ac/dc preregulator, which is the first stage in a two-stage power converter. The UCC2851X family of combination PWM controllers is perfect for offline applications that require PFC and auxiliary power supplies to meet different system requirements. The performance of this two-stage power converter is shown in Figures 6–9.

References
For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/litnumber and replace “litnumber” with the TI Lit. # for the materials listed below.

Document Title

TI Lit. #
3. Slup117
4. Slup093
5. Slup106
6. Slup110
7. Slup517
8. Sluu117

Related Web sites
analog.ti.com
www.ti.com/sc/device/TL431
www.ti.com/sc/device/UCC28517
www.ti.com/sc/analogapps
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI’s standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI products or services and is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

- **Products**
  - Amplifiers: amplifier.ti.com
  - Data Converters: dataconverter.ti.com
  - DSP: dsp.ti.com
  - Interface: interface.ti.com
  - Logic: logic.ti.com
  - Power Mgmt: power.ti.com
  - Microcontrollers: microcontroller.ti.com

- **Applications**
  - Audio: www.ti.com/audio
  - Automotive: www.ti.com/automotive
  - Broadband: www.ti.com/broadband
  - Digital control: www.ti.com/digitalcontrol
  - Military: www.ti.com/military
  - Optical Networking: www.ti.com/opticalnetwork
  - Security: www.ti.com/security
  - Telephony: www.ti.com/telephony
  - Video & Imaging: www.ti.com/video
  - Wireless: www.ti.com/wireless

**TI Worldwide Technical Support**

**Internet**
- TI Semiconductor Product Information Center Home Page: support.ti.com
- TI Semiconductor KnowledgeBase Home Page: support.ti.com/sc/knowledgebase

**Product Information Centers**

**Americas**
- **Phone**: +1(972) 644-5580
- **Fax**: +1(972) 927-6377

**Europe, Middle East, and Africa**
- **Phone (Belgium (English))**: +32 (0) 27 45 54 32
- **Fax (Belgium)**: +32 (0) 3 215 80 44
- **Phone (Finland (English))**: +358 (0) 9 2517 3948
- **Fax (Finland)**: +358 (0) 9 215 73 948
- **Phone (France)**: +33 (0) 1 30 70 11 54
- **Fax (France)**: +33 (0) 1 30 70 90 00
- **Phone (Germany)**: +49 (0) 8161 80 33 11
- **Fax (Germany)**: +49 (0) 8161 80 33 11
- **Phone (Israel (English))**: 1800 949 0107
- **Fax (Israel)**: 080 80 80 00
- **Phone (Italy)**: 800 79 11 37
- **Fax (Italy)**: 0800 79 11 37
- **Phone (Japan)**: +81 (0) 3 3344 5317
- **Fax (Japan)**: +81 (0) 3 3344 5317

**Asia**
- **Phone (Australia)**: 1-800-999-084
- **Fax (Australia)**: 1-800-999-084
- **Phone (China)**: 800-820-8682
- **Fax (China)**: 800-820-8682
- **Phone (Hong Kong)**: 800-96-5941
- **Fax (Hong Kong)**: 800-96-5941
- **Phone (Indonesia)**: 001-803-8861-1006
- **Fax (Indonesia)**: 001-803-8861-1006
- **Phone (Israel)**: +972-3-305-2804
- **Fax (Israel)**: +972-3-305-2804
- **Phone (Japan)**: +81-3-3344-5317
- **Fax (Japan)**: +81-3-3344-5317
- **Phone (Malaysia)**: 1-800-80-3373
- **Fax (Malaysia)**: 1-800-80-3373
- **Phone (Philippines)**: 800-96-5941
- **Fax (Philippines)**: 800-96-5941
- **Phone (Singapore)**: 800-96-5941
- **Fax (Singapore)**: 800-96-5941
- **Phone (South Korea)**: 080-551-2804
- **Fax (South Korea)**: 080-551-2804
- **Phone (Spain)**: +34 902 35 40 28
- **Fax (Spain)**: +34 902 35 40 28
- **Phone (Sweden)**: +46 (0) 8 587 555 22
- **Fax (Sweden)**: +46 (0) 8 587 555 22
- **Phone (Switzerland)**: +41 (0) 1 30 70 11 54
- **Fax (Switzerland)**: +41 (0) 1 30 70 90 00
- **Phone (United Kingdom)**: +44 (0) 1604 66 33 99
- **Fax (United Kingdom)**: +44 (0) 1604 66 33 99

**Safe Harbor Statement:** This publication may contain forward-looking statements that involve a number of risks and uncertainties. These “forward-looking statements” are intended to qualify for the safe harbor from liability established by the Private Securities Litigation Reform Act of 1995. These forward-looking statements generally can be identified by phrases such as TI or its management “believes,” “expects,” “anticipates,” “foresees,” “forecasts,” “estimates” or other words or phrases of similar import. Similarly, such statements herein that describe the company’s products, business strategy, outlook, objectives, expected results and the like, are forward-looking statements that involve a number of risks and uncertainties. TI’s actual results and outcomes may differ materially from the estimates or predictions in these forward-looking statements. These forward-looking statements reflect the current views, expectations of management concerning future events and are subject to numerous risks and uncertainties. For a discussion of important factors that might cause actual results to differ from those that are forward-looking statements, see “Risk Factors” in TI’s most recent Annual Report on Form 10-K and any subsequent Quarterly Reports on Form 10-Q. Users of this publication should review the most recent reports and filings by TI with the Securities and Exchange Commission and are urged to carefully review and consider the detailed disclosures made by TI in those reports.

**Trademarks:** All trademarks are the property of their respective owners.

**Mailing Address:**
Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

© 2005 Texas Instruments Incorporated